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# SX8650

World's Lowest Power & Smallest Footprint 4-wire Resistive Touchscreen Controller with 15kV ESD

**ADVANCED COMMUNICATIONS & SENSING** DATASHEET

## GENERAL DESCRIPTION

The SX8650 is an ultra low power 4-wire resistive touchscreen controller optimized for portable equipment where power and board-space are at a premium.

It incorporates a highly accurate 12-bit ADC for data conversion and operates from a single 1.65 to 3.7V supply voltage.

The SX8650 features a built-in preprocessing algorithm for data measurements, which greatly reduces the host processing overhead and bus activity. This complete touchscreen solution includes four user-selectable operation modes which offer programmability on different configurations such as conversion rate and settling time, thus enable optimization in throughput and power consumption for a wide range of touch sensing applications.

The touch screen inputs have been specially designed to provide robust on-chip ESD protection of up to ±15kV in both HBM and Contact Discharge, and eliminates the need for external protection devices.

The SX8650 supports the Fast-mode I²C (400kbit/s) serial bus data protocol and includes 2 user-selectable slave addresses. A custom I2C address is possible on request.

The SX8650 is offered in two tiny packages: 3.0 mm x 3.0 mm DFN and a 1.5 mm x 2.0 mm wafer-level chip-scale package (WLCSP).

## APPLICATIONS

- Portable Equipment
- Mobile Communication Devices
- Cell phone, PDA, MP3, GPS, DSC
- Touch Screen Monitors

## KEY PRODUCT FEATURES

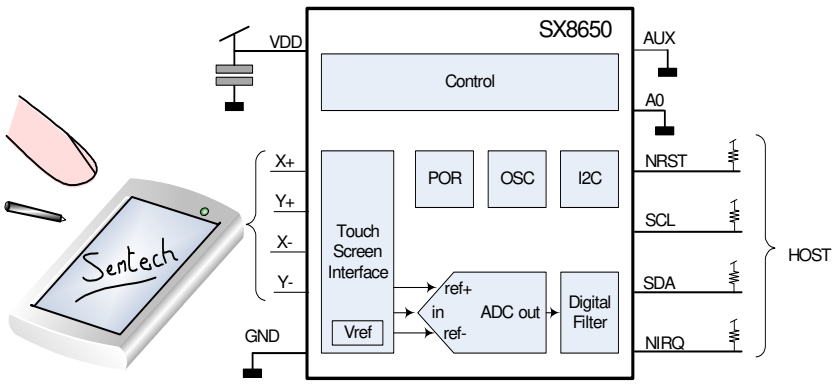
- Extremely Low Power Consumption: 23uA@1.8V 8kSPS
- Superior On-chip ESD Protection
  - ⇨±15kV HBM (X+,X-,Y+,Y-)
  - ⇨±2kV CDM
  - ⇨±25kV Air Gap Discharge
  - ⇨±15kV Contact Discharge
  - ⇨±300V MM
- Single 1.65V to 3.7V Supply/Reference
- Integrated Preprocessing Block to Reduce Host Loading and Bus Activity
- Four User Programmable Operation Modes provides Flexibility to address Different Application Needs
  - ⇨Manual, Automatic, Pen Detect, Pen Trigger
- High Precision 12-bit Resolution
- Low Noise Ratiometric Conversion
- Selectable Polling or Interrupt Modes
- Touch Pressure Measurement
- 400kHz Fast-Mode I²C Interface
- Hardware Reset & I²C Software Reset
- -40℃ to 85℃ Operation
- 12-LD (3.0 mm x 3.0 mm) DFN Package
- 12-Ball (1.5 mm x 2.0 mm) WLCSP Package
- Pin-compatible with SX8651
- Pb-Free, Halogen Free, RoHS/WEEE compliant product
- Windows CE 6.0, Linux Driver Support Available

## ORDERING INFORMATION

| Part Number | Package |
|---|---|
| SX8650ICSTRT[1] | 12 - Ball WLCSP (1.5 mm x 2.0 mm) |
| SX8650IWLTRT[1] | 12 - Lead DFN (3.0 mm x 3.0 mm) |

1. 3000 Units / reel

## Block Diagram



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# 1. General Description

## 1.1. DFN Pinout Diagram and Marking Information (Top View)

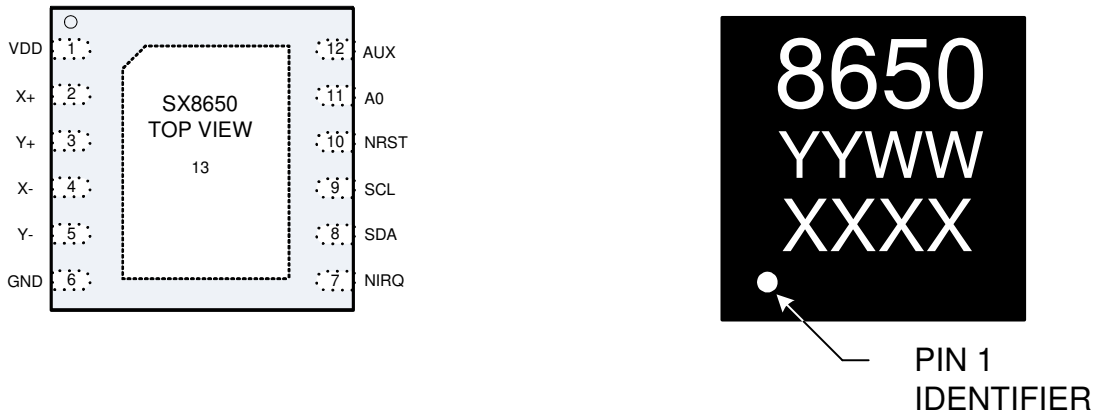



*Figure 1. SX8650SX8650 DFN Top View, Pad on Bottom Side*

YYWW : date code
XXXXX: Lot Number

## 1.2. WLCSP Pinout Diagram and Marking Information (Top View)

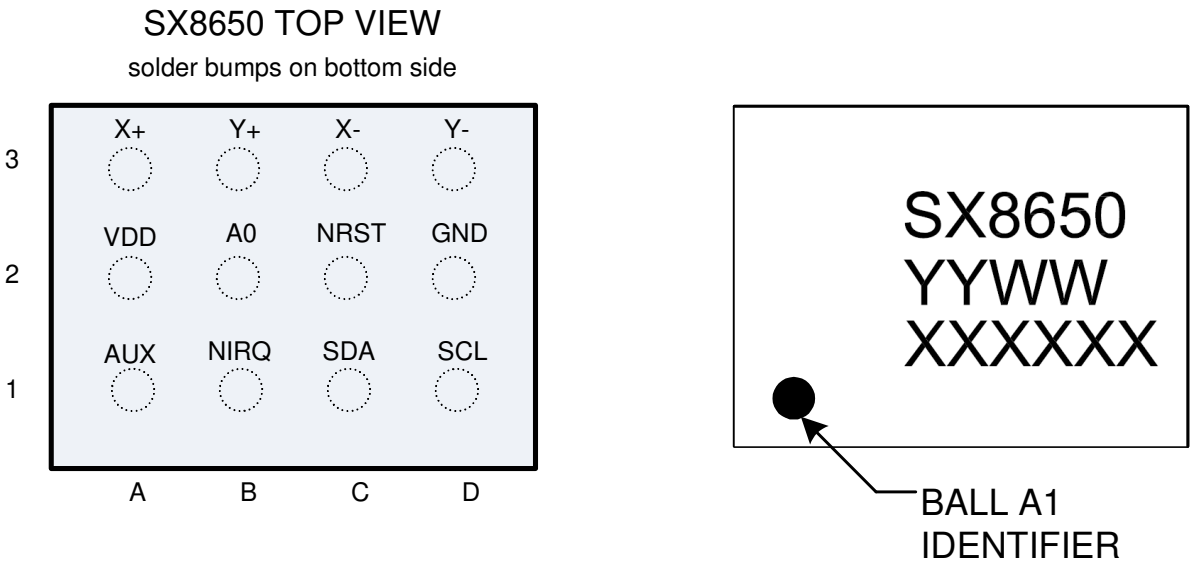



*Figure 2. SX8650 WLCSP Top View, Solder Bumps on Bottom Side*

YYWW : date code
XXXXX: Lot Number

## 1.3. Pin Description

| Pin Number # | | Name | Type | Description |
|---|---|---|---|---|
| DFN | WLCSP | | | |
| 1 | A2 | VDD | Power | Input power supply connect to a 0.1uF capacitor to GND |
| 2 | A3 | X+ | Analog | X+ channel input |
| 3 | B3 | Y+ | Analog | Y+ channel input |
| 4 | C3 | X- | Analog | X- channel input |
| 5 | D3 | Y- | Analog | Y- channel input |
| 6 | D2 | GND | Ground | Ground |
| 7 | B1 | NIRQ | Digital Output / Open Drain Output | Interrupt output, active low. Need external pull-up resistor |
| 8 | C1 | SDA | Digital Input / Open Drain Output | I2C data input/output |
| 9 | D1 | SCL | Digital Input / Open Drain Output | I2C clock, input/output |
| 10 | C2 | NRST | Digital Input / Output | Reset Input, active low. Need external 50k pull-up resistor |
| 11 | B2 | A0 | Digital Input | I2C slave address selection input |
| 12 | A1 | AUX | Digital Input/Analog Input | Analog auxiliary input or conversion synchronization |
| 13 | | GND | Ground | Die attach paddle, connect to Ground |

*Table 1 Pin description*

## 1.4. Simplified Block Diagram

The SX8650 simplified block diagram is shown in Figure 3.

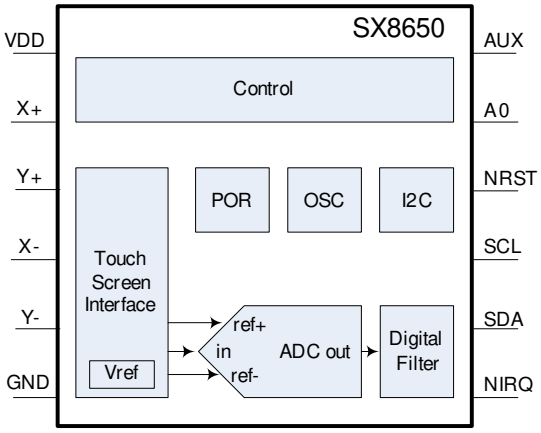



*Figure 3. Simplified block diagram of the SX8650*

## 2. Electrical Characteristics

Stresses above the values listed in "Absolute Maximum Ratings" may cause permanent damage to the device.
This is a stress rating only and functional operation of the device at these, or any other conditions beyond the "Recommended Operating Conditions", is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

| Parameter | | Symbol | Min. | Max. | Unit |
|---|---|---|---|---|---|
| Supply Voltage | | $V_{DDABS}$ | -0.5 | 3.9 | V |
| Input voltage (non-supply pins) | | $V_{IN}$ | -0.5 | 3.9 | V |
| Input current (non-supply pins) | | $I_{IN}$ | | 10 | mA |
| Operating Junction Temperature | | $T_{JCT}$ | | 125 | ℃ |
| Reflow temperature | | $T_{RE}$ | | 260 | ℃ |
| Storage temperature | | $T_{STOR}$ | -50 | 150 | ℃ |
| ESD HBM (Human Body Model) | High ESD pins: X+, X-,Y+,Y- | $ESD_{HBM1}$ | ± 15(i) | | kV |
| | | | ± 8(ii) | | kV |
| | All pins except high ESD pins: AUX,A0,NRST,NIRQ,SDA,SCL | $ESD_{HBM2}$ | ± 2 | | kV |
| ESD (Contact Discharge) | High ESD pins: X+, X-,Y+,Y- | $ESD_{CD}$ | ± 15 | | kV |
| Latchup | | $I_{LU}$ | ± 100(iii) | | mA |

*Table 2. Absolute Maximum Ratings*

(i) Tested to TLP (10A)
(ii) Tested to JEDEC standard JESD22-A114
(iii) Tested to JEDEC standard JESD78

### 2.1. Recommended Operating Conditions

| Parameter | Symbol | Min. | Max | Unit |
|---|---|---|---|---|
| Supply Voltage | $V_{DD}$ | 1.65V | 3.7 | V |
| Ambient Temperature Range | $T_A$ | -40 | 85 | ℃ |

### 2.2. Thermal Characteristics

| Parameter | Symbol | Min. | Max | Unit |
|---|---|---|---|---|
| Thermal Resistance with DFN package - Junction to Ambient (i) | $\theta_{JA}$ | | 39 | ℃/W |
| Thermal Resistance with WLCSP package - Junction to Ambient (i) | $\theta_{JA}$ | | 65 | ℃/W |

(iii) $\theta_{JA}$ is calculated from a package in still air, mounted to 3" x 4.5", 4 layer FR4 PCB with thermal vias under exposed pad (if applicable) per JESD51 standards.

## 2.3. Electrical Specifications

| Parameter | Symbol | Conditions | Min. | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **Current consumption** | | | | | | |
| Manual | $I_{pwd}$ | Manual (converter stopped, pen detection off, I2C listening, OSC stopped) | | 0.4 | 0.75 | uA |
| Pen Detect | $I_{pndt}$ | Pen detect mode (converter stopped, pen detection activated, device will generate interrupt upon detection, I2C listening, OSC stopped). | | 0.4 | 0.75 | uA |
| Pen Trigger | $I_{pntr}$ | Pen trigger mode (converter stopped, pen detection activated, device will start conversion upon pen detection. I2C listening, OSC stopped | | 0.4 | 0.75 | uA |
| Automatic | $I_{wt}$ | Automatic (converter stopped, pen detection off, I2C listening, OSC and timer on, device is waiting for timer expiry) | | 1.5 | | uA |
| Operation @8kSPS, VDD=1.8V | $I_{opl}$ | X,Y Conv. RATE=4kSPS, $N_{filt}$=1 PowDly=0.5us, SetDly=0.5us | | 23 | 50 | uA |
| Operation @42kSPS, VDD=3.3V | $I_{oph}$ | X,Y Conv. RATE=3kSPS, $N_{filt}$=7 PowDly=0.5us, SetDly=0.5us | | 105 | 140 | uA |
| **Digital I/O** | | | | | | |
| High-level input voltage [1] | $V_{IH}$ | | $0.7V_{DD}$ | | $V_{DD}$+0.5 | V |
| Low-level input voltage | $V_{IL}$ | | $V_{SS}$-0.3 | | $0.3V_{DD}$ | V |
| SDA / SCL Hysteresis of Schmitt trigger inputs<br>VDD > 2 V<br>VDD < 2 V | $V_{hys}$ | | <br>$0.05V_{DD}$<br>$0.1V_{DD}$ | | | V |
| Low-level output voltage | $V_{OL}$ | $I_{OL}$=3mA, $V_{DD}$>2V<br>$I_{OL}$=3mA, $V_{DD}$<2V | 0<br>0 | | 0.4<br>$0.2V_{DD}$ | V |
| Input leakage current | $L_I$ | CMOS input | | | ±1 | uA |
| **AUX** | | | | | | |
| Input voltage range | $V_{IAUX}$ | | 0 | | $V_{DD}$ | V |
| Input capacitance | $C_{X+}$,$C_{X-}$,$C_{Y+}$, $C_{Y-}$ | | | 50 | | pF |
| | $C_{AUX}$ | | | 5 | | pF |

| Parameter | Symbol | Conditions | Min. | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Input leakage current | $I_{IAUX}$ | | -1 | | 1 | uA |
| | | | | | | |
| **Startup** | | | | | | |
| Power-up time (Delay | $t_{POR}$ | Time between rising edge VDD and rising NIRQ | | | 1 | ms |
| | | | | | | |
| **Reset** | | | | | | |
| Reset low time | $t_{NRST}$ | | 50 | | | ns |
| | | | | | | |
| **ADC** | | | | | | |
| Resolution | $A_{res}$ | | 12 | | | bits |
| Offset | $A_{off}$ | | | ±1 | | LSB |
| Gain error | $A_{ge}$ | At full scale | | 0.5 | | LSB |
| Differential nonlinearity | $A_{dnl}$ | | | ±1 | | LSB |
| Integral nonlinearity | $A_{inl}$ | | | ±1.5 | | LSB |
| | | | | | | |
| **Resistors** | | | | | | |
| X+, X-, Y+, Y- resistance | $R_{chn}$ | Touch Pad Biasing Resistance | | 5 | | Ohm |
| Pen detect resistance | $R_{PNDT\_00}$ | $R_{PNDT}$ = 0 | | 100 | | kOhm |
| | $R_{PNDT\_01}$ | $R_{PNDT}$ = 1 | | 200 | | kOhm |
| | $R_{PNDT\_10}$ | $R_{PNDT}$ = 2 | | 50 | | kOhm |
| | $R_{PNDT\_11}$ | $R_{PNDT}$ = 3 | | 25 | | kOhm |
| | | | | | | |
| **External components** | | **recommendations** | | | | |
| Capacitor between VDD, GND | $C_{vdd}$ | Type 0402, tolerance +/-50% | | 0.1 | | uF |

1. SCL, SDA, NRST and NIRQ can be pulled up to a potential higher than the chip VDD but must not exceed the maximun voltage of 3.7V.

All values are valid within the recommended operating conditions unless otherwise specified.

## 2.4. Host Interface Specifications

| Parameter | Symbol | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **I2C TIMING SPECIFICATIONS** (i) | | | | | | |
| SCL clock frequency | $f_{SCL}$ | | 0 | | 400 | kHz |
| SCL low period | $t_{LOW}$ | | 1.3 | | | us |
| SCL high period | $t_{HIGH}$ | | 0.6 | | | us |
| Data setup time | $t_{SU;DAT}$ | | 100 | | | ns |
| Data hold time | $t_{HD;DAT}$ | | 0 | | | ns |
| Repeated start setup time | $t_{SU;STA}$ | | 0.6 | | | us |
| Start condition hold time | $t_{HD;STA}$ | | 0.6 | | | us |
| Stop condition setup time | $t_{SU;STO}$ | | 0.6 | | | us |
| Bus free time between stop and start | $t_{BUF}$ | | 1.3 | | | us |
| Data valid time | $t_{VD;DAT}$ | | | | 0.9 | us |
| Data valid ack time | $t_{VD;ACK}$ | | | | 0.9 | us |
| Pulse width of spikes that must be suppressed by the input filter | $t_{SP}$ | | | | 50 | ns |
| **I2C BUS SPECIFICATIONS** | | | | | | |
| Capacitive Load on each bus line SCL, SDA | $C_b$ | | | | 400 | pF |

*Table 3 Host Interface Specifications*

**Notes:**

(i) All timing specifications refer to voltage levels ($V_{IL}$, $V_{IH}$, $V_{OL}$) defined in Table 3 unless otherwise mentioned.

## 2.5. Host Interface Timing Waveforms

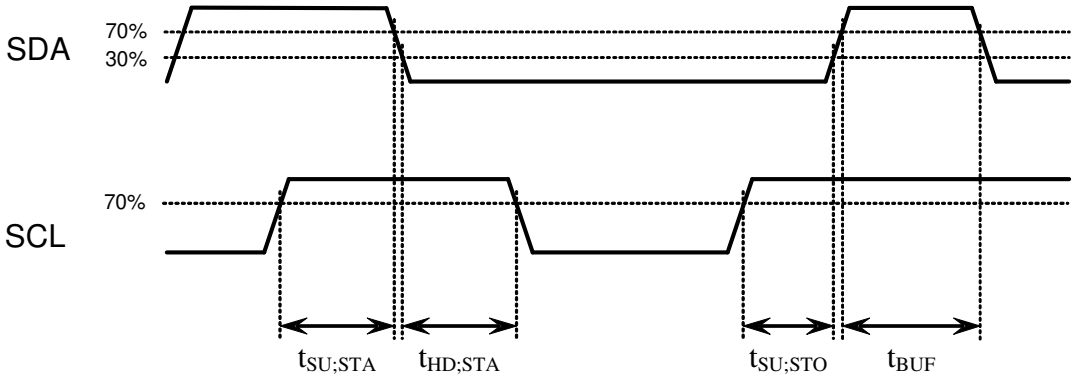



*Figure 4. I2C Start and Stop timing*

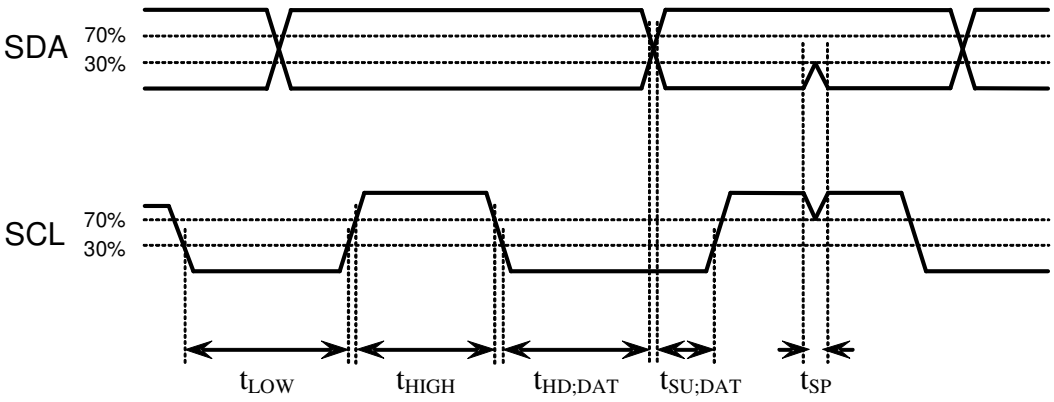
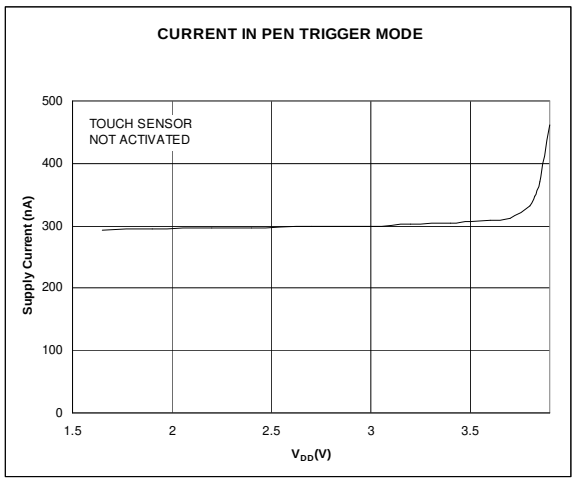
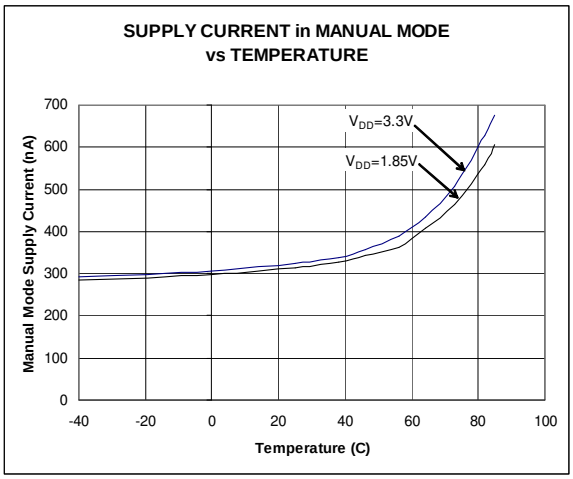


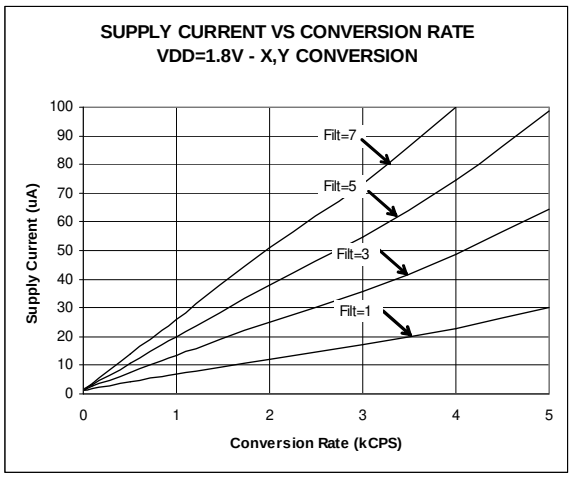

*Figure 5. I2C Data timing*

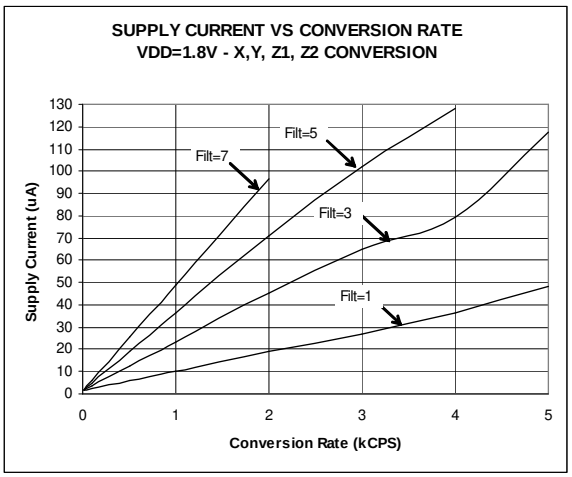
## 2.6. Typical Operating Characteristics

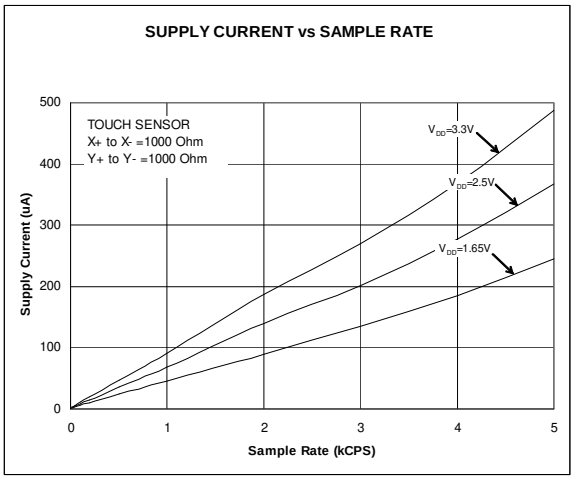
At Ta= -40°C to +85°C, VDD=1.7V to 3.7V, PowDly=0.5 us, SetDly=0.5us, Filt=1, Resistive touch screen sensor current not taking in account, unless otherwise noted.



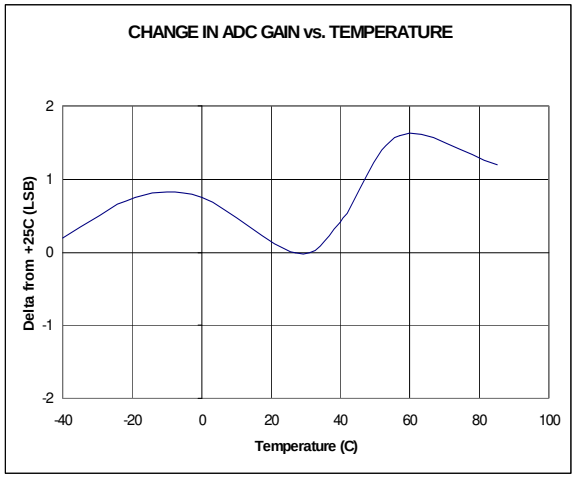



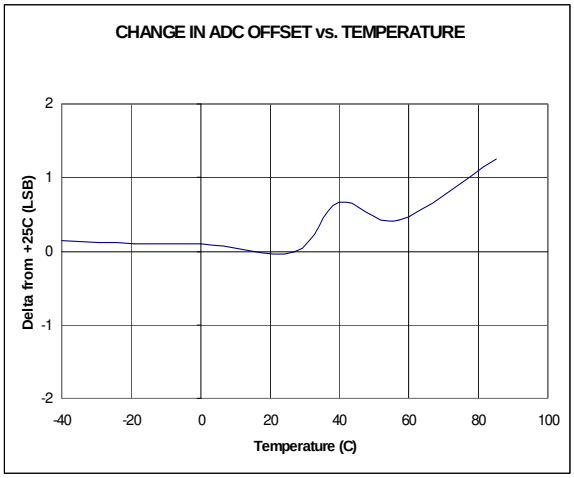



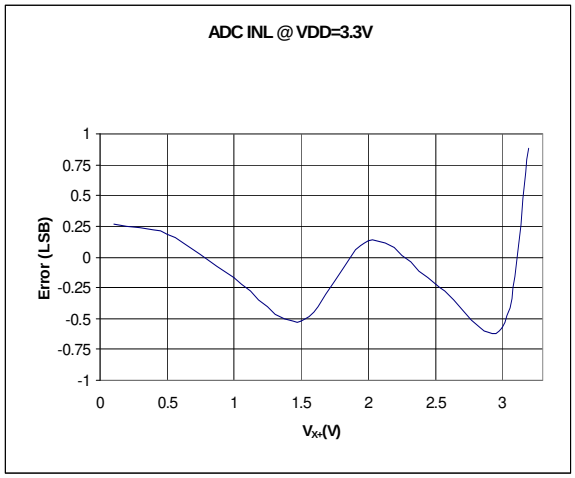



## Typical Operating Characteristics (continued)

At Ta= -40°C to +85°C, VDD=1.7V to 3.7V, PowDly=0.5 us, SetDly=0.5us, Filt=1, Resistive touch screen sensor current not taking in account, unless otherwise noted.



# 3. Functional Description

## 3.1. General Introduction

This section provides an overview of the SX8650 architecture, device pinout and a typical application.

The SX8650 is designed for 4-wire resistive touch screen applications (Figure 6).The touch screen or touch panel is the resistive sensor and can be activated by either a finger or stylus. The touch screen coordinates and touch pressure are converted into I2C format by the SX8650 for transfer to the host.

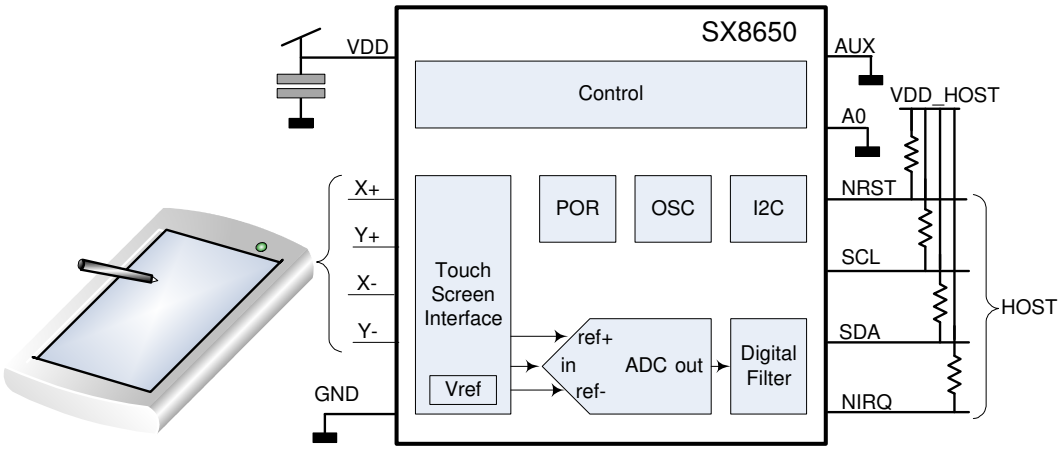



*Figure 6. SX8650 with screen*

## 3.2. Channel Pins

### 3.2.1. X+, X-, Y+. Y-

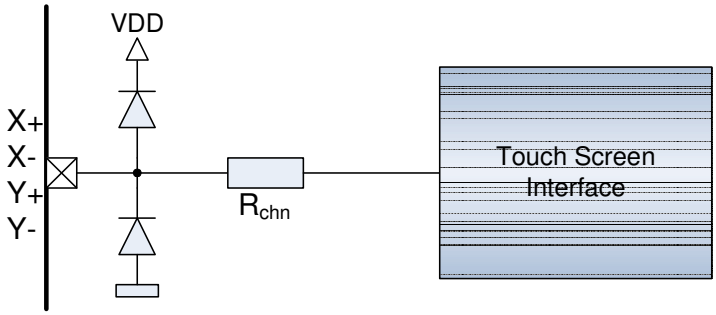



*Figure 7. Simplified diagram of X+, X-, Y+, Y- pins*

The SX8650's channel pins (X+, X-, Y+, Y-) directly connect to standard touch screen X and Y resistive layers. The SX8650 separately biases each of these layers and converts the resistive values into (X,Y) coordinates.

The channel pins are protected to VDD and GROUND.

Figure 7 shows the simplified diagram of the X+, X-, Y+, Y- pins.

### 3.2.2. AUX

The SX8650 interface includes an AUX pin that serves two functions: an ADC input; and a start of conversion trigger. When used as an ADC, the single ended input range is from GND to VDD, referred to GND. When the AUX input is configured to start conversions, the AUX input can be further configured as a rising and / or falling edge trigger.

The AUX is protected to VDD and GROUND.

Figure 8 shows a simplified diagram of the AUX pin.

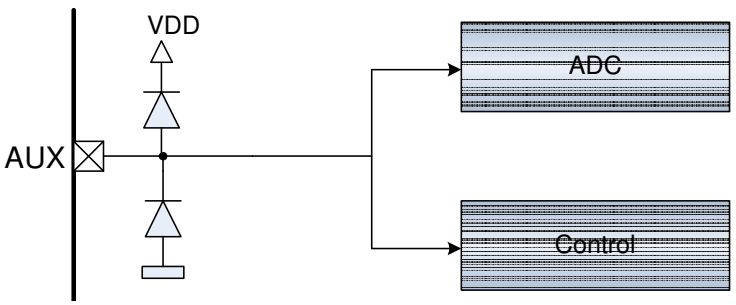
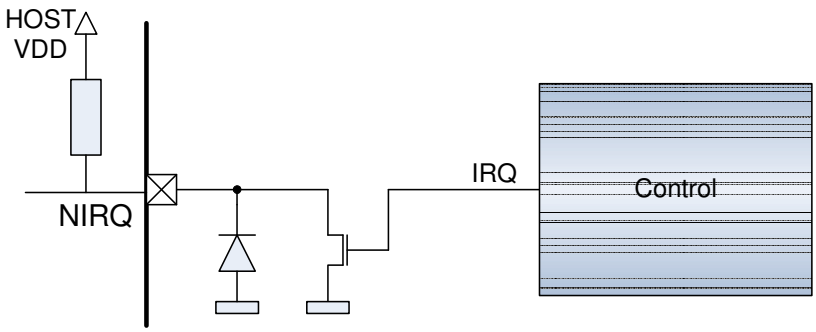



*Figure 8. Simplified diagram of AUX*

## 3.3. Host Interface and Control Pins

The SX8650 host and control interface consists of: NIRQ, I2C pins SCL and SDA, A0, and NRST.

### 3.3.1. NIRQ




The NIRQ pin is an active low, open drain output to facilitate interfacing to different supply voltages and thus requires an external pull-up resistor (1-10 kOhm). The NIRQ pin does not have protection to VDD.

The NIRQ function is designed to provide an interrupt to the host processor. Interrupts may occur when a pen is detected, or when channel data is available.

Figure 9 shows a simplified diagram of the NIRQ pin.

*Figure 9. Simplified diagram of NIRQ*

### 3.3.2. SCL

The SCL pin is a high-impedance input and open-drain output pin. The SCL pin does not have protection to VDD to conform to I2C slave specifications. An external pull-up resistor (1-10 kOhm) is required.

Figure 10 shows the simplified diagram of the SCL pin.

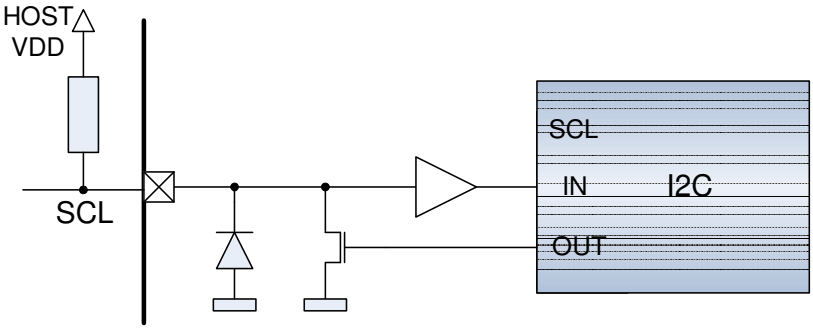
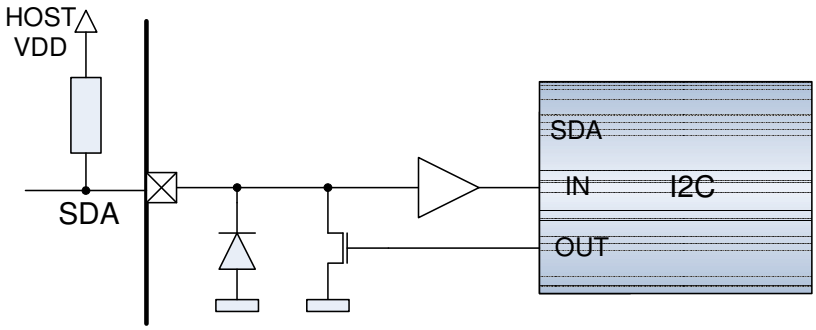



*Figure 10. Simplified diagram of SCL*

### 3.3.3. SDA




SDA is an I/O pin. It can be used as an open-drain output (with external pull-up resistor) or as an input. An external pull-up resistor (1-10 kOhm) is required.

The SDA I/O pin does not have protection to VDD to conform to I2C slave specifications.

Figure 11 shows a simplified diagram of the SDA pin.

*Figure 11. Simplified diagram of SDA*

### 3.3.4. A0

The A0 pin is connected to the I2C address select control circuitry and is used to modify the device I2C address.

The A0 pin is protected to GROUND.

Figure 12 shows a simplified diagram of the A0 pin.

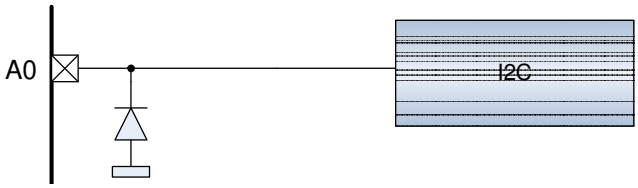
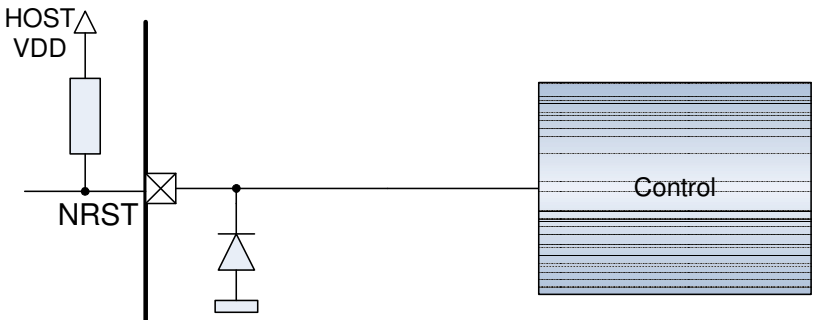



*Figure 12. Simplified diagram of A0*

### 3.3.5. NRST




The NRST pin is an active low input that provides a hardware reset of the SX8650's control circuitry.

The NRST pin is protected GROUND to enable interfacing with devices at a different supply voltages.

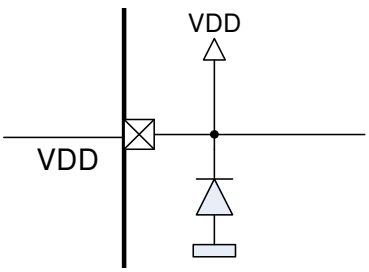
Figure 13 shows a simplified diagram of the NRST pin.

*Figure 13. Simplified diagram of NRST*

## 3.4. Power Management Pins

The SX8650's power management input consists of the following Power and Ground pins.

### 3.4.1. VDD



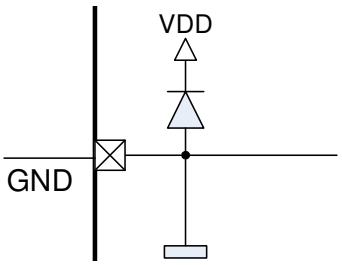

The VDD is a power pin and is the power supply for the SX8650.

The VDD has ESD protection to GROUND.

Figure 14 shows a simplified diagram of the VDD pin.

*Figure 14. Simplified diagram of VDD*

### 3.4.2. GND




The SX8650 has one power management ground pin, GND. (The die attach paddle on DFN is also connected to GND.)

The GND has ESD protection to VDD.

Figure 15 shows a simplified diagram of the GND pin.

*Figure 15. Simplified diagram of GND*

# 4. Detailed Description

## 4.1. Touch Screen Operation

A resistive touch screen consists of two (resistive) conductive sheets separated by an insulator when not pressed. Each sheet is connected through 2 electrodes at the border of the sheet (Figure 16). When a pressure is applied on the top sheet, a connection with the lower sheet is established. Figure 17 shows how the Y coordinate can be measured. The electrode plates are connected through terminals X+, X- and Y+, Y- to an analog to digital converter (ADC) and a reference voltage. The resistance between the terminals X+ and X- is defined by Rxtot. Rxtot will be split in 2 resistors, R1 and R2, in case the screen is touched. The resistance between the terminals Y+ and Y- is represented by R3 and R4. The connection between the top and bottom sheet is represented by the touch resistance ($R_T$).

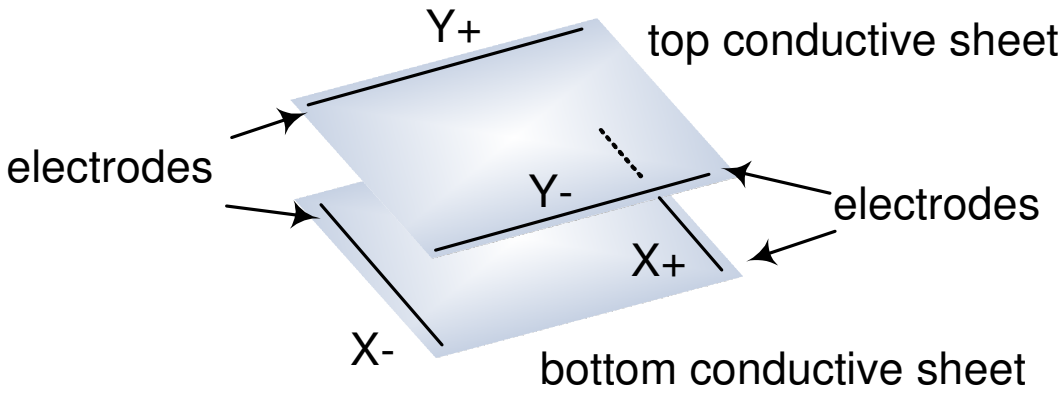



*Figure 16. 4-wire Touch Screen*

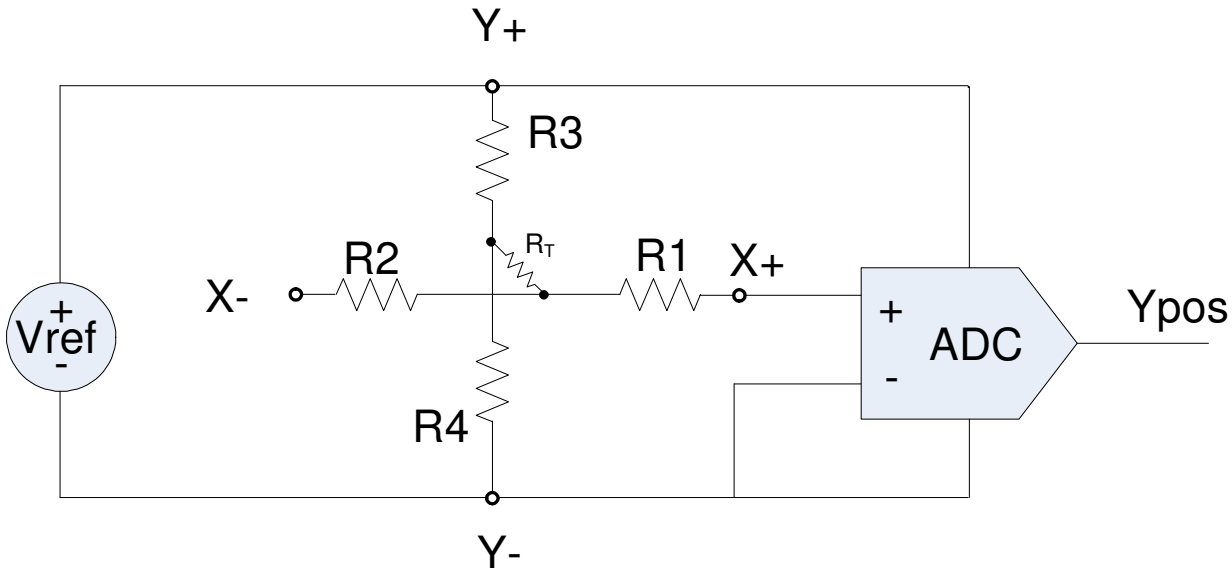



*Figure 17. Touch Screen Operation ordinate measurement (Y)*

### 4.2. Coordinates Measurement

The top resistive sheet (Y) is biased with a voltage source. Resistors R3 and R4 determine a voltage divider proportional to the Y position of the contact point. Since the converter has a high input impedance, no current flows through R1 so that the voltage X+ at the converter input is given by the voltage divider created by R3 and R4.

The X coordinate is measured in a similar fashion with the bottom resistive sheet (X) biased to create a voltage divider by R1 and R2, while the voltage on the top sheet is measured through R3. Figure 18 shows the coordinates measurement setup. The resistance $R_T$ is the resistance obtained when a pressure is applied on the screen. $R_T$ is created by the contact area of the X and Y resistive sheet and varies with the applied pressure.

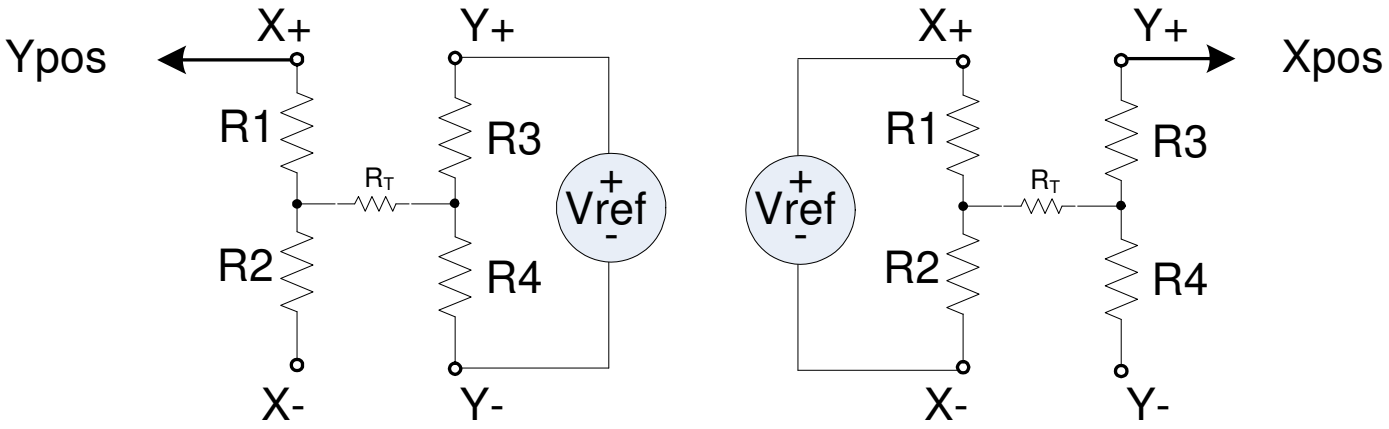



*Figure 18. Ordinate (Y) and abscissa (X) coordinates measurement setup*

The X and Y position are found by: $Xpos = 4095 \cdot \frac{R2}{R1 + R2}$ $Ypos = 4095 \cdot \frac{R4}{R3 + R4}$

### 4.3. Pressure Measurement

The pressure measurement consists of two additional setups: z1 and z2 (see Figure 19).

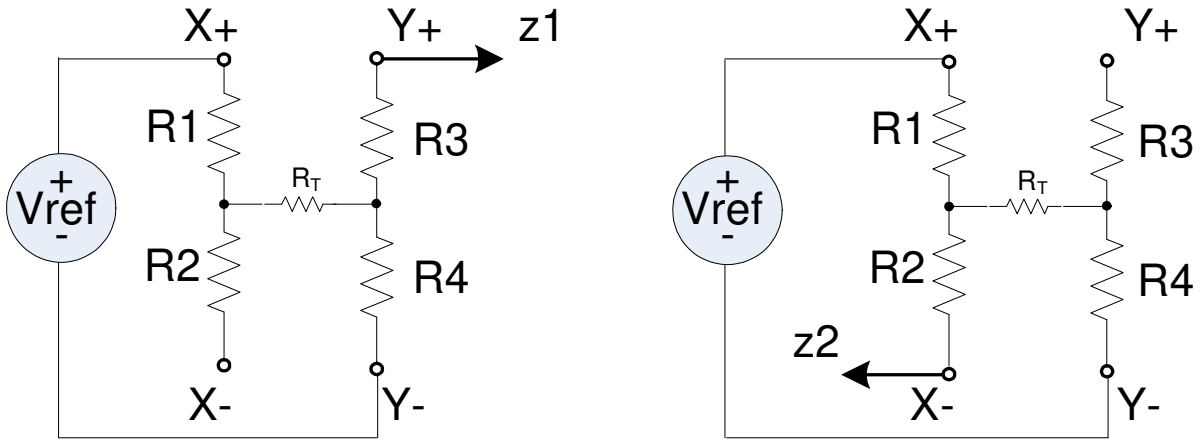



*Figure 19. z1 and z2 pressure measurement setup*

The corresponding equations for the pressure: $z1 = 4095 \cdot \frac{R4}{R1 + R4 + R_T}$ $z2 = 4095 \cdot \frac{R4 + Rt}{R1 + R4 + R_T}$

The X and Y total sheet resistance (Rxtot, Rytot) are known from the touch screen supplier.

$$Rxtot = R1 + R2$$

$$Rytot = R3 + R4$$

R4 is proportional to the Y coordinate.

The R4 value is given by the total Y plate resistance multiplied by the fraction of the Y position over the full coordinate range.

$$R4 = Rytot \cdot \frac{Ypos}{4095}$$

By re-arranging z1 and z2 one obtains

$$R_T = R4 \cdot \left[\frac{z2}{z1} - 1\right]$$

Which results in:

$$R_T = Rytot \cdot \frac{Ypos}{4095} \cdot \left[\frac{z2}{z1} - 1\right]$$

The touch resistance calculation above requires three channel measurements (Ypos, z2 and z1) and one specification data (Rytot).An alternative calculation method is using Xpos, Ypos, one z channel and both Rxtot and Rytot shown in the next calculations

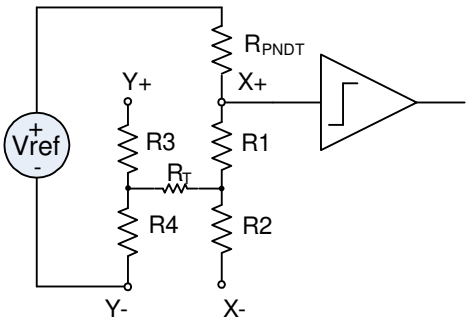
R1 is inverse proportional to the X coordinate.

$$R1 = Rxtot \cdot \left[1 - \frac{Xpos}{4095}\right]$$

Substituting R1 and R4 into z1 and rearranging terms gives:

$$R_T = \frac{Rytot \cdot Ypos}{4095} \cdot \left[\frac{4095}{z1} - 1\right] - Rxtot \cdot \left[1 - \frac{Xpos}{4095}\right]$$

## 4.4. Pen Detection




The pen detection circuitry is used both to detect a user action and generate an interrupt or start an acquisition in PENDET and PENTRG mode respectively. Doing a pen detection prior to conversion avoids feeding the host with dummy data and saves power.

If the touchscreen is powered between X+ and Y- through a resistor $R_{PNDT}$, no current will flow so long as pressure is not applied to the surface (see Figure 20). When some pressure is applied, a current path is created and brings X+ to the level defined by the resistive divider determined by $R_{PNDT}$ and the sum of R1, $R_T$ and R4.

The level is detected by a comparator.

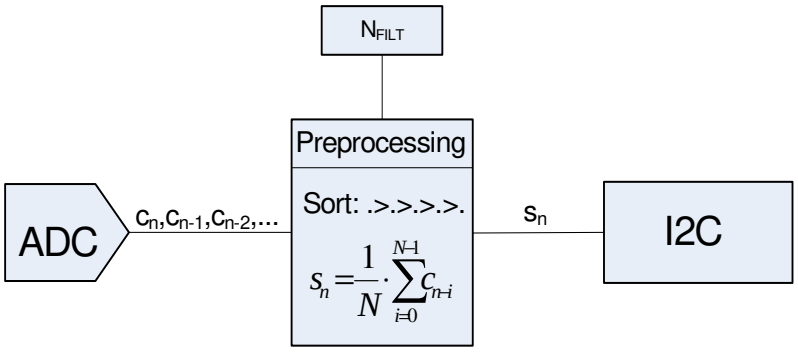
*Figure 20. Pen detection*

$R_{PNDT}$ should be set to the greatest value 200 kOhm for optimal detection (see Table 6). Increasing PowDly settings can also improve the detection on panel with high resistance.

The pen detection will set the PENIRQ bit of the RegStat register.

In PENDET mode, the pen detection will set NIRQ low. The PENIRQ bit will be cleared and the NIRQ will be de-asserted as soon as the host reads the status register.

# 5. Data Processing




The SX8650 offers 4 types of data processing which allows the user to make trade-offs between data throughput, power consumption and noise rejection.

The parameter FILT is used to select the filter order $N_{filt}$ . The noise rejection will be improved with a high order to the detriment of the power consumption. The K coefficient in Table 4 is a filter constant. Its value is K=4079/4095.

*Figure 21. Filter structure*

.

| FILT | $N_{filt}$ | Processing |
|---|---|---|
| 0 | 1 | $s_n = c_n$<br>No average. |
| 1 | 3 | $= \frac{1}{3} \cdot \frac{4079}{4095}(c_n + c_{n-1} + c_{n-2})$<br>3 ADC samples are averaged |
| 2 | 5 | $= \frac{1}{5} \cdot \frac{4079}{4095}(c_n + c_{n-1} + c_{n-2} + c_{n-3} + c_{n-4})$<br>5 ADC samples are averaged |
| 3 | 7 | $c_{max1} \geq c_{max2} \geq c_a \geq c_b \geq c_c \geq c_{min1} \geq c_{min2}$<br>$= \frac{1}{3} \cdot \frac{4079}{4095}(c_a + c_b + c_c)$<br>7 ADC samples are sorted and the 3 center samples are averaged |

*Table 4. Filter order*

## 5.1. Host Interface and Control

The host interface consists of I2C (SCL and SDA) and the NIRQ, A0, NRST signals.

The I2C implemented on the SX8650 is compliant with:

- Standard Mode (100 kbit/s) & Fast Mode (400 kbit/s)
- Slave mode
- 7 bit slave address

### 5.1.1. I2C Address

Pin A0 defines the LSB of the I2C address. It is shown on Figure 22.

.

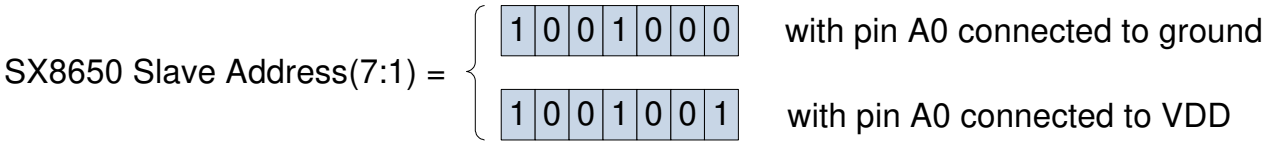



*Figure 22. I2C slave address*

Upon request of the customer, a custom I2C address can be burned in the NVM.

The host uses the I2C to read and write data and commands to the configuration and status registers. During a conversion, the I2C clock can be stretched until the end of the processing.

Channel data read is done by I2C throughput optimized formats.

The supported I2C access formats are described in the next sections:

- I2C Write Registers
- I2C Read Registers
- I2C Host Commands
- I2C Read Channels

### 5.1.2. I2C Write Registers

The format for I2C write is given in Figure 23.

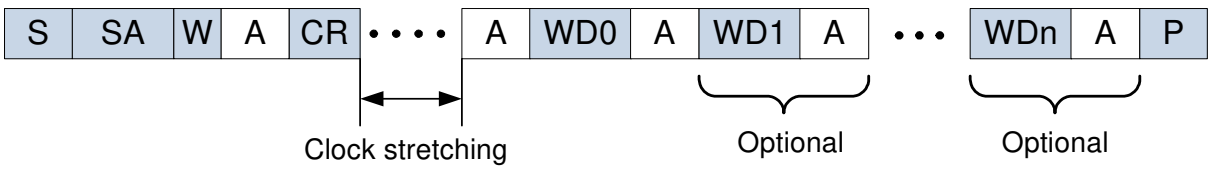
After the start condition [S], the SX8650 slave address (SA) is sent, followed by an eighth bit (W='0') indicating a Write.

The SX8650 then Acknowledges [A] that it is being addressed, and the host sends 8-bit Command and Register address consisting of the command bits '000' followed by the SX8650 Register Address (RA).

The SX8650 Acknowledges [A] and the host sends the appropriate 8-bit Data Byte (WD0) to be written.

Again the SX8650 Acknowledges [A].

In case the host needs to write more data, a succeeding 8-bit Data Byte will follow (WD1), acknowledged by the slave [A]. This sequence will be repeated until the host terminates the transfer with the Stop condition [P].




S: Start condition
SA: SX8650 Slave Address(7:1)
W: '0'
A: Acknowledge
CR: '000' + Register Address(4:0)
WDn: Write Data byte(7:0), 0...n
P: Stop condition

From host to SX8650
From SX8650 to host

*Figure 23. I2C write register*

The register address increments automatically when successive register data (WD1...WDn) is supplied by the host. This automatic increment can be used for the first 4 register addresses (see Table 6).

The correct sampling of the screen by the SX8650 and the host I2C bus traffic are events that might occur simultaneously. The SX8650 will synchronize these events by the use of clock stretching if that is required. The stretching occurs directly after the last received command bit (see Figure 23).

### 5.1.3. I2C Read Registers

The format for incremental I2C read for registers is given in Figure 24. The read has to start with a write of the read address.

After the start condition [S], the SX8650 Slave Address (SA) is sent, followed by an eighth bit (W='0') indicating a Write. The SX8650 then Acknowledges [A] that it is being addressed, and the host responds with a 8-bit CR Data consisting of '010' followed by the Register Address (RA). The SX8650 responds with an Acknowledge [A] and the host sends the Repeated Start Condition [Sr]. Once again, the SX8650 Slave Address (SA) is sent, followed by an eighth bit (R='1') indicating a Read.

The SX8650 responds with an Acknowledge [A] and the read Data byte (RD0). If the host needs to read more data it will acknowledge [A] and the SX8650 will send the next read byte (RD1). This sequence can be repeated until the host terminates with a NACK [N] followed by a stop [P].

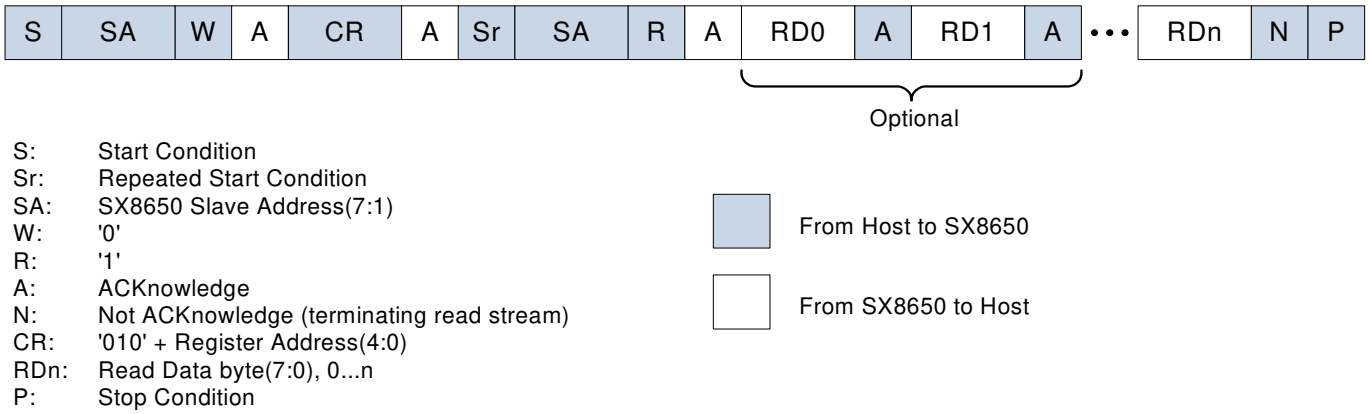



*Figure 24. I2C read registers*

The I2C read register format of Figure 24 is maintained until the Stop Condition. After the Stop Condition the SX8650 is performing succeeding reads by the compact read format of the I2C read channels described in the next section.

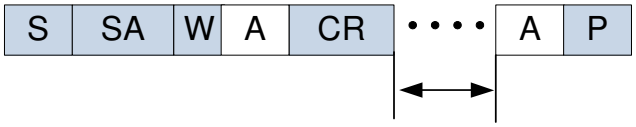
No clock stretching will occur for the I2C read registers.

### 5.1.4. I2C Host Commands

The format for I2C commands is given in Figure 25.

After the start condition [S], the SX8650 Slave Address (SA) is sent, followed by an eighth bit (W='0') indicating a Write. The SX8650 then Acknowledges [A] that it is being addressed, and the host responds with an 8-bit Data consisting of a '1' + command(6:0). The SX8650 Acknowledges [A] and the host sends a stop [P].

The exact definition of command(6:0) can be found in Table 8.




S: Start condition
SA: SX8650 Slave Address(7:1)
W: '0'
A: Acknowledge
CR: '1' + Command(6:0)
P: Stop condition

From host to SX8650
From SX8650 to host

*Figure 25. I2C host command*

The sampling of the screen by the SX8650 and the host I2C bus traffic are events that might occur simultaneously. The SX8650 will synchronize these events by the use of clock stretching if that is required. The stretching occurs directly after the last received command bit (see Figure 25).

### 5.1.5. I2C Read Channels

The host is able to read the channels with a high throughput, by the format shown in Figure 26.

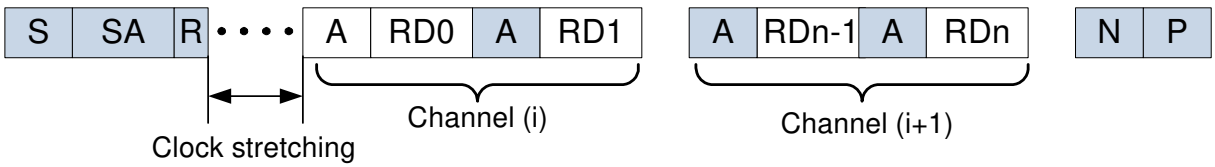
After the start condition [S], the SX8650 Slave Address (SA) is sent, followed by an eighth bit (R='1') indicating a read. The SX8650 responds with an Acknowledge [A] and the Read Data byte (RD0). The host sends an Acknowledge [A] and the SX8650 responds with the Read Data byte (RD1). If the host needs to read more data, it will acknowledge [A] and the SX8650 will send the next read bytes. This sequence can be repeated until the host terminates with a NACK [N] followed immediately by a stop [P]. The NACK [N] releases the NIRQ line. The stop [P] must occur before the end of the conversion.

The channel data that can be read is defined by the last conversion sequence.

A maximum number of 10 data bytes is passed when all channels (X, Y, z1, z2 and AUX) are activated in the "I2CRegChanMsk".

The channel data is sent with the following order: X, Y, Z1, Z2, AUX. The first byte of the data contains the channel information as shown in Figure 27.

Typical applications require only X and Y coordinates, thus only 4 bytes of data will be read.




S: Start condition
SA: SX8650 Slave Address(7:1)
R: '1'
A: Acknowledge
N: Not Acknowledge (terminating read stream)
RDn: Read Data byte(7:0), 0...n
P: Stop condition

From host to SX8650
From SX8650 to host

*Figure 26. I2C read channels*

The sampling of the screen by the SX8650 and the host I2C bus traffic are events that might occur simultaneously. The SX8650 will synchronize these events by the use of clock stretching if that is required. The stretching occurs directly after the address and read bit have been sent for the I2C read channels command (see Figure 26).

### 5.1.6. Data Channel Format

Channel data is coded on 16 bits as shown in Figure 27

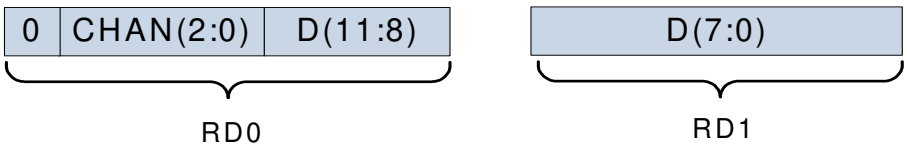



*Figure 27. data channel format*

The 3 bits CHAN(2:0) are defined in Table 9 and show which channel data is referenced. The channel data D(11:0) is of unsigned format and corresponds to a value between 0 and 4095.

### 5.1.7. Invalid Qualified Data

The SX8650 will return 0xFFFF data in case of invalid qualified data.

This occurs:

- when the SX8650 converted channels and the host channel readings do not correspond. E.g. the host converts X and Y and the host tries to read X, Y and z1 and z2.
- when a conversion is done without a pen being detected.

## 5.2. I2C Register Map

| I2C register address RA(4:0) | Register | Description |
|---|---|---|
| 0 0000 | I2CRegCtrl0 | Write, Read |
| 0 0001 | I2CRegCtrl1 | Write, Read |
| 0 0010 | I2CRegCtrl2 | Write, Read |
| 0 0100 | I2CRegChanMsk | Write, Read |
| 0 0101 | I2CRegStat | Read |
| 1 1111 | I2CRegSoftReset | Write |

*Table 5. I2C Register address*

The details of the registers are described in the next sections.

## 5.3. Host Control Writing

The host control writing allows the host to change SX8650 settings. The control data goes from the host towards the SX8650 and may be read back for verification.

| register | bits | default | description | | |
|---|---|---|---|---|---|
| I2CRegCtrl0 | 7:4 | 0000 | RATE | Set rate in coordinates per sec (cps) (± 20%)<br>If RATE equals zero then Manual mode.<br>if RATE is larger than zero then Automatic mode | |
| | | | | 0000: Timer disabled -Manual mode<br>0001: 10 cps<br>0010: 20 cps<br>0011: 40 cps<br>0100: 60 cps<br>0101: 80 cps<br>0110: 100 cps<br>0111: 200 cps | 1000: 300 cps<br>1001: 400 cps<br>1010: 500 cps<br>1011: 1k cps<br>1100: 2k cps<br>1101: 3k cps<br>1110: 4k cps<br>1111: 5k cps |
| | 3:0 | 0000 | POWDLY | Settling time (± 10%): The channel will be biased for a time of POWDLY before each channel conversion | |
| | | | | 0000: Immediate (0.5 us)<br>0001: 1.1 us<br>0010: 2.2 us<br>0011: 4.4 us<br>0100: 8.9 us<br>0101: 17.8 us<br>0110: 35.5 us<br>0111: 71.0 us | 1000: 0.14 ms<br>1001: 0.28 ms<br>1010: 0.57 ms<br>1011: 1.14 ms<br>1100: 2.27 ms<br>1101: 4.55 ms<br>1110: 9.09 ms<br>1111: 18.19 ms |
| I2CRegCtrl1 | 7:6 | 00 | AUXAQC | 00: AUX is used as an analog input<br>01: On rising AUX edge, wait POWDLY and start acquisition | 10: On falling AUX edge, wait POWDLY and start acquisition<br>11: On rising and falling AUX edges, wait POWDLY and start acquisition |
| | | | | The AUX trigger requires the manual mode. | |
| | 5 | 1 | CONDIRQ | Enable conditional interrupts<br>0: interrupt always generated at end of conversion cycle. If no pen is detected the data is set to 'invalid qualified'.<br>1: interrupt generated when pen detect is successful | |
| | 4 | 0 | reserved | | |
| | 3:2 | 00 | RPDNT | Select the Pen Detect Resistor<br>00: 100 KOhm<br>01: 200 KOhm<br>10: 50 KOhm<br>11: 25 KOhm | |
| | 1:0 | 00 | FILT | Digital filter control<br>00: Disable<br>01: 3 sample averaging<br>10: 5 sample averaging<br>11: 7 sample acquisition, sort, average 3 middle samples | |

*Table 6. I2C registers*

| register | bits | default | description | | |
|---|---|---|---|---|---|
| I2CRegCtrl2 | 7:4 | 0 | reserved | | |
| | 3:0 | 0000 | SETDLY | Settling time while filtering (± 10%)<br>When filtering is enabled, the channel will initially bias for a time of POWDLY for the first conversion, and for a time of SETDLY for each subsequent conversion in a filter set. | |
| | | | | 0000: Immediate (0.5 us)<br>0001: 1.1 us<br>0010: 2.2 us<br>0011: 4.4 us<br>0100: 8.9 us<br>0101: 17.8 us<br>0110: 35.5 us<br>0111: 71.0 us | 1000: 0.14 ms<br>1001: 0.28 ms<br>1010: 0.57 ms<br>1011: 1.14 ms<br>1100: 2.27 ms<br>1101: 4.55 ms<br>1110: 9.09 ms<br>1111: 18.19 ms |
| I2CRegChanMsk | 7 | 1 | XCONV | 0: no sample<br>1: sample, report X channel | |
| | 6 | 1 | YCONV | 0: no sample<br>1: sample, report Y channel | |
| | 5 | 0 | Z1CONV | 0: no sample<br>1: sample, report Z1 channel | |
| | 4 | 0 | Z2CONV | 0: no sample<br>1:sample, report Z2 channel | |
| | 3 | 0 | AUXCONV | 0: no sample<br>1: sample, report AUX channel | |
| | 0 | 0 | reserved | | |
| | 0 | 0 | reserved | | |
| | 0 | 0 | reserved | | |
| I2CRegStat | The host status reading allows the host to read the status of the SX8650. The data goes from the SX8650 towards the host. Host writing to this register is ignored. | | | | |
| | 7 | 0 | CONVIRQ | 0: no IRQ pending<br>1: End of conversion sequence IRQ pending<br>IRQ is cleared by the I2C channel reading | |
| | 6 | 0 | PENIRQ | operational in pen detect mode<br>0: no IRQ pending<br>1: Pen detected IRQ pending<br>IRQ is cleared by the I2C status reading | |
| | 5:0 | 000000 | reserved | | |
| I2CRegSoftReset | 7:0 | 0x00 | If the host writes the value 0xDE to this register, then the SX8650 will be reset.<br>Any other data will not affect the SX8650 | | |

*Table 6. I2C registers*