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Description

The SX8725 is a data acquisition system based on Semtech's low power ZoomingADC™ technology. It directly connects most types of miniature sensors with a general purpose microcontroller.

With 1 differential input, it can adapt to multiple sensor systems. Its digital outputs are used to bias or reset the sensing elements.

Applications

- Industrial pressure sensing
- Industrial temperature sensing
- Barometer
- Compass

Features

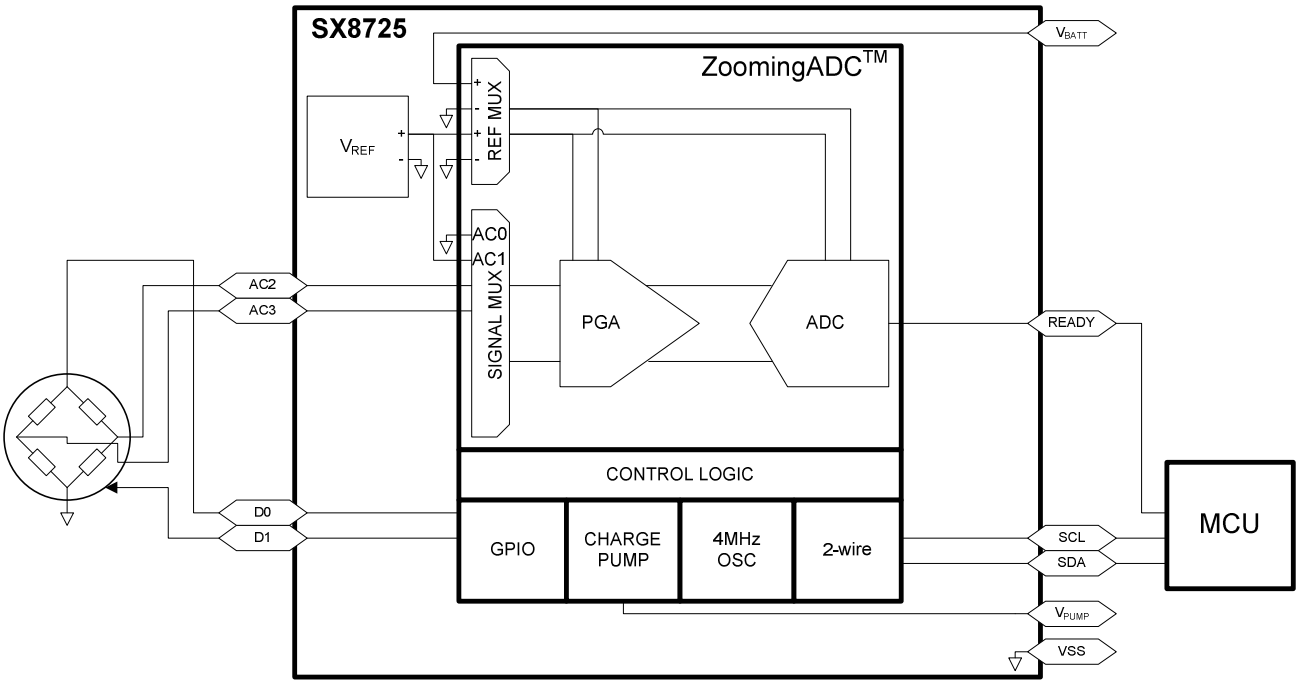
- Up to 16-bit differential data acquisition
- Programmable gain: (1/12 to 1000)
- Sensor offset compensation up to 15 times full scale of input signal
- 1 differential or 2 single-ended signal inputs
- Programmable Resolution versus Speed versus Supply current
- 2 digital outputs to bias Sensors
- Internal or external voltage reference
- Internal time base
- Low-power (250 uA for 16b @ 500 S/s)
- 2-WIRE interface

Ordering Information

Device	Package	Reel quantity
SX8725E083TRT	MLPD-W-12 4x4	3000
SX8725E083TDT	MLPD-W-12 4x4	1000

1) Available in tape and reel only
2) Lead free, WEEE and RoHS compliant.

Functional Block Diagram



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Absolute Maximum Ratings

Exceeding the specifications below may result in permanent damage to the device or device malfunction. Operation outside the parameters specified in the Electrical Characteristics section is not implied.

Parameter	Symbol	Comments / Conditions	Min	Max	Unit
Power supply	V_{BATT}		V_{SS} - 0.3	5.7	V
Storage temperature	T_{STORE}		-55	150	℃
Temperature under bias	T_{BIAS}		-40	140	℃
Max sensor common mode	V_{VR_P}		V_{SS} - 300	V_{BATT} + 300	mV
	V_{VR_N}				
Input voltage			V_{SS} - 300	V_{BATT} + 300	mV
Peak reflow temperature	T_{PKG}			260	℃

Notes: This device is ESD sensitive. Use of standard ESD handling precautions is required.

Electrical Characteristics

All values are valid within the operating conditions unless otherwise specified.

Parameter	Symbol	Comments / Conditions	Min	Typ	Max	Unit
Operating conditions						
Power supply	V_{BATT}		2.4		5.5	V
Operating temperature	T_{OP}		-40		125	°C
Current consumption						
Active current, @ 30 °C, 5.5 V	I_{OP}	16 b @ 250 Sample/s ADC, f_s = 125 kHz		250	300	µA
		16 b @ 1 kSample/s PGA3 + ADC, f_s= 500 kHz		700	800	
		16 b + gain 1000 @ 1 kSample/s PGA3,2,1 + ADC, f_s = 500kHz		1000	1200	
Active current, @ 30 °C, 3.3 V	I_{OP}	16 b @ 250 Sample/s PGA3 + ADC, f_s = 125 kHz		150		µA
		16 b @ 1 kSample/s PGA3 + ADC, f_s= 500 kHz		300		
		16 b + gain 1000 @ 1 kSample/s PGA3,2,1 + ADC, f_s = 500kHz		850		
Sleep current	I_{sleep}	@ 30 °C		75	200	nA
		up to 85 °C		100		
		@125 °C		150		
Time base						
Max ADC over-sampling frequency	F_{Smax}	@ 25 °C	450	500	550	kHz
Min ADC over-sampling frequency	F_{Smin}	@ 25 °C	56.25	62.5	68.75	kHz
Digital I/O						
Input logic high	V_{IH}		0.7			V_{BATT}
Input logic low	V_{IL}				0.3	V_{BATT}
Output logic high	V_{OH}	I_{OH} < 4mA			V_{BATT}-0.4	V
Output logic low	V_{OL}	I_{OL} < 4mA	0.4			V
VREF: Internal Bandgap Reference						
Absolute output voltage		V_{BATT} > 3V	1.19	1.22	1.25	V
Variation over Temperature		V_{BATT} > 3V, ref to 25°C	-1		+1	%
Total Output Noise		V_{BATT} > 3V, rms, broadband			1	mV

ZoomingADC Specifications

Unless otherwise specified: Temperature T_A = +25° C, V_{DD} = +5V, GND = 0V, $V_{REF,\ ADC}$ = +5V, V_{IN} = 0V, over-sampling frequency f_S = 250 kHz, *PGA3 on with Gain = 1, PGA1&PGA2 off*, offsets $GDOff_2$ = $GDOff_3$ = 0. Power operation: normal (IB_AMP_ADC[1:0] = IB_AMP_PGA[1:0] = '01'). For resolution *n* = 12 bits: *OSR* = 32 and N_{ELCONV} = 4. For resolution *n* = 16 bits: *OSR* = 512 and N_{ELCONV} = 2. Bandgap chopped at N_{ELCONV} rate.

Parameter	Symbol	Comments / Conditions	Min	Typ	Max	Unit
Analog Input						
Differential Input Voltage Ranges $V_{IN} = (V_{INP} - V_{INN})$		Gain = 1, *OSR* = 32 (Note 1)	-2.42		2.42	V
		Gain = 100, *OSR* = 32	-24.2		24.2	mV
		Gain = 1000, *OSR* = 32	-2.42		2.42	mV
Reference Voltage Range $V_{REF,\ ADC} = (V_{REFP} - V_{REFN})$					V_{DD}	V
Programmable Gain Amplifier (PGA)						
Total PGA Gain	GD_{TOT}	(Note 1)	1/12		1000	V/V
PGA1 Gain	GD_1	See Table 5	1		10	V/V
PGA2 Gain	GD_2	See Table 6	1		10	V/V
PGA3 Gain	GD_3	Step = 1/12 V/V, See Table 8	0		127/12	V/V
Gain Setting Precision (each stage)			-3	±0.5	3	%
Gain Temperature Dependence				±5		ppm/°C
PGA2 Offset	$GDoff_2$	Step = 0.2 V/V, See Table 7	-1		1	V/V
PGA3 Offset	$GDoff_3$	Step = 1/12 V/V, See Table 9	-63/12		63/12	V/V
Offset Setting Precision (PGA2 or 3)		(Note 2)	-3	±0.5	3	%
Offset Temperature Dependence				±5		ppm/°C
Input Impedance PGA1		Gain = 1 (Note 3)	1500			kΩ
		Gain = 10 (Note 3)	150			kΩ
Input Impedance PGA2, PGA3		Maximal gain (Note 3)	150			kΩ
Output RMS noise		PGA1 (Note 4)		205		µV
		PGA2 (Note 5)		340		µV
		PGA3 (Note 6)		365		µV
ADC Static Performance						
Resolution, n		(Note 7)	6		16	Bits
No Missing Codes		(Note 8)			16	Bits
Gain Error		(Note 9)		±0.15		%
Offset Error		n = 16 bits (Note 10)		±1		%
				±1		LSB
Integral Non-Linearity, INL		n = 12 Bits (Note 11)		±0.6		LSB
		n = 16 Bits (Note 11)		±1.5		LSB
Differential Non-Linearity, DNL		n = 12 Bits (Note 12)		±0.5		LSB
		n = 16 Bits (Note 12)		±0.5		LSB
Common Mode input range			V_{SS}-0.3		V_{BATT}+0.3	V
Power Supply Rejection Ratio	PSRR	VDD = 5V ± 0.3V (Note 13)		78		dB
		VDD = 3V ± 0.3V (Note 13)		72		dB
ADC Dynamic Performance						
Conversion Time	T_{CONV}	n = 12 bits (Note 14)	133			cycles/f_S
		n = 16 bits (Note 14)	1027			cycles/f_S
Throughput Rate (Continuous Mode)	$1/T_{CONV}$	n = 12 bits, f_S = 250kHz		1.88		kSps
		n = 16 bits, f_S = 250kHz		0.485		kSps
Nbr of Initialization Cycles	N_{INIT}		0		2	cycles

Parameter	Symbol	Comments / Conditions	Min	Typ	Max	Unit
Nbr of End Conversion Cycles	N_{END}		0		5	cycles
PGA Stabilization Delay		(Note 15)		OSR		cycles
ADC Digital Output						
Output Data Coding		Binary Two's Complement See Table 15 and Table 16				
Power Supply						
Voltage Supply Range	V_{DD}		2.4	5	5.5	V
Analog Quiescent Current		Only ZoomingADC				
Total Consumption	I_Q	V_{DD} = 5V/3V		800/675		µA
ADC Only Consumption		V_{DD} = 5V/3V		260/190		µA
PGA1 Consumption		V_{DD} = 5V/3V		190/170		µA
PGA2 Consumption		V_{DD} = 5V/3V		150/135		µA
PGA3 Consumption		V_{DD} = 5V/3V		200/180		µA
Analog Power Dissipation		All PGAs & ADC Active				
Normal Power Mode		V_{DD} = 5V/3V (Note 16)		4.0/2.0		mW
3/4 Power Reduction Mode		V_{DD} = 5V/3V (Note 17)		3.2/1.6		mW
1/2 Power Reduction Mode		V_{DD} = 5V/3V (Note 18)		2.4/1.1		mW
1/4 Power Reduction Mode		V_{DD} = 5V/3V (Note 19)		1.5/0.7		mW
Temperature						
Operating Range			-40		125	℃

Notes:

(1) Gain defined as overall PGA gain $GD_{TOT} = GD_1 \cdot GD_2 \cdot GD_3$. Maximum input voltage is given by: $V_{IN,\,MAX} = \pm(V_{REF,ADC}/2) \cdot (OSR/OSR+1)$.
(2) Offset due to tolerance on $GDoff_2$ or $GDoff_3$ setting. For small intrinsic offset, use only ADC and PGA1.
(3) Measured with block connected to inputs through AMUX block. Normalized input sampling frequency for input impedance is f_S = 500kHz. This figure must be multiplied by 2 for f_S = 250kHz, 4 for f_S = 125kHz. Input impedance is proportional to 1/ f_S.
(4) Figure independent on PGA1 gain and sampling frequency f_S.
(5) Figure independent on PGA2 gain and sampling frequency f_S.
(6) Figure independent on PGA3 gain and sampling frequency f_S.
(7) Resolution is given by n = 2·log2(*OSR*) + log2(N_{ELCONV}). *OSR* can be set between 8 and 1024, in powers of 2. N_{ELCONV} can be set to 1, 2, 4 or 8.
(8) If a ramp signal is applied to the input, all digital codes appear in the resulting ADC output data.
(9) Gain error is defined as the amount of deviation between the ideal (theoretical) transfer function and the measured transfer function (with the offset error removed).
(10) Offset error is defined as the output code error for a zero volt input (ideally, output code = 0). For ± 1 LSB offset, N_{ELCONV} must be ≥2.
(11) INL defined as the deviation of the DC transfer curve of each individual code from the best-fit straight line. This specification holds over the full scale. (For 16 bits INL set PGA3 on).
(12) DNL is defined as the difference (in LSB) between the ideal (1 LSB) and measured code transitions for successive codes.
(13) Figures for Gains = 1 to 100. PSRR is defined as the amount of change in the ADC output value as the power supply voltage changes.
(14) Conversion time is given by: $T_{CONV} = (N_{ELCONV} \cdot (OSR + 1) + 1) / f_S$. *OSR* can be set between 8 and 1024, in powers of 2. N_{ELCONV} can be set to 1, 2, 4 or 8.
(15) PGAs are reset after each writing operation to registers **RegACCfg1-5**. The ADC must be started after a PGA or inputs common-mode stabilization delay. This is done by writing bit Start several cycles after PGA settings modification or channel switching. Delay between PGA start or input channel switching and ADC start should be equivalent to *OSR* (between 8 and 1024) number of cycles. This delay does not apply to conversions made without the PGAs.
(16) Nominal (maximum) bias currents in PGAs and ADC, i.e. IB_AMP_PGA[1:0] = '11' and IB_AMP_ADC[1:0] = '11'.
(17) Bias currents in PGAs and ADC set to 3/4 of nominal values, i.e. IB_AMP_PGA[1:0] = '10', IB_AMP_ADC[1:0] = '10'.
(18) Bias currents in PGAs and ADC set to 1/2 of nominal values, i.e. IB_AMP_PGA[1:0] = '01', IB_AMP_ADC[1:0] = '01'.
(19) Bias currents in PGAs and ADC set to 1/4 of nominal values, i.e. IB_AMP_PGA[1:0] = '00', IB_AMP_ADC[1:0] = '00'.

Timing Characteristics

Parameter	Symbol	Comments / Conditions	Min	Typ	Max	Unit
Interrupt (Ready) timing specification						
READY pulse width (2)	t_{IRQ}			1		$1/F_S$
2-WIRE timing specifications(1)						
SCL clock frequency	f_{SCL}		0		400	kHz
SCL low period	t_{LOW}		1.3			µs
SCL high period	t_{HIGH}		0.6			µs
Data setup time	$t_{SU;DAT}$		100			ns
Data hold time	$t_{HD;DAT}$		0			ns
Repeated start setup time	$t_{SU;STA}$		0.6			µs
Start condition hold time	$t_{HD;STA}$		0.6			µs
Stop condition hold time	$t_{SU;STO}$		0.6			µs
Bus free time between stop and start	t_{BUF}		1.3			µs
Input glitch suppression	t_{SP}		50			ns

Notes:
(1) All timing specifications are referred to VILmin and VIHmax voltage levels defined for the SCL and SDA pins.
(2) The READY pulse indicates End of Conversion. This is a Low going pulse of duration equal to one cycle of the ADC sampling rate.

2-WIRE Timing Waveforms

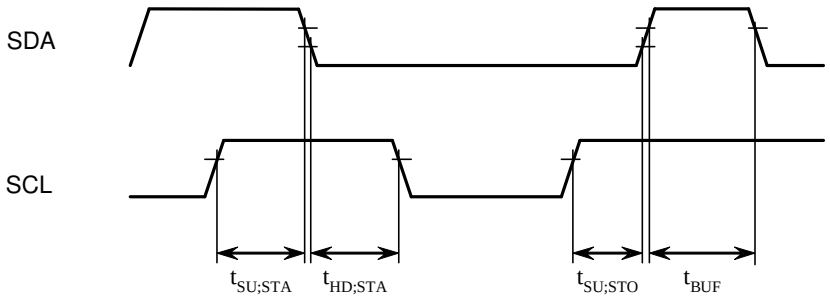


Figure 1 - 2-WIRE Start and Stop timings

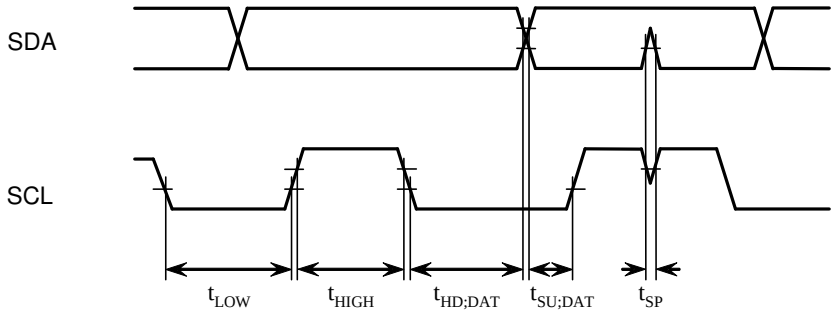
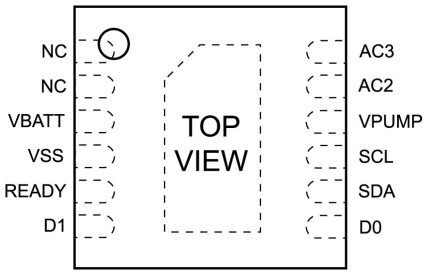


Figure 2 - 2-WIRE Data timings

Pin Configuration



Marking Information

yyww = Date code
xxxx = Semtech lot number

Pin Description

Pin	Name	Type	Function
1	NC	-	Not Connected
2	NC	-	Not Connected
3	V_{BATT}	Power Input	2.4V to 5.5V power supply
4	V_{SS}	Power Input	Chip Ground
5	READY	Digital Output	Conversion complete flag.
6	D_1	Digital IO + analog	Digital output sensor drive (V_{BATT} or V_{SS})
			V_{REF} Input in optional operating mode
7	D_0	Digital IO + analog	Digital output sensor drive (V_{BATT} or V_{SS})
			V_{REF} Output in optional operating mode
8	SDA	Digital IO	2-WIRE Data
9	SCL	Digital IO	2-WIRE Clock. Up to 400KHz.
10	V_{PUMP}	Power IO	Charge pump output. Raises ADC supply above V_{BATT} if V_{BATT} supply is too low. Recommended range for capacitor is 1nF to 10 nF. Connect the capacitor to GND.
11	AC_2	Analog Input	Differential sensor input in conjunction with AC_3
12	AC_3	Analog Input	Differential sensor input in conjunction with AC_2
13	V_{SS}	Power Input	Bottom ground pad (1)

Notes:
(1) This pin is internally connected to V_{SS}. It should also be connected to V_{SS} on PCB to reduce noise and improve thermal behavior.

Circuit Description

General Description

The SX8725 is a complete low-power acquisition path with programmable gain, acquisition speed and resolution.

Block Diagram

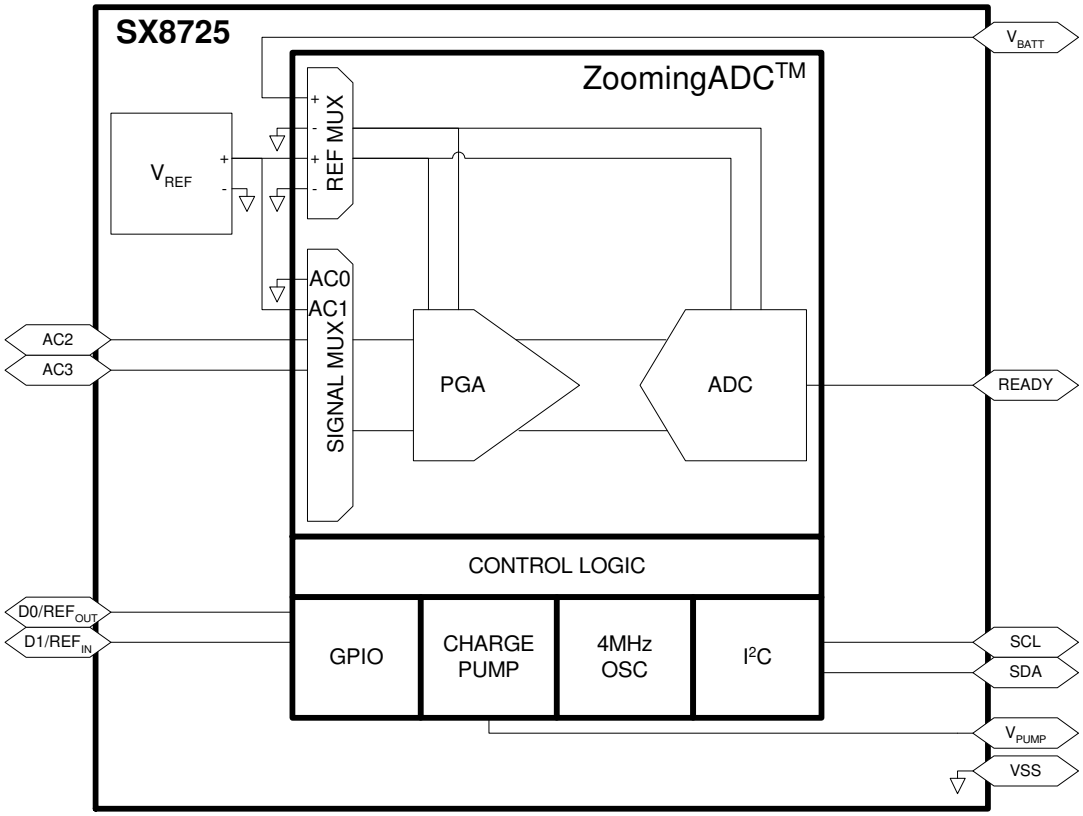


Figure 3 - SX8725 Block Diagram

VREF

The internally generated V_{REF} is a trimmed bandgap reference with a nominal value of 1.22V that provides a stable voltage reference for the ZoomingADC.

This reference voltage is directly connected to one of the ZoomingADC reference multiplexer inputs.

The bandgap voltage stability is only guaranteed for V_{BATT} voltages of 3V and above. As V_{BATT} drops down to 2.4V, the bandgap voltage could reduce by up to 50mV.

The bandgap has relatively weak output drive so it is recommended that if the bandgap is required as a signal input then PGA1 must be enabled with Gain = 1.

GPIO

The GPIO block is a multipurpose 4 bit input/output port. In addition to digital behavior, D0 and D1 pins can be programmed as analog pins in order to be used as output (reference voltage monitoring) and input for an external reference voltage (For further details see Figure 14, Figure 15, Figure 16 and Figure 17). Each port terminal can be individually selected as digital input or output.

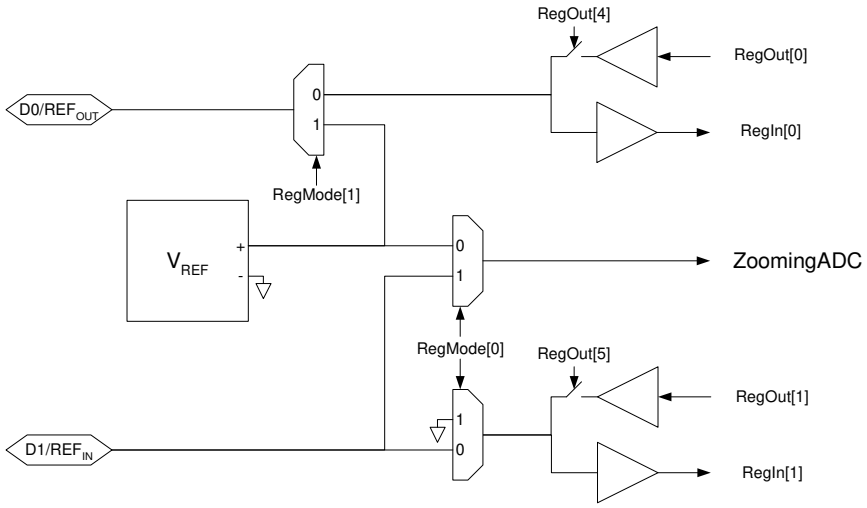


Figure 4 - GPIO Block Diagram

The direction of each bit within the GPIO block (input only or input/output) can be individually set using the 4th and 5th bits of the **RegOut** register. If D[x]_DIR = 1, both the input and output buffer are active on the corresponding GPIO block pin. If D[x]_DIR = 0, the corresponding GPIO block pin is an input only and the output buffer is in high impedance. After power on reset the GPIO block pins are in input/output mode (D[x]_DIR are reset to 1)

The input values of GPIO block are available in **RegIn** register (read only). Reading is always direct – there is no debounce function in the GPIO block. In case of possible noise on input signals, an external hardware filter has to be realized. The input buffer is also active when the GPIO block is defined as output and the effective value on the pin can be read back.

Data stored in the 1st and 2nd bits of **RegOut** register are outputted at GPIO block if D[x]_DIR = 1. The default values after power on reset is low (0).

The digital pins are able to deliver a driving current up to 8 mA.

When the bits VREF_D0_OUT and VREF_D1_IN in the **RegMode** register are set to 1 the D0 and D1 pins digital behavior are automatically bypassed in order to either input or output the voltage reference signals.

Charge Pump

This block generates a supply voltage able to power the analog switch drive levels on the chip.

The minimum acceptable switch supply is 3V which means that if V_{BATT} drops below 3V then the block should be activated to generate a voltage of 3V or above. If V_{BATT} is greater than 3V then V_{BATT} may be switched straight through to the V_{PUMP} output.

If control input bit MULT_FORCE_OFF = 1 in **RegMode** register then the charge pump is disabled and V_{BATT} is permanently connected to V_{PUMP}.

If control input bit MULT_FORCE_ON = 1 in **RegMode** register then the charge pump is permanently enabled. This overrides MULT_FORCE_OFF bit in **RegMode** register.

If MULT_FORCE_ON = 0 and MULT_FORCE_OFF = 0 bits in **RegMode** register then the charge pump will start if V_{BATT} drops below 3V, otherwise V_{BATT} will be switched directly through to V_{PUMP}.

These controls are supplied to give the user the option of fixing the charge pump state to avoid it turning off and on when V_{BATT} is close to 3V.

The cell will use the on-chip bandgap reference and comparator to detect when V_{BATT} is too low. When activated, the block will use the charge pump to boost the V_{BATT} voltage to above 3V but with diode limiting to ensure that the generated voltage never exceeds 0.7V above V_{BATT}.

An external capacitor is required on V_{PUMP} whenever the power supply is supposed to be less or drop below 3V. This capacitor should be large enough to ensure that generated voltage is smooth enough to avoid affecting conversion accuracy but not so large that it gives an unacceptable settling time. A recommended value is around 2.2nF.

The block will also indicate when the pumped output voltage is sufficiently high to allow ADC conversions to be started. This will be a simple comparison which will give a ready signal when the V_{PUMP} output is 3V or above.

RC Oscillator

This block provides the master clock reference for the chip. It produces a clock at 4 MHz which is divided internally in order to generate the clock sources needed by the other blocks.

The oscillator technique is a low power relaxation design and it is designed to vary as little as possible over temperature and supply voltage.

This oscillator is trimmed at manufacture chip test.

The RC oscillator will start up after a chip reset to allow the trimming values to be read and calibration registers and 2-WIRE address set to their programmed values. Once this has been done, the oscillator will be shut down and the chip will enter a sleep state while waiting for an 2-WIRE communication.

2-WIRE

The 2-WIRE interface gives access to the chip registers. It complies with the 2-WIRE protocol specifications, restricted to the slave side of the communication.

General features:

- Slave only operation
- Fast mode operation (up to 400 kHz)
- Combined read and write mode support
- General call reset support
- 7-bit device address customization
- Stretch 2-WIRE clock SCL only before sending ACK/NACK

The interface handles 2-WIRE communication at the transaction level: the processor is only aware of read and writes transactions. A read transaction is an external request to get the content of system memory location and a write transaction is an external request to write the content of a system memory location.

2-WIRE Communication Format

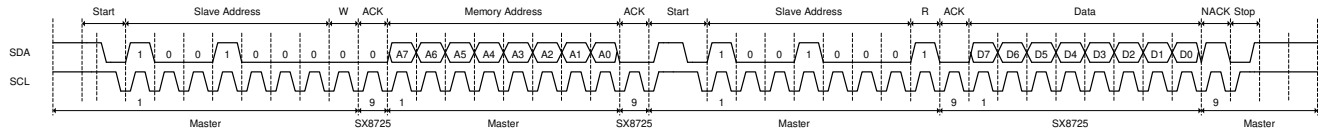


Figure 5 - Timing Diagram for Reading from SX8725

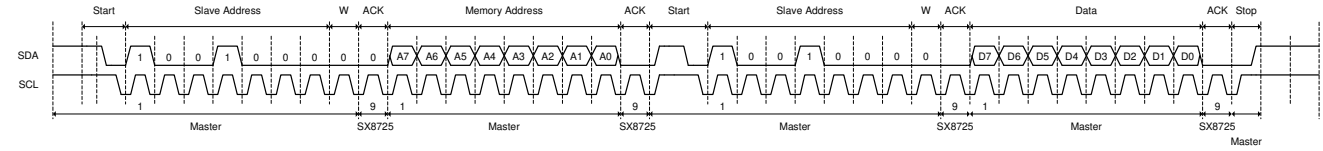


Figure 6 - Timing Diagram for Writing to the SX8725

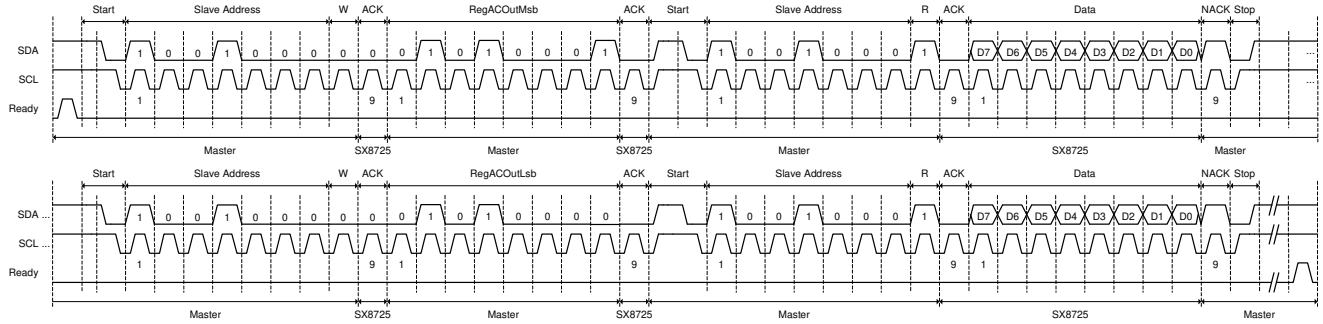


Figure 7 - Timing Diagram for Reading an ADC Sample from SX8725

2-WIRE Address

The default 2-WIRE slave address is 1001000 in binary.
This is the standard part 2-WIRE slave address. Other addresses between 1001001 and 1001111 are available by special request.

ZoomingADC

Features

The ZoomingADC is a complete and versatile low-power analog front-end interface typically intended for sensing applications.
In the following text the ZoomingADC will be referred as ZADC.

The key features of the ZADC are:

- Programmable 6 to 16-bit dynamic range over-sampled ADC
- Flexible gain programming between 0.5 and 1000
- Flexible and large range offset compensation
- 2-channel differential or 3-channel single-ended input
- 2-channel differential reference inputs
- Power saving modes

Overview

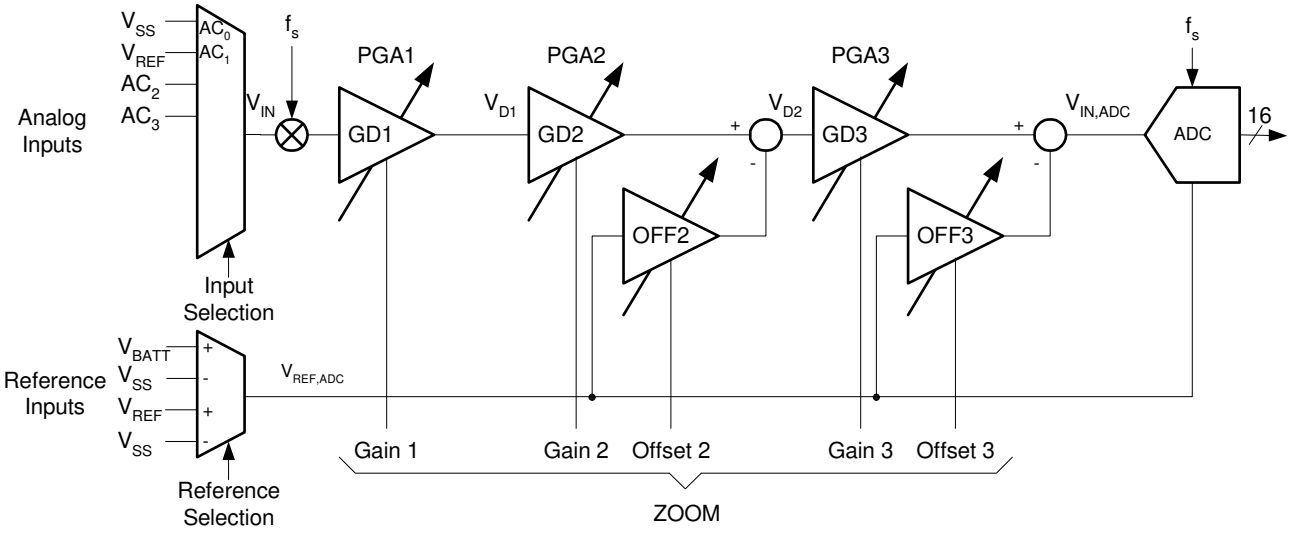


Figure 8 - ZADC General Functional Block Diagram

The total acquisition chain consists of an input multiplexer, 3 programmable gain amplifier stages and an over sampled A/D converter. The reference voltage can be selected on two different channels. Two offset compensation amplifiers allow for a wide offset compensation range. The programmable gain and offset allow the application to zoom in on a small portion of the reference voltage defined input range.

ZADC Description

Acquisition Chain

Figure 8 shows the general block diagram of the acquisition chain (AC). A control block (not shown in Figure 8) manages all communications with the 2-WIRE peripheral. The clocking is derived from the internal 4 MHz Oscillator.

Analog inputs can be selected through a 4 input multiplexer, while reference input is selected between two differential channels. It should however be noted that only 3 acquisition channels (including the V_{REF}) are available when configured as single ended since the input amplifier is always operating in differential mode with both positive and negative input selected through the multiplexer.

The core of the zooming section is made of three differential programmable amplifiers (PGA). After selection of an input and reference signals V_{IN} and $V_{REF,ADC}$ combination, the input voltage is modulated and amplified through

stages 1 to 3. Fine gain programming up to 1'000 V/V is possible. In addition, the last two stages provide programmable offset. Each amplifier can be bypassed if needed.

The output of the PGA stages is directly fed to the analog-to-digital converter (ADC), which converts the signal $V_{IN,ADC}$ into digital.

Like most ADCs intended for instrumentation or sensing applications, the ZoomingADC is an over-sampled converter (See Note[1]). The ADC is a so-called incremental converter; with bipolar operation (the ADC accepts both positive and negative differential input voltages). In first approximation, the ADC output result relative to full-scale (*FS*) delivers the quantity:

$$\frac{OUT_{ADC}}{F_S/2} \cong \frac{V_{IN,ADC}}{V_{REF,ADC}/2}$$

Equation 1

in two's complement (see Equation 4 and Equation 5 for details). The output code OUT_{ADC} is *-FS/2* to *+FS/2* for $V_{IN,ADC} \cong -V_{REF,ADC}/2$ to $+V_{REF,ADC}/2$ respectively. As will be shown, $V_{IN,ADC}$ is related to input voltage V_{IN} by the relationship:

$$V_{IN,ADC} = GD_{TOT} \cdot V_{IN} - GDoff_{TOT} \cdot V_{REF,ADC} \quad \text{(V)}$$

Equation 2

where GD_{TOT} is the total PGA gain, and $GDoff_{TOT}$ is the total PGA offset.

[1] Note: Over-sampled converters are operated with a sampling frequency f_S much higher than the input signal's Nyquist rate (typically f_S is 20-1'000 times the input signal bandwidth). The sampling frequency to throughput ratio is large (typically 10-500). These converters include digital decimation filtering. They are mainly used for high resolution, and/or low-to-medium speed applications.

Registers

The system has a bank of eight 8-bit registers: six registers are used to configure the acquisition chain (**RegAcCfg0** to **5**), and two registers are used to store the output code of the analog-to-digital conversion (**RegAcOutMsb** & **Lsb**).

Register Name	Bit Position							
	7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RegACOutLsb	OUT[7:0]							
RegACOutMsb	OUT[15:8]							
RegACCfg0 Default values:	START 0	SET_NELC[1:0] 01		SET_OSR[2:0] 010			CONT 0	- 0
RegACCfg1 Default values:	IB_AMP_ADC[1:0] 11		IB_AMP_PGA[1:0] 11		ENABLE[3:0] 0000			
RegACCfg2 Default values:	FIN[1:0] 00		PGA2_GAIN[1:0] 00		PGA2_OFFSET[3:0] 0000			
RegACCfg3 Default values:	PGA1_G 0	PGA3_GAIN[6:0] 0001100						
RegACCfg4 Default values:	- 0	PGA3_OFFSET[6:0] 0000000						
RegACCfg5 Default values:	BUSY 0	DEF 0	AMUX[4:0] 00000					VMUX 0

Table 1 - Peripheral Registers to Configure the Acquisition Chain (AC) and to Store the Analog-to-Digital Conversion (ADC) Result

With:

- OUT: (r) digital output code of the analog-to-digital converter. (MSB = OUT[15])
- START: (w) setting this bit triggers a single conversion (after the current one is finished). This bit always reads back 0.
- SET_NELC: (rw) sets the number of elementary conversions to 2 SET_NELC[1:0]. To compensate for offsets, the input signal is chopped between elementary conversions (1,2,4,8).
- SET_OSR: (rw) sets the over-sampling rate (OSR) of an elementary conversion to 2(3+SET_OSR[2:0]). OSR = 8, 16, 32, ..., 512, 1024.
- CONT: (rw) setting this bit starts a conversion. A new conversion will automatically begin as long as the bit remains at 1.
- TEST: bit only used for test purposes. In normal mode, this bit is forced to 0 and cannot be overwritten.
- IB_AMP_ADC: (rw) sets the bias current in the ADC to 0.25*(1+ IB_AMP_ADC[1:0]) of the normal operation current (25, 50, 75 or 100% of nominal current). To be used for low-power, low-speed operation.
- IB_AMP_PGA: (rw) sets the bias current in the PGAs to 0.25*(1+IB_AMP_PGA[1:0]) of the normal operation current (25, 50, 75 or 100% of nominal current). To be used for low-power, low-speed operation.
- ENABLE: (rw) enables the ADC modulator (bit 0) and the different stages of the PGAs (PGAi by bit i=1,2,3). PGA stages that are disabled are bypassed.
- FIN: (rw) These bits set the over sampling frequency of the acquisition chain. Expressed as a fraction of the oscillator frequency, the sampling frequency is given as: 11 → 500 kHz, 10 → 250 kHz, 01 → 125 kHz, 00 → 62.5 kHz.
- PGA1_GAIN: (rw) sets the gain of the first stage: 0 → 1, 1 → 10.
- PGA2_GAIN: (rw) sets the gain of the second stage: 00 → 1, 01 → 2, 10 → 5, 11 → 10.
- PGA3_GAIN: (rw) sets the gain of the third stage to PGA3_GAIN[6:0]·1/12.
- PGA2_OFFSET: (rw) sets the offset of the second stage between –1 and +1, with increments of 0.2. The MSB gives the sign (0 → positive, 1 → negative); amplitude is coded with the bits PGA2_OFFSET[5:0].
- PGA3_OFFSET: (rw) sets the offset of the third stage between –5.25 and +5.25, with increments of 1/12. The MSB gives the sign (0 → positive, 1 → negative); amplitude is coded with the bits PGA3_OFFSET[5:0].
- BUSY: (r) set to 1 if a conversion is running.
- DEF: (w) sets all values to their defaults (PGA disabled, max speed, nominal modulator bias current, 2 elementary conversions, over-sampling rate of 32) and starts a new conversion without waiting the end of the preceding one.
- AMUX(4:0): (rw) AMUX(4) sets the mode (0 → differential inputs, 1 → single ended inputs with A_0 = common reference) AMUX(3) sets the sign (0 → straight, 1→ cross) AMUX(2:0) sets the channel.
- VMUX: (rw) sets the differential reference channel (0 → V_{BATT}, 1 → V_{REF}).
  (r = read; w = write; rw = read & write)

ZADC Detailed Functionality Description

Continuous-Time vs. On-Request

The ADC can be operated in two distinct modes: "continuous-time" and "on-request" modes (selected using the bit CONT).

In "continuous-time" mode, the input signal is repeatedly converted into digital. After a conversion is finished, a new one is automatically initiated. The new value is then written in the result register, and the corresponding internal trigger pulse is generated. This operation is sketched in Figure 9. The conversion time in this case is defined as T_{CONV}.

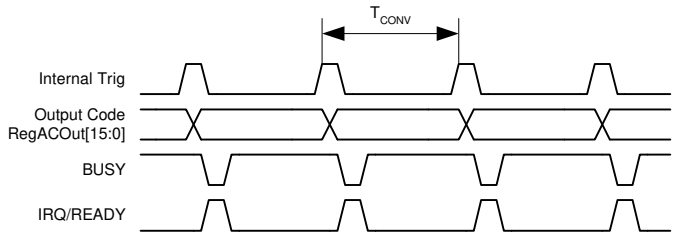


Figure 9 - ADC "Continuous-Time" Operation

In the "on-request" mode, the internal behavior of the converter is the same as in the "continuous-time" mode, but the conversion is initiated on user request (with the START bit). As shown in Figure 10, the conversion time is also T_{CONV}.

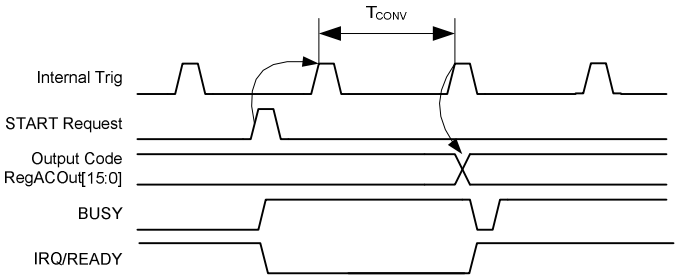


Figure 10 - ADC "On-Request" Operation

Input Multiplexers

The ZoomingADC has eight analog inputs AC_0 to AC_7 and four reference inputs AC_R_0 to AC_R_3. Let us first define the differential input voltage V_{IN} and reference voltage $V_{REF,ADC}$ respectively as:

$$V_{IN} = V_{INP} - V_{INN} \qquad (V)$$

Equation 3

and:

$$V_{REF,ADC} = V_{REFP} - V_{REFN} \qquad (V)$$

Equation 4

As shown in Table 2, the inputs can be configured in two ways: either as 4 differential channels ($V_{IN1} = AC_1 - AC_0$,..., $V_{IN3} = AC_5 - AC_4$), or AC_0 can be used as a common reference, providing 5 signal paths all referred to AC_0. The control word for the analog input selection is AMUX[4:0]. Notice that the bit AMUX[3] controls the sign of the input voltage.

AMUX[4:0] (RegACCfg5[5:1])	V_{INP}	V_{INN}
00x00	AC_1 (V_{REF})	AC_0 (V_{SS})
00x01	AC_3	AC_2
10000	AC_0 (V_{SS})	AC_0 (V_{SS})
10001	AC_1 (V_{REF})	
10010	AC_2	
10011	AC_3	

AMUX[4:0] (RegACCfg5[5:1])	V_{INP}	V_{INN}
01x00	AC_0 (V_{SS})	AC_1 (V_{REF})
01x01	AC_2	AC_3
11000	AC_0 (V_{SS})	AC_0 (V_{SS})
11001		AC_1 (V_{REF})
11010		AC_2
11011		AC_3

Table 2 - Analog Input Selection

Similarly, the reference voltage is chosen among two differential channels ($V_{REF,ADC}$ = AC_R_1 - AC_R_0 or $V_{REF,ADC}$ = AC_R_3 - AC_R_2) as shown in Table 3. The selection bit is VMUX. The reference inputs V_{REFP} and V_{REFN} (common-mode) can be up to the power supply range.

VMUX (RegACCfg5[0])	V_{REFP}	V_{REFN}
0	AC_R_1 (V_{BATT})	AC_R_0 (V_{SS})
1	AC_R_3 (V_{REF})	AC_R_2 (V_{SS})

Table 3 - Analog Reference Input Selection

Programmable Gain Amplifiers

As seen in Figure 8, the zooming function is implemented with three programmable gain amplifiers (PGA). These are:

- PGA1: coarse gain tuning
- PGA2: medium gain and offset tuning
- PGA3: fine gain and offset tuning. Should be set ON for high linearity data acquisition

All gain and offset settings are realized with ratios of capacitors. The user has control over each PGA activation and gain, as well as the offset of stages 2 and 3. These functions are examined hereafter.

ENABLE[3:0] (RegACCfg1[3:0])	Block
xxx0	ADC disabled
xxx1	ADC enabled
xx0x	PGA1 disabled
xx1x	PGA1 enabled
x0xx	PGA2 disabled
x1xx	PGA2 enabled
0xxx	PGA3 disabled
1xxx	PGA3 enabled

Table 4 - ADC & PGA Enabling

PGA1_GAIN (RegACCfg3[7])	PGA1 Gain GD_1 (V/V)
0	1
1	10

Table 5 - PGA1 Gain Settings

PGA2_GAIN[1:0] (RegACCfg2[5:4])	PGA2 Gain GD_2 (V/V)
00	1
01	2
10	5
11	10

Table 6 - PGA2 Gain Settings

PGA2_OFFSET[3:0] (RegACCfg2[3:0])	PGA2 Offset $GDoff_2$ (V/V)
0000	0
0001	+0.2
0010	+0.4
0011	+0.6
0100	+0.8
0101	+1
1001	-0.2
1010	-0.4
1011	-0.6
1100	-0.8
1101	-1

Table 7 - PGA2 Offset Settings

PGA3_GAIN[6:0] (RegACCfg3[6:0])	PGA3 Gain GD_3 (V/V)
0000000	0
0000001	1/12(=0.083)
...	...
0000110	6/12
...	...
0001100	12/12
0010000	16/12
...	
0100000	32/12
...	
1000000	64/12
...	
1111111	127/12(=10.58)

Table 8 - PGA3 Gain Settings

PGA3_OFFSET[6:0] (RegACCfg4[6:0])	PGA3 Offset $GDoff_3$ (V/V)
0000000	0
0000001	+1/12(=+0.083)
0000010	+2/12
...	...
0010000	+16/12
...	...
0100000	+32/12
...	...
0111111	+63/12(=+5.25)
1000000	0
1000001	-1/12(=-0.083)
1000010	-2/12
...	...
1010000	-16/12
...	...
1100000	-32/12
...	...
1111111	-63/12(=-5.25)

Table 9 - PGA3 Offset Settings

PGA & ADC Enabling

Depending on the application objectives, the user may enable or bypass each PGA stage. This is done according to the word ENABLE and the coding given in Table 4. To reduce power dissipation, the ADC can also be inactivated while idle.

PGA1

The first stage can have a buffer function (unity gain) or provide a gain of 10 (see Table 5). The voltage V_{D1} at the output of PGA1 is:

$$V_{D1} = GD_1 \cdot V_{IN} \quad \text{(V)}$$

Equation 5

where GD_1 is the gain of PGA1 (in V/V) controlled with the bit PGA1_GAIN.

PGA2

The second PGA has a finer gain and offset tuning capability, as shown in Table 6 and Table 7. The voltage V_{D2} at the output of PGA2 is given by:

$$V_{D2} = GD_2 \cdot V_{D1} - GDoff_2 \cdot V_{REF,ADC} \quad \text{(V)}$$

Equation 6

where GD_2 and $GDoff_2$ are respectively the gain and offset of PGA2 (in V/V). These are controlled with the words PGA2_GAIN[1:0] and PGA2_OFFSET[3:0].

PGA3

The finest gain and offset tuning is performed with the third and last PGA stage, according to the coding of Table 8 and Table 9. The output of PGA3 is also the input of the ADC. Thus, similarly to PGA2, we find that the voltage entering the ADC is given by:

$$V_{IN,ADC} = GD_3 \cdot V_{D2} - GDoff_3 \cdot V_{REF,ADC} \quad \text{(V)}$$

Equation 7

where GD_3 and $GDoff_3$ are respectively the gain and offset of PGA3 (in V/V). The control words are PGA3_GAIN[6:0] and PGA3_OFFSET[6:0]. To remain within the signal compliance of the PGA stages, the condition:

$$V_{D1}, V_{D2} < V_{DD} \quad \text{(V)}$$

Equation 8

must be verified.

Finally, combining equations 5 to 7 for the three PGA stages, the input voltage $V_{IN,ADC}$ of the ADC is related to V_{IN} by:

$$V_{IN,ADC} = GD_{TOT} \cdot V_{IN} - GDoff_{TOT} \cdot V_{REF,ADC} \quad \text{(V)}$$

Equation 9

where the total PGA gain is defined as:

$$GD_{TOT} = GD_3 \cdot GD_2 \cdot GD_1 \quad \text{(V/V)}$$

Equation 10

and the total PGA offset is:

$$GDoff_{TOT} = GDoff_3 + GD_3 \cdot GDoff_2 \quad \text{(V/V)}$$

Equation 11

ADC Characteristics

The main performance characteristics of the ADC (resolution, conversion time, etc.) are determined by three programmable parameters. The setting of these parameters and the resulting performances are described later.

- Over-sampling frequency f_s
- Over-Sampling Ratio OSR
- Number of Elementary Conversions NELCONV

Conversion Sequence

A conversion is started each time the bit START or the bit DEF is set. As depicted in Figure 11, a complete analog-to-digital conversion sequence is made of a set of N_{ELCONV} elementary incremental conversions and a final quantization step. Each elementary conversion is made of (OSR+1) over-sampling periods $T_s=1/f_s$, i.e.:

$$T_{ELCONV} = \frac{(OSR+1)}{fs} \quad \text{(s)}$$

Equation 12

The result is the mean of the elementary conversion results. An important feature is that the elementary conversions are alternatively performed with the offset of the internal amplifiers contributing in one direction and the other to the output code. Thus, converter internal offset is eliminated if at least two elementary sequences are performed (i.e. if $N_{ELCONV} \geq 2$). A few additional clock cycles are also required to initiate and end the conversion properly.

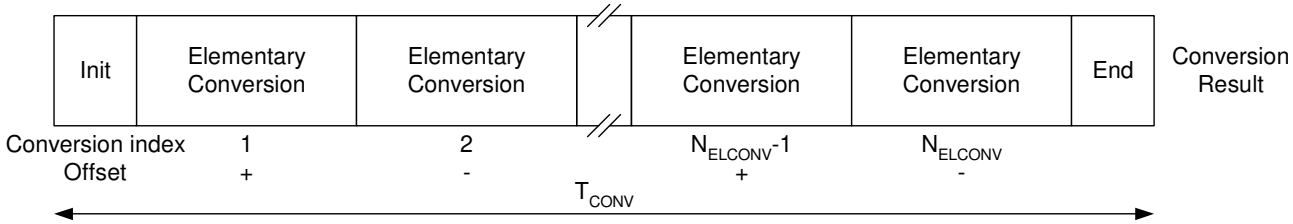


Figure 11 - Analog-to-Digital Conversion Sequence

Note:
The internal bandgap reference state may be forced High or Low, or may be set to toggle during conversion at either the same rate or half the rate of the Elementary Conversion. This may be useful to help eliminate bandgap related internal offset voltage and $1/f_s$ noise.

Over-Sampling Frequency

The word FIN[1:0] (see Table 10) is used to select the over-sampling frequency f_s. The over-sampling frequency is derived from the 4MHz oscillator clock.

FIN[1:0] (RegACCfg2[7:6])	Over-Sampling Frequency f_s (Hz)
00	62.5 kHz
01	125 kHz
10	250 kHz
11	500 kHz

Table 10 - Over-Sampling Frequency Settings

Over-Sampling Ratio

The over-sampling ratio (*OSR*) defines the number of integration cycles per elementary conversion. Its value is set with the word SET_OSR[2:0] in power of 2 steps (see Table 11) given by:

$$OSR = 2^{3+SET\_OSR[2:0]}$$

Equation 13

SET_OSR[2:0] (RegACCfg0[4:2])	Over-Sampling Ratio *OSR* (-)
000	8
001	16
010	32
011	64
100	128
101	256
110	512
111	1024

Table 11 - Over-Sampling Ratio Settings

Elementary Conversions

As mentioned previously, the whole conversion sequence is made of a set of N_{ELCONV} elementary incremental conversions. This number is set with the word SET_NELC[1:0] in power of 2 steps (see Table 12) given by:

$$N_{ELCONV} = 2^{SET\_NELC[1:0]}$$

Equation 14

SET_NELC[1:0] (RegACCfg0[6:5])	# of Elementary Conversions N_{ELCONV} (-)
00	1
01	2
10	4
11	8

Table 12 - Number of Elementary Conversion Settings

As already mentioned, N_{ELCONV} must be equal or greater than 2 to reduce internal amplifier offsets.

Resolution

The theoretical resolution of the ADC, without considering thermal noise, is given by:

$$n = 2 \cdot \log_2(OSR) + \log_2(N_{ELCONV}) \quad \text{(Bits)}$$

Equation 15

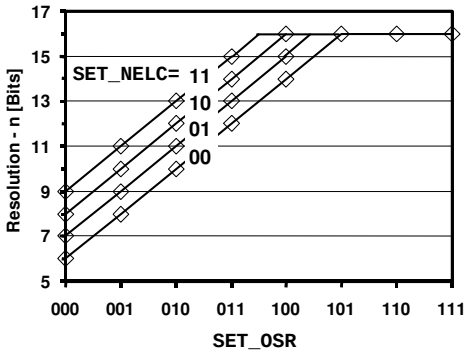


Figure 12 - Resolution vs. SET_OSR[2:0] and SET_NELC[1:0]

Using look-up Table 13 or the graph plotted in Figure 12, resolution can be set between 6 and 16 bits. Notice that, because of 16-bit register use for the ADC output, **practically the resolution is limited to 16 bits**, i.e. n ≤ 16. Even though the resolution is truncated to 16 bit by the output register size, it may make sense to set OSR and N_{ELCONV} to higher values in order to reduce the influence of the thermal noise in the PGA and of external noises (see section “PGA Gain & Offset, Linearity and Noise” in page 37).

SET_OSR [2:0]	SET_NELC[1:0]			
	00	01	10	11
000	6	7	8	9
001	8	9	10	11
010	10	11	12	13
011	12	13	14	15
100	14	15	16	16
101	16	16	16	16
110	16	16	16	16
111	16	16	16	16

Note: shaded area: resolution truncated to 16 bits due to output register size **RegACOut**[15:0]

Table 13 - Resolution vs. SET_OSR[2:0] and SET_NELC[1:0] Settings

Conversion Time and Throughput

As explained in Figure 12, conversion time is given by:

$$T_{CONV} = \frac{N_{ELCONV} \cdot (OSR+1)+1}{f_s} \quad \text{(s)}$$

Equation 16

and throughput is then simply $1/T_{CONV}$. For example, consider an over-sampling ratio of 256, 2 elementary conversions, and a over-sampling frequency of 500kHz (SET_OSR = "101", SET_NELC = "01", FIN = "00"). In this case, using Table 14, the conversion time is 515 over-sampling periods, or 1.03ms. This corresponds to a throughput of 971Hz in continuous-time mode. The plot of Figure 7 illustrates the classic trade-off between resolution and conversion time.

SET_OSR [2:0]	SET_NELC[1:0]			
	00	01	10	11
000	10	19	37	73
001	18	35	69	137
010	34	67	133	265
011	66	131	261	521
100	130	259	517	1033
101	258	515	1029	2057
110	514	1027	2053	4105
111	1026	2051	4101	8201

Table 14 - Normalized Conversion Time (T_{CONV}*f_s) vs. SET_OSR[2:0] and SET_NELC[1:0] (Normalized to Over-Sampling Period 1/f_s)

Note
Some high sample rate configurations can not be used due to 2-WIRE speed limitation.

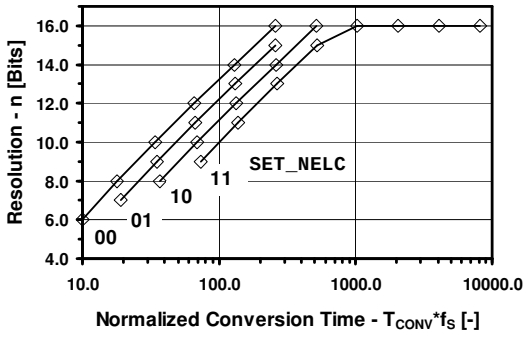


Figure 13 - Resolution vs. Normalized Conversion Time for Different SET_NELC[1:0]