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Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
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DESCRIPTION

The SX8725S is a data acquisition system based on Semtech's low power ZoomingADC™ technology. It directly connects most types of miniature sensors with a general purpose microcontroller.

With 1 differential input, it can adapt to multiple sensor systems. Its digital outputs are used to bias or reset the sensing elements.

FEATURES

- Up to 16-bit differential data acquisition
- Programmable gain: (1/12 to 1000)
- Sensor offset compensation up to 15 times full scale of input signal
- 1 differential or 2 single-ended signal inputs
- Programmable Resolution versus Speed versus Supply current
- Digital outputs to bias Sensors
- Internal or external voltage reference
- Internal time base
- Low-power (250 uA for 16b @ 250 S/s)
- SPI interface, 2 Mbps serial clock

APPLICATIONS

- Industrial pressure sensing
- Industrial temperature sensing
- Industrial chemical sensing
- Barometer
- Compass

ORDERING INFORMATION

DEVICE	PACKAGE	REEL QUANTITY
SX8725SWLTDT	MLPQ-W-16 4x4	1000

- Available in tape and reel only
- WEEE/RoHS compliant, Pb-Free and Halogen Free.

FUNCTIONAL BLOC DIAGRAM

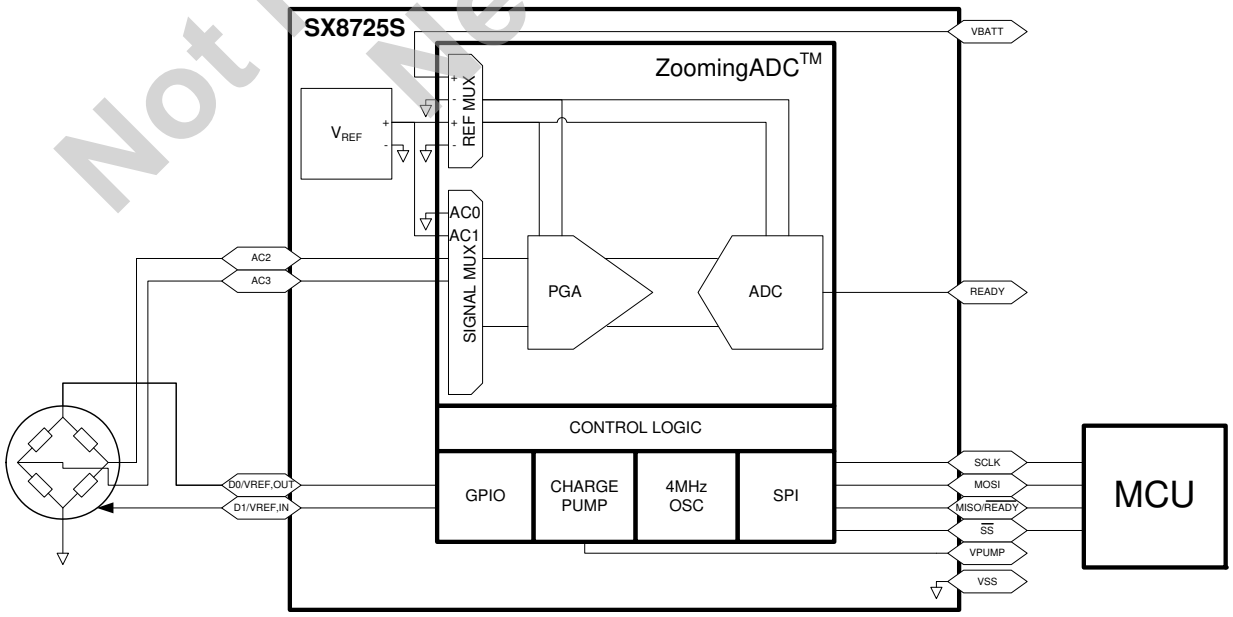


TABLE OF CONTENT

TABLE OF CONTENT

ELECTRICAL SPECIFICATIONS

1 Absolute Maximum Ratings

Note The Absolute Maximum Ratings, in table below, are stress ratings only. Functional operation of the device at conditions other than those indicated in the Operating Conditions sections of this specification is not implied.
Exposure to the absolute maximum ratings, where different to the operating conditions, for an extended period may reduce the reliability or useful lifetime of the product.

Table 1. Absolute Maximum Ratings

Parameter	Symbol	Condition	Min	Max	Units
Power supply	V_{BATT}		V_{SS} - 0.3	6.5	V
Storage temperature	T_{STORE}		-55	150	°C
Temperature under bias	T_{BIAS}		-40	140	°C
Input voltage	V_{INABS}	All inputs	V_{SS} - 300	V_{BATT} + 300	mV
Peak reflow temperature	T_{PKG}			260	°C
ESD conditions	ESD_{HBM}	Human Body Model ESD	2000		V
Latchup			100		mA

2 Operating Conditions

Unless otherwise specified: $V_{REF,ADC}$ = V_{BATT}, V_{IN} = 0V, Over-sampling frequency f_S = 250 kHz, *PGA3 on with Gain = 1*, *PGA1&PGA2 off*, offsets *GDOff2* = *GDOff3* = 0. Power operation: normal (*IbAmpAdc[1:0]* = *IbAmpPga[1:0]* = '01').
For resolution n = 12 bits: *OSR* = 32 and N_{ELCONV} = 4.
For resolution n = 16 bits: *OSR* = 256 and N_{ELCONV} = 2.
Bandgap chopped at N_{ELCONV} rate. If V_{BATT} < 3V, Charge Pump is forced on. If V_{BATT} > 3V, Charge Pump is forced off.

Table 2. Operating conditions limits

Parameter	Symbol	Comment/Condition	Min	Typ	Max	Unit
Power supply	V_{BATT}		2.4		5.5	V
Operating temperature	T_{OP}		-40		125	°C

.

Table 3. Electrical Characteristics

Parameter	Symbol	Comment/Condition	Min	Typ	Max	Unit
CURRENT CONSUMPTION[1]						
Active current, 5.5V	I_{OP55}	16 b @ 250 Sample/s ADC, fs = 125 kHz		250	300	µA
		16 b @ 1kSample/s PGA3 + ADC, fs = 500 kHz		650	850	
		16 b + gain 1000 @ 1kSample/s PGA3,2,1 + ADC, fs = 500 kHz		1000	1250	
Active current, 3.3V	I_{OP33}	16 b @ 250 Sample/s ADC, fs = 125 kHz		150		µA
		16 b @ 1 kSample/s PGA3 + ADC, fs = 500 kHz		500		
		16 b + gain 1000 @ 1kSample/s PGA3,2,1 + ADC, fs = 500 kHz		830		
Sleep current	I_{SLEEP}	@25°C		150	250	nA
		up to 85°C		200		
		@125°C		250		
TIME BASE						
Max ADC Over-Sampling frequency	f_{Smax}	@25°C	425	500	575	kHz
ADC Over-Sampling frequency drift	f_{ST}			0.15		% / °C
DIGITAL I/O						
Input logic high	V_{IH}		0.7			V_{BATT}
Input logic low	V_{IL}				0.3	V_{BATT}
Output logic high	V_{OH}	I_{OH} < 4 mA			V_{BATT}-0.4	V
Output logic low	V_{OL}	I_{OL} < 4 mA	0.4			V
Leakages currents						

Table 3. Electrical Characteristics

Parameter	Symbol	Comment/Condition	Min	Typ	Max	Unit
Input leakage current	I_{LeakIn}	Digital input mode, no pull-up or pull-down	-100		100	nA
VREF: Internal Bandgap Reference						
Absolute output voltage	V_{BG}	V_{BATT} > 3V	1.19	1.22	1.25	V
Variation over Temperature	V_{BGT}	V_{BATT} > 3V, over Temperature	-1.5		+1.5	%
Total Output Noise	V_{BGN}	V_{BATT} > 3V			1	mVrms

1. The device can be operated in either active or sleep states. The Sleep state is complete shutdown, but the active state can have a variety of different current consumptions depending on the settings. Some examples are given here: The Sleep state is the default state after power-on-reset. The chip can then be placed into an active state after a Slave Select command on $\overline{SS}$ pin is received.

Table 4. ZoomingADC Specifications

Parameter	Symbol	Condition	Min	Typ	Max	Unit
ANALOG INPUT CHARACTERISTICS						
Differential Input Voltage Range $V_{IN} = V_{INP}-V_{INN}$		Gain=1, OSR=32, V_{REF}=5V. **Note 1**	-2.42		+2.42	V
		Gain=100, OSR=32, V_{REF}=5V	-24.2		+24.2	mV
		Gain=1000, OSR=32, V_{REF}=5V	-2.42		+2.42	mV
PROGRAMMABLE GAIN AMPLIFIER						
Total PGA Gain	GD_{TOT}	**Note 1**	1/12		1000	V/V
PGA1 Gain	GD_1	(see **Table 10, page 22**)	1		10	V/V
PGA2 Gain	GD_2	(see **Table 11, page 22**)	1		10	V/V
PGA3 Gain	GD_3	Step = 1/12 V/V (see **Table 12, page 22**)	1/12		127/12	V/V
Gain Settings Precision (each stage)		Gain ≥ 1	-3	±0.5	+3	%
Gain Temperature Dependence				±5		ppm / °C
PGA2 Offset	GD_{OFF2}	Step = 0.2 V/V (see **Table 11, page 22**)	-1		+1	V/V
PGA3 Offset	GD_{OFF3}	Step = 1/12 V/V (see **Table 12, page 22**)	-63/12		+63/12	V/V
Offset Settings Precision (PGA2 or PGA3)		**Note 2**	-3	±0.5	+3	%
Offset Temperature Dependence				±5		ppm / °C
Input Impedance on ADC	Z_{INADC}		500			kΩ
Input Impedance on PGA1 (see **section 11.1, page 49**)	Z_{INPGA1}	Gain = 1. **Note 3**	900	1150		kΩ
		Gain = 10. **Note 3**	250	350		kΩ
Input Impedance on PGA2	Z_{INPGA2}	Gain = 1. **Note 3**	500	1000		kΩ
		Gain = 10. **Note 3**	125	270		kΩ
Input Impedance on PGA3	Z_{INPGA3}	Gain = 1. **Note 3**	500	780		kΩ
		Gain = 10. **Note 3**	125	190		kΩ

Table 4. ZoomingADC Specifications

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Output RMS Noise per over-sample		PGA1. **Note 4**		205		µV
		PGA2. **Note 4**		340		µV
		PGA3. **Note 4**		365		µV
ADC STATIC PERFORMANCES						
Resolution (No Missing Codes)	n	**Note 5** **Note 6**	6		16	Bits
Gain Error		**Note 7**		±0.15		%
Offset Error		n = 16 bits. **Note 8**		±1		LSB
Integral Non-Linearity	INL	resolution n = 12 bits. **Note 9**		±0.6		LSB
		resolution n = 16 bits. **Note 9**		±1.5		LSB
Differential Non-Linearity	DNL	resolution n = 12 bits. **Note 10**		±0.5		LSB
		resolution n = 16 bits. **Note 10**		±0.5		LSB
Power Supply Rejection Ratio DC	PSRR	V_{BATT} = 5V +/- 0.3V. **Note 11**		78		dB
		V_{BATT} = 3V +/- 0.3V. **Note 11**		72		dB
ADC DYNAMIC PERFORMANCES						
Conversion Time	T_{CONV}	n = 12 bits. **Note 12**		133		fs cycles
		n = 16 bits. **Note 12**		517		fs cycles
Throughput Rate (Continuous Mode)	$1/T_{CONV}$	n = 12 bits, fs = 250 kHz		1.88		kSps
		n = 16 bits, fs = 250 kHz		0.483		kSps
PGA Stabilization Delay		**Note 13** (see **Table 11, page 22**)		OSR		fs cycles
ZADC ANALOG QUIESCENT CURRENT						
ADC Only Consumption	I_Q	V_{BATT} = 5.5V/3.3V		285/210		µA
PGA1 Consumption		V_{BATT} = 5.5V/3.3V		104/80		µA
PGA2 Consumption		V_{BATT} = 5.5V/3.3V		67/59		µA
PGA3 Consumption		V_{BATT} = 5.5V/3.3V		98/91		µA
ANALOG POWER DISSIPATION: All PGAs & ADC Active						
Normal Power Mode		V_{BATT} = 5.5V/3.3V. **Note 14**		4.0/2.0		mW
3/4 Power Reduction Mode		V_{BATT} = 5.5V/3.3V. **Note 15**		3.2/1.6		mW
1/2 Power Reduction Mode		V_{BATT} = 5.5V/3.3V. **Note 16**		2.4/1.1		mW
1/4 Power Reduction Mode		V_{BATT} = 5.5V/3.3V. **Note 17**		1.5/0.7		mW

(1) Gain defined as overall *PGA* gain *GDTOT* = *GD1* x *GD2* x *GD3*. Maximum input voltage is given by: $V_{IN,MAX} = \pm(V_{REF} / 2)\ (OSR / OSR+1)$.
(2) Offset due to tolerance on *GDoff2* or *GDoff3* setting. For small intrinsic offset, use only *ADC* and *PGA1*.
(3) Measured with block connected to inputs through *Amux* block. Normalized input sampling frequency for input impedance is f_S = 500 kHz (f_S max, worst case). This figure must be multiplied by 2 for f_S = 250 kHz, 4 for f_S = 125 kHz. Input impedance is proportional to $1/f_S$.
(4) Figure independent from gain and sampling frequency. fs. The effective output noise is reduced by the over-sampling ratio
(5) Resolution is given by n = 2 log2(*OSR*) + log2(N_{ELCONV}). *OSR* can be set between 8 and 1024, in powers of 2. N_{ELCONV} can be set to 1, 2, 4 or 8.
(6) If a ramp signal is applied to the input, all digital codes appear in the resulting *ADC* output data.
(7) Gain error is defined as the amount of deviation between the ideal (theoretical) transfer function and the measured transfer function (with the offset error removed).
(8) Offset error is defined as the output code error for a zero volt input (ideally, output code = 0). For 1 LSB offset, N_{ELCONV} must be at least 2.

(9) INL defined as the deviation of the DC transfer curve of each individual code from the best-fit straight line. This specification holds over the full scale.
(10) DNL is defined as the difference (in LSB) between the ideal (1 LSB) and measured code transitions for successive codes.
(11) Values for Gain = 1. PSRR is defined as the amount of change in the *ADC* output value as the power supply voltage changes.
(12) Conversion time is given by: $T_{CONV} = (N_{ELCONV} (OSR + 1) + 1) / fs$. *OSR* can be set between 8 and 1024, in powers of 2. N_{ELCONV} can be set to 1, 2, 4 or 8.
(13) PGAs are reset after each writing operation to registers **RegACCfg1-5**, corresponding to change of configuration or input switching. The *ADC* should be started only some delay after a change of PGA configuration through these registers. Delay between change of configuration of PGA or input channel switching and ADC start should be equivalent to OSR (between 8 and 1024) number of cycles. This is done by writing bit Start several cycles after *PGA* settings modification or channel switching. This delay does not apply to conversions made without the *PGAs*.
(14) Nominal (maximum) bias currents in *PGAs* and *ADC*, i.e. *IbAmpPga[1:0]* = '11' and *IbAmpAdc[1:0]* = '11'.
(15) Bias currents in *PGAs* and *ADC* set to 3/4 of nominal values, i.e. *IbAmpPga[1:0]* = '10', *IbAmpAdc[1:0]* = '10'.
(16) Bias currents in *PGAs* and *ADC* set to 1/2 of nominal values, i.e. *IbAmpPga[1:0]* = '01', *IbAmpAdc[1:0]* = '01'.
(17) Bias currents in *PGAs* and *ADC* set to 1/4 of nominal values, i.e. *IbAmpPga[1:0]* = '00', *IbAmpAdc[1:0]* = '00'.

2.1 Timing Characteristics

Table 5. General timings

Parameter	Symbol	Comment/Condition	Min	Typ	Max	Unit
ADC INTERRUPT (READY) TIMING SPECIFICATIONS						
READY pulse width	t_{IRQ}	**Note 18**		1		1/fs
STARTUP TIMES						
Startup sequence time at POR	$t_{STARTUP}$				800	µs
Time to enable RC from Sleep after a SPI command	t_{RCEN}			100	450	µs
Effective Start	t_{START_SPI}			250		µs

(18) The READY pulse indicates End of Conversion. This is a Positive pulse of duration equal to one cycle of the ADC sampling rate in "continuous mode". See also **Figure 15, page 30** for data conversion waveforms.

2.1.1 POR Timings

The Slave Select pin ($\overline{SS}$) can be used to detect the effective start of the device. See **section 9.4, page 42** for functional descriptions. The SPI interface can be accessed as soon as the $\overline{SS}$ pin (slave) is set to 'input' as illustrated on **Figure 2**.

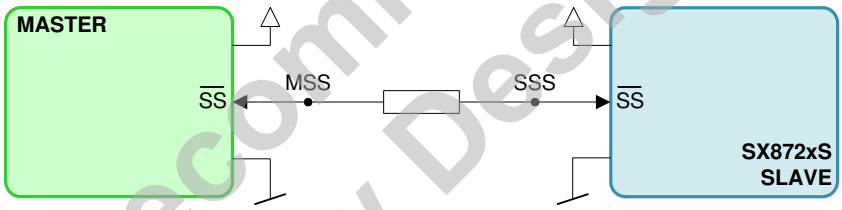


Figure 1. SPI Master detecting start sequence through Slave Select pin

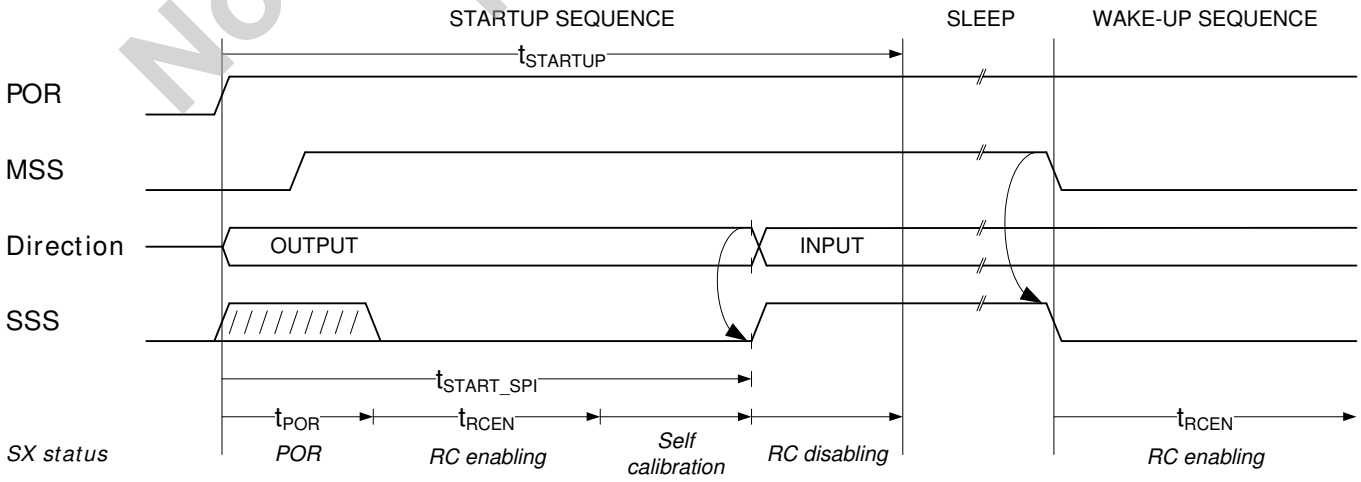


Figure 2. Slave Select pin and Power-On-Reset Timings

2.1.2 SPI interface timings

Parameter	Symbol	Min	Typ	Max	Units
$\overline{SS}$ to SCLK Edge	t_{SSSC}	30			ns
SCLK Period	t_{SC}	500			ns
SCLK Low Pulse width	t_{SCL}	200			ns
SCLK High Pulse width	t_{SCH}	200			ns
Data Output Valid after SCLK Edge	t_{DV}		125	200	ns
Data Input Setup Time before SCLK Edge	t_{DS}	0			ns
Data Input Hold Time after SCLK Edge	t_{DH}	100	250		ns
$\overline{SS}$ High after SCLK Edge	t_{SCSS}	0			ns
$\overline{SS}$ High to MISO High Impedance	t_{SSD}			30	ns

2.1.3 SPI timing diagram

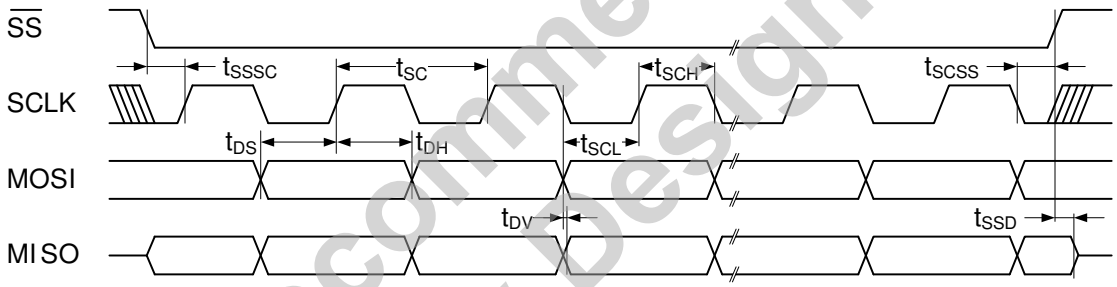
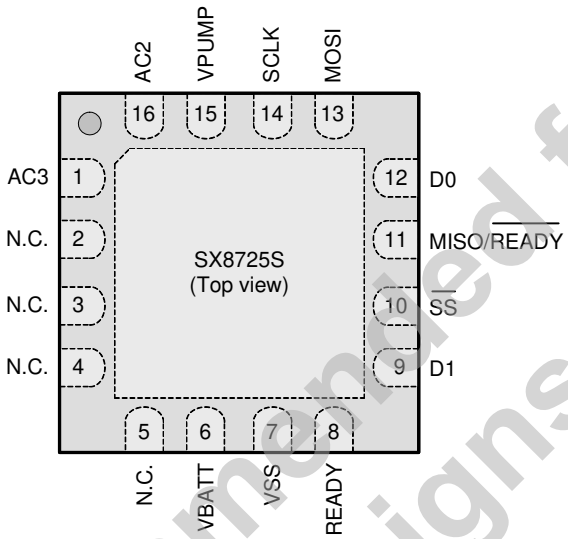


Figure 3. SPI timing diagram

CIRCUIT DESCRIPTION

3 Pin Configuration



4 Marking Information

nnnnn = Part Number
yyww = Date Code[1]
xxxxx = Semtech Lot Number
xxxxx

1.Date codes and Lot numbers starting with the 'E' character are used for Engineering samples

5 Pin Description

Note The bottom pad is internally connected to *VSS*. It should also be connected to *VSS* on PCB to reduce noise and improve thermal behavior.

Pin	Name	Type	Function
1	AC3	Analog Input	Differential sensor input in conjunction with AC2
2	N.C.	-	Not used
3	N.C.	-	Not used
4	N.C.	-	Not used
5	N.C.	-	Not used
6	VBATT	Power Input	2.4V to 5.5V power supply
7	VSS	Power Input	Chip Ground
8	READY	Digital Output	Data Ready (active high). Conversion complete flag.
9	D1	Digital IO	Digital output sensor drive (V_{BATT} or V_{SS})
		Analog	V_{REF} Input in optional operating mode
10	$\overline{SS}$	Digital Input	Slave select (active low).
11	MISO/$\overline{READY}$	Digital Output	Serial data output: Master Input, Slave Output. Can be combined with Data Ready (active low when Data Ready function enabled).
12	D0	Digital IO	Digital output sensor drive (V_{BATT} or V_{SS})
		Analog	V_{REF} Output in optional operating mode
13	MOSI	Digital Input	Serial data input: Master Output, Slave Input .
14	SCLK	Digital Input	Serial clock input.
15	VPUMP	Power IO	Charge pump output. Raises ADC supply above V_{BATT} if V_{BATT} supply is too low. Recommended range for capacitor is 1nF to 10 nF. Connect the capacitor to ground.
16	AC2	Analog Input	Differential sensor input in conjunction with AC3

6 General Description

The SX8725S is a complete low-power acquisition path with programmable gain, acquisition speed and resolution.

6.1 Bloc diagram

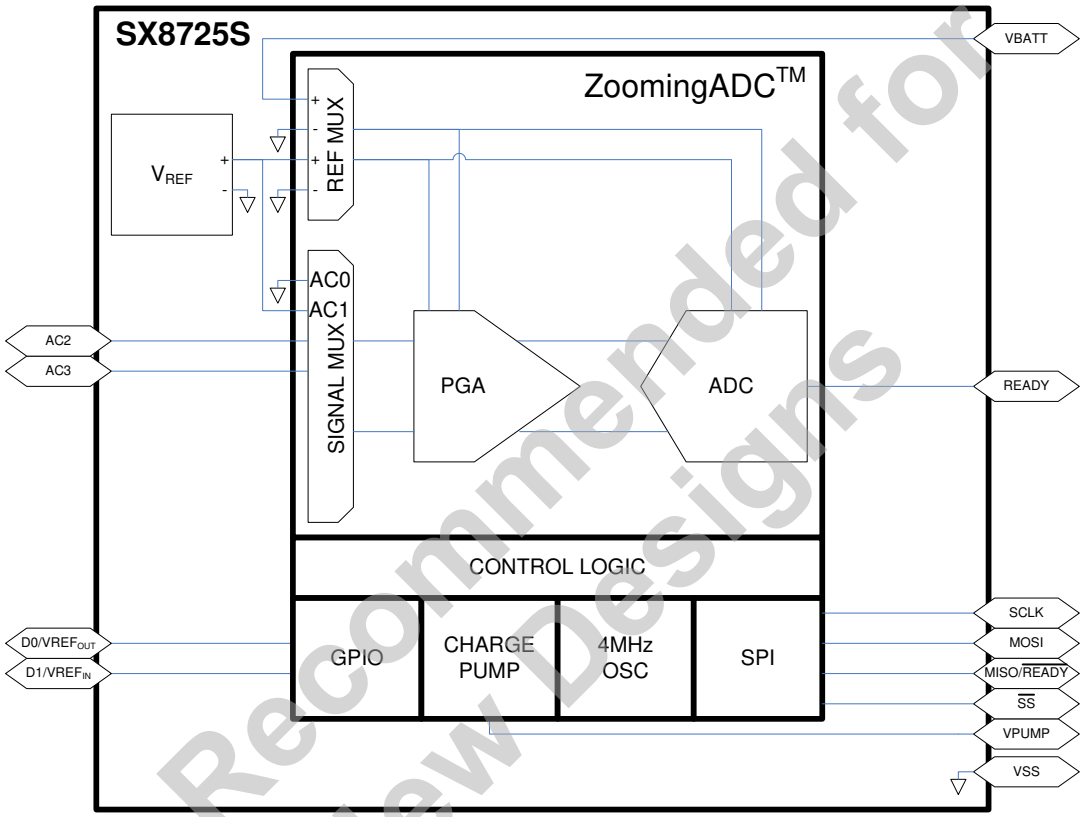


Figure 4. SX8725S bloc diagram

6.2 VREF

The internally generated *VREF* is a trimmed bandgap reference with a nominal value of 1.22V that provides a stable voltage reference for the *ZoomingADC*.

This reference voltage is directly connected to one of the ZoomingADC reference multiplexer inputs.

The bandgap voltage stability is only guaranteed for *VBATT* voltages of 3V and above. As *VBATT* drops down to 2.4V, the bandgap voltage could reduce by up to 50mV.

The bandgap has relatively weak output drive so it is recommended that if the bandgap is required as a signal input then *PGA1* must be enabled with gain = 1.

6.3 GPIO

The *GPIO* block is a multipurpose 2 bit input/output port. In addition to digital behavior, *D0* and *D1* pins can be programmed as analog pins in order to be used as output (reference voltage monitoring) and input for an external

reference voltage (For further details see **Figure 7**, **Figure 8**, **Figure 9** and **Figure 10**). Each port terminal can be individually selected as digital input or output.

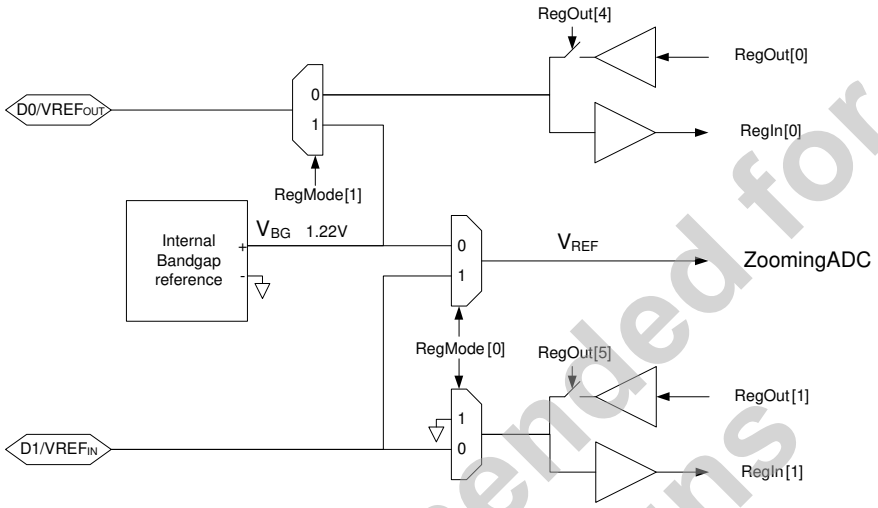


Figure 5. GPIO bloc diagram

The direction of each bit within the *GPIO* block (input only or input/output) can be individually set using the bits of the **RegOut** (address 0x40) register. If *D[x]Dir* = 1, both the input and output buffer are active on the corresponding *GPIO* block pin. If *D[x]Dir*= 0, the corresponding *GPIO* block pin is an input only and the output buffer is in high impedance. After power on reset the GPIO block pins are in input/output mode (*D[x]Dir* are reset to 1).

The input values of *GPIO* block are available in **RegIn** (address 0x41) register (read only). Reading is always direct - there is no debounce function in the *GPIO* block. In case of possible noise on input signals, an external hardware filter has to be realized. The input buffer is also active when the *GPIO* block is defined as output and the effective value on the pin can be read back.

Data stored in the LSB bits of **RegOut** register are outputted at *GPIO* block if *D[x]Dir= 1*. The default values after power on reset is low (0).
The digital pins are able to deliver a driving current up to 8 mA.

When the bits *VrefD0Out* and *VrefD1In* in the **RegMode** (address 0x70) register are set to 1 the *D0* and *D1* pins digital behavior are automatically bypassed in order to either input or output the voltage reference signals.

6.3.1 Optional Operating Mode: External Vref

D0 and *D1* are multi-functional pins with the following functions in different operating modes (see **RegMode** register for control settings):

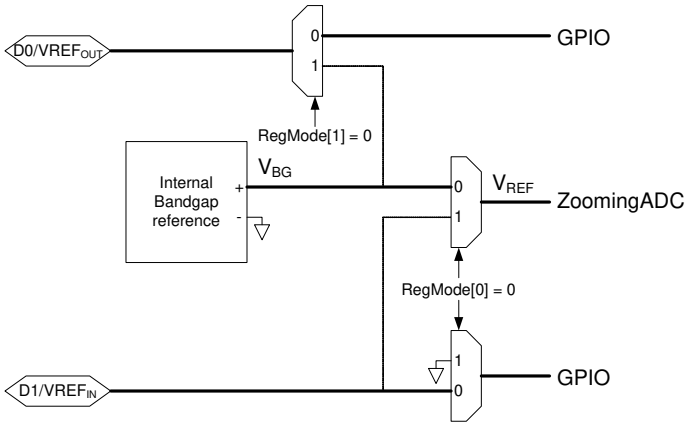


Figure 7. D0 and D1 are Digital Inputs / Outputs

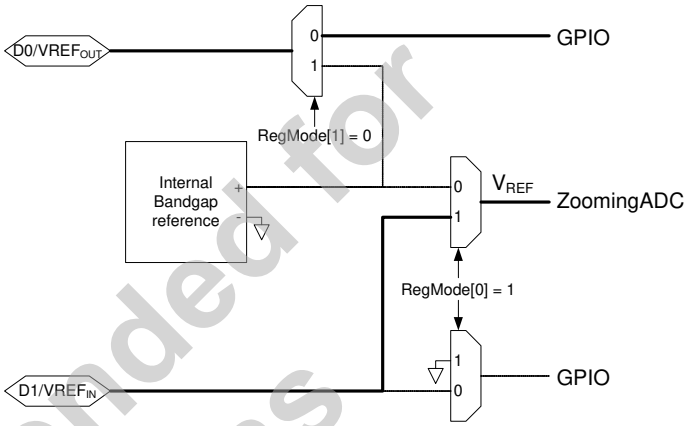


Figure 8. D1 is Reference Voltage Input and D0 is Digital Input / Output

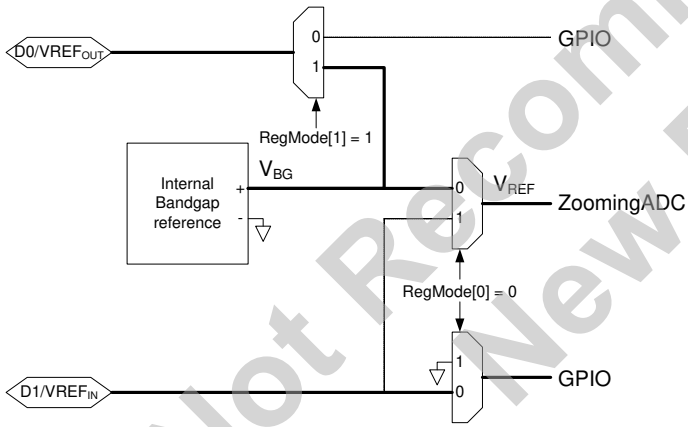


Figure 9. D1 is Digital Input / Output and D0 Reference Voltage Output

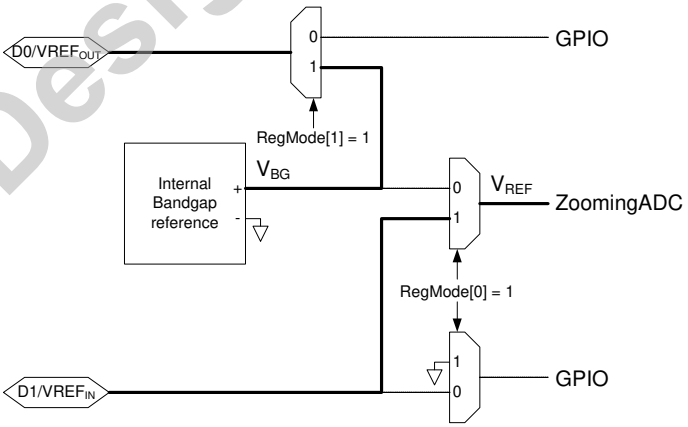


Figure 10. D0 is Reference Voltage Output and D1 is Reference Voltage Input

This allows external monitoring of the internal bandgap reference or the ability to use an external reference input for the *ADC*, or the option to filter the internal *VREF* output before feeding back as *VREF,ADC* input. The internally generated *VREF* is a trimmed as ADC reference with a nominal value of 1.22V. When using an external *VREF,ADC* input, it may have any value between 0V and *VBATT*. Simply substitute the external value for 1.22 V in the *ADC* conversion calculations.

6.4 Charge Pump

This block generates a supply voltage able to power the analog switch drive levels on the chip higher than VBATT if necessary.

If *VBATT* voltage drops below 3V then the block should be activated. If *VBATT* voltage is greater than 3V then *VBATT* may be switched straight through to the *VPUMP* output. If the charge pump is not activated then *VPUMP* = *VBATT*.

If control input bit *MultForceOff* = 1 in **RegMode** (address 0x70) register then the charge pump is disabled and *VBATT* is permanently connected to *VPUMP* output.

If control input bit *MultForceOn* = 1 in **RegMode** register then the charge pump is permanently enabled. This overrides *MultForceOff* bit in **RegMode** register.

An external capacitor is required on *VPUMP* pin. This capacitor should be large enough to ensure that generated voltage is smooth enough to avoid affecting conversion accuracy but not so large that it gives an unacceptable settling time. A recommended value is around 2.2nF.

6.5 RC Oscillator

This block provides the master clock reference for the chip. It produces a clock at 4 MHz which is divided internally in order to generate the clock sources needed by the other blocks.

The oscillator technique is a low power relaxation design and it is designed to vary as little as possible over temperature and supply voltage.

This oscillator is trimmed at manufacture chip test.

The *RC* oscillator will start up after a chip reset to allow the trimming values to be read and calibration registers. Once this has been done, the oscillator will be shut down and the chip will enter a sleep state while waiting for a SPI communication.

The worst case duration from reset (or POR) to the sleep state is 800us.

6.5.1 Wake-up from sleep

When the device is in sleep state, the *RC* oscillator will start up after a communication. The start up sequence for the *RC* oscillator is 450us in worst case.
During this time, the internal blocs using the RC can not be used: no ADC conversion can be started.

7 ZoomingADC

7.1 Overview

The *ZoomingADC* is a complete and versatile low-power analog front-end interface typically intended for sensing applications. In the following text the *ZoomingADC* will be referred as *ZADC*.

The key features of the *ZADC* are:

- Programmable 6 to 16-bit dynamic range over-sampled *ADC*
- Flexible gain programming between 1/12 and 1000
- Flexible and large range offset compensation
- Differential or single-ended input
- 2-channel differential reference inputs
- Power saving modes

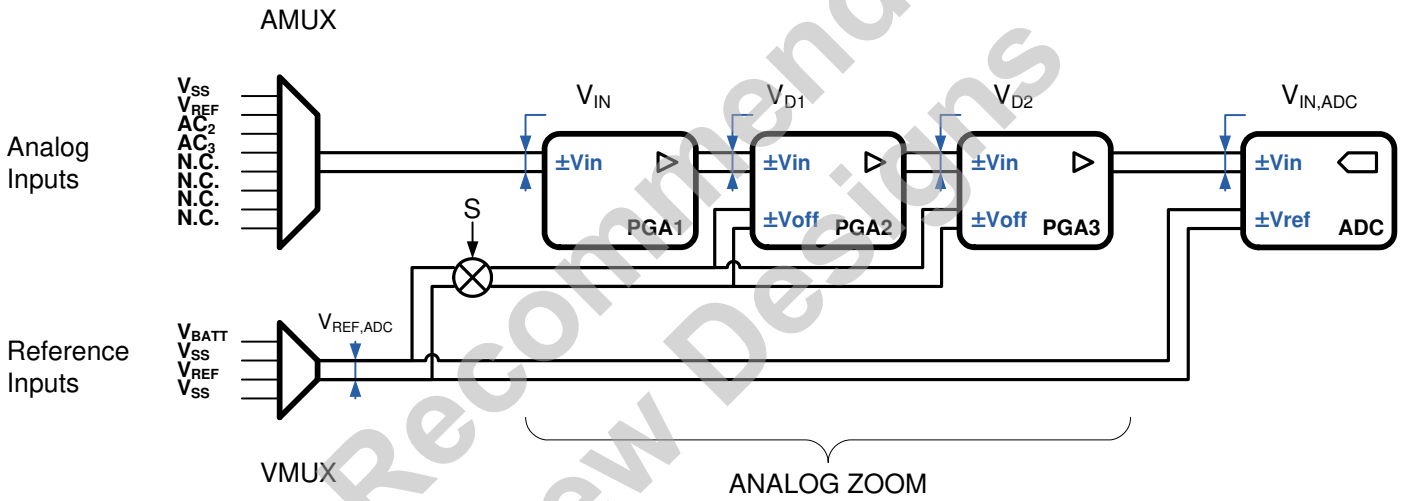


Figure 11. ZADC General Functional Block Diagram

The total acquisition chain consists of an input multiplexer, 3 programmable gain amplifier stages and an over sampled A/D converter. The reference voltage can be selected on two different channels. Two offset compensation amplifiers allow for a wide offset compensation range. The programmable gain and offset allow the application to zoom in on a small portion of the reference voltage defined input range.

7.1.1 Acquisition Chain

Figure 11, page 17 shows the general block diagram of the acquisition chain (*AC*). A control block (not shown in **Figure 11**) manages all communications with the SPI peripheral. The clocking is derived from the internal 4 MHz Oscillator.

Analog inputs can be selected through an 8 input multiplexer, while reference input is selected between two differential channels. It should however be noted that only 7 acquisition channels (including the VREF) are available when configured as single ended since the input amplifier is always operating in differential mode with both positive and negative input selected through the multiplexer.

The core of the zooming section is made of three differential programmable amplifiers (*PGA*). After selection of an input and reference signals VIN and VREF,ADC combination, the input voltage is modulated and amplified through stages 1 to 3. Fine gain programming up to 1'000 V/V is possible. In addition, the last two stages provide programmable offset. Each amplifier can be bypassed if needed.

The output of the cascade of *PGA* is directly fed to the analog-to-digital converter (*ADC*), which converts the signal VIN,ADC into digital.

Like most *ADCs* intended for instrumentation or sensing applications, the ZoomingADC™ is an over-sampled converter [1]. The *ADC* is a so-called incremental converter; with bipolar operation (the *ADC* accepts both positive and negative differential input voltages). In first approximation, the *ADC* output result relative to full-scale (*FS*) delivers the quantity:

$$\frac{OUT_{ADC}}{FS/2} \cong \frac{V_{IN,ADC}}{V_{REF}/2}$$

Equation 1

in two's complement (see **Equation 18** and **Equation 19, page 30** for details). The output code OUTADC is *-FS* / 2 to + *FS* / 2 for VIN,ADC = -VREF,ADC / 2 to + VREF,ADC / 2 respectively. As will be shown, VIN,ADC is related to input voltage VIN by the relationship:

$$V_{IN,ADC} = GD_{TOT} \cdot V_{IN} - GDoff_{TOT} \cdot S \cdot V_{REF} \quad [V]$$

Equation 2

where *GDTOT* is the total *PGA* gain, *GDOFFTOT* is the total magnitude of *PGA* offset and S is the sign of the offset (see **Table 8, page 21**).

7.1.2 Programmable Gain Amplifiers

As seen in **Figure 11, page 17**, the zooming function is implemented with three programmable gain amplifiers (*PGA*). These are:

- *PGA1*: coarse gain tuning
- *PGA2*: medium gain and offset tuning
- *PGA3*: fine gain and offset tuning. Should be set ON for high linearity data acquisition

All gain and offset settings are realized with ratios of capacitors. The user has control over each *PGA* activation and gain, as well as the offset of stages 2 and 3. These functions are examined hereafter.

1. Over-sampled converters are operated with a sampling frequency *fs* much higher than the input signal's Nyquist rate (typically *fs* is 20-1'000 times the input signal bandwidth). The sampling frequency to throughput ratio is large (typically 10-500). These converters include digital decimation filtering. They are mainly used for high resolution, and/or low-to-medium speed applications.

7.1.3 PGA & ADC Enabling

Depending on the application objectives, the user may enable or bypass each *PGA* stage. This is done according to the word *Enable* and the coding given in **Table 6**. To reduce power dissipation, the *ADC* can also be inactivated while idle.

Table 6. ADC and PGA Enabling

Enable (RegACCfg1[3:0])	Block
XXX0 XXX1	ADC disabled ADC enabled
XX0X XX1X	PGA1 disabled PGA1 enabled
X0XX X1XX	PGA2 disabled PGA2 enabled
0XXX 1XXX	PGA3 disabled PGA3 enabled

7.2 ZoomingADC Registers

The system has a bank of eight 8-bit registers: six registers are used to configure the acquisition chain (**RegAcCfg0** to **RegAcCfg5**), and two registers are used to store the output code of the analog-to-digital conversion (**RegAcOutMsb** & **Lsb**).

Table 7. Registers to Configure the Acquisition Chain (AC) and to Store the Analog-to-Digital Conversion (ADC) Result

Register Name	Bit position							
	7	6	5	4	3	2	1	0
RegACOutLsb	*Out*[7:0] **Note 1**							
RegACOutMsb	*Out*[15:8]							
RegACCfg0 Default values:	*Start* 0, **Note 2**	*SetNelconv* 01, **Note 3**		*SetOsr* 010, **Note 4**			*Continuous* 0, **Note 5**	*SampleShiftEn* 0, **Note 6**
RegACCfg1 Default value:	*IbAmpAdc* 11, **Note 7**		*IbAmpPga* 11, **Note 8**		*Enable* 0000, **Note 9**			
RegACCfg2 Default value:	*SetFs* 00, **Note 10**		*Pga2Gain* 00, **Note 12**		Pga2Offset 0000, **Note 14**			
RegACCfg3 Default value:	*Pga1Gain* 0, **Note 11**	*Pga3Gain* 0001100, **Note 13**						
RegACCfg4 Default value:	*DataReadyEn* 0, **Note 15**	*Pga3Offset* 0000000, **Note 16**						
RegACCfg5 Default value:	*Busy* 0, **Note 17**	*Def* 0, **Note 18**	*Amux* 00000, **Note 19**					*Vmux* 0, **Note 20**

(r = read; w = write; rw = read & write)

(1) **Out**: (r) digital output code of the analog-to-digital converter. (*MSB = Out[15]*)
(2) **Start**: (w) setting this bit triggers a single conversion (after the current one is finished). This bit always reads back 0.

(3) **SetNelconv**: (rw) sets the number of elementary conversions to $2^{(SetNelconv[1:0])}$. To compensate for offsets, the input signal is chopped between elementary conversions (1,2,4,8).
(4) **SetOsr**: (rw) sets the over-sampling rate (*OSR*) of an elementary conversion to $2^{(3+SetOsr[2:0])}$. *OSR* = 8, 16, 32, ..., 512, 1024.
(5) **Continuous**: (rw) setting this bit starts a conversion. When this bis is 1, A new conversion will automatically begin directly when the previous one is finished.
(6) **SampleShiftEn**: (rw) the 16-bit samples can be directly shifted out though the SPI interface by the master when a conversion is done.
(7) **IbAmpAdc**: (rw) sets the bias current in the *ADC* to 0.25 x (1+ *IbAmpAdc[1:0]*) of the normal operation current (25, 50, 75 or 100% of nominal current). To be used for low-power, low-speed operation.
(8) **IbAmpPga**: (rw) sets the bias current in the PGAs to 0.25 x (1+*IbAmpPga[1:0]*) of the normal operation current (25, 50, 75 or 100% of nominal current). To be used for low-power, low-speed operation.
(9) **Enable**: (rw) enables the *ADC* modulator (bit 0) and the different stages of the *PGAs* (*PGAi* by bit i=1,2,3). *PGA* stages that are disabled are bypassed.
(10) **SetFs**: (rw) These bits set the over sampling frequency of the acquisition chain. Expressed as a fraction of the oscillator frequency, the sampling frequency is given as: 11 ' 500 kHz, 10 ' 250 kHz, 01 ' 125 kHz, 00 ' 62.5 kHz.
(11) **Pga1Gain**: (rw) sets the gain of the first stage: 0 ' 1, 1 ' 10.
(12) **Pga2Gain**: (rw) sets the gain of the second stage: 00 ' 1, 01 ' 2, 10 ' 5, 11 ' 10.
(13) **Pga3Gain**: (rw) sets the gain of the third stage to *Pga3Gain[6:0]* 1/12.
(14) **Pga2Offset**: (rw) sets the offset of the second stage between -1 and +1, with increments of 0.2. The *MSB* gives the sign (0 positive, 1 negative); amplitude is coded with the bits *Pga2Offset[5:0]*.
(15) **DataReadyEn**: (rw) enables the combined data ready mode with the MISO of the SPI interface.
(16) **Pga3Offset**: (rw) sets the offset of the third stage between -5.25 and +5.25, with increments of 1/12. The *MSB* gives the sign (0 positive, 1 negative); amplitude is coded with the bits *Pga3Offset[5:0]*.
(17) **Busy**: (r) set to 1 if a conversion is running.
(18) **Def**: (w) sets all values to their defaults (PGA disabled, *AMux* not changed, *VMux* not changed, *ADC* enabled, nominal modulator bias current (100%), 2 elementary conversions, *OSR* = 32, N_{ELCONV} = 2, *fs* = 62.5kHz) and starts a new conversion without waiting the end of the preceding one.
(19) **Amux**(4:0): (rw) *Amux[4]* sets the mode (0 ' differential inputs, 1 ' single ended inputs with A0= common reference) *Amux[3]* sets the sign (0 ' straight, 1' cross) *Amux[2:0]* sets the channel.
(20) **Vmux**: (rw) sets the differential reference channel (0 ' V_{BATT}, 1 ' V_{REF}).

7.3 Input Multiplexers (AMUX and VMUX)

The ZoomingADC has analog inputs *AC0* to *AC3* and reference inputs. Let us first define the differential input voltage V_{IN} and reference voltage $V_{REF,ADC}$ respectively as:

$$V_{IN} = V_{INP} - V_{INN} \quad [V]$$

Equation 3

$$V_{REF} = V_{REFP} - V_{REFN} \quad [V]$$

Equation 4

As shown in **Table 8**, the inputs can be configured in two ways: either as 4 differential channels (*VIN1= AC1 - AC0*, *VIN2 = AC3 - AC2*), or *AC0* can be used as a common reference, providing 7 signal paths all referred to *AC0*. The control word for the analog input selection is *Amux*. Notice that the *Amux* bit 4 controls the sign of the input voltage.

Table 8. Analog Input Selection

Amux (RegACCfg5[5:1])	VINP	VINN
Sign S = 1		
00x00	AC1(VREF)	AC0(VSS)
00x01	AC3	AC2
00x10	N.C.	N.C.
00x11	N.C.	N.C.
10000	AC0(VSS)	AC0(VSS)
10001	AC1(VREF)	
10010	AC2	
10011	AC3	
10100	N.C.	
10101	N.C.	
10110	N.C.	
10111	N.C.	

Amux (RegACCfg5[5:1])	VINP	VINN
Sign S = -1		
01x00	AC1(VSS)	AC0(VREF)
01x01	AC2	AC3
01x10	N.C.	N.C.
01x11	N.C.	N.C.
11000	AC0(VSS)	AC0(VSS)
11001		AC1(VREF)
11010		AC2
11011		AC3
11100		N.C.
11101		N.C.
11110		N.C.
11111		N.C.

Similarly, the reference voltage is chosen among two differential channels (*VREF = VBATT-VSS*, *VREF = VBG-VSS* or *VREF = VREF,IN-VSS*) as shown in **Table 9**. The selection bit is *Vmux*. The reference inputs *VREFP* and *VREFN* (common-mode) can be up to the power supply range.

Table 9. Analog reference Input Selection

Vmux (RegACCfg5[0])	VREFP	VREFN
0	VREF = VBATT	VSS
1	VREF = VBG or VREF,IN[1]	VSS

1. External voltage reference on D1 GPIO pin. See **section 6.3 on page 13** about GPIO and "RegMode[0x70]" on page 48.

7.4 First Stage Programmable Gain Amplifier (PGA1)

The first stage can have a buffer function (unity gain) or provide a gain of 10 (see **Table 10**). The voltage *VD1* at the output of *PGA1* is:

$$V_{D1} = GD_1 \cdot V_{IN} \quad [V]$$

Equation 5

where *GD1* is the gain of *PGA1* (in V/V) controlled with the *Pga1Gain* bit.

Table 10. PGA1 gain settings

Pga1Gain bit (RegACCfg3[7])	PGA1 gain [V/V] *GD1* [V/V]
0	1
1	10

7.5 Second Stage Programmable Gain Amplifier (PGA2)

The second *PGA* has a finer gain and offset tuning capability, as shown in **Table 11**. The *VD2* voltage at the output of *PGA2* is given by:

$$V_{D2} = GD_2 \cdot V_{D1} - GDoff_2 \cdot S \cdot V_{REF} \quad [V]$$

Equation 6

where *GD2* and *GDOFF2* are respectively the gain and offset of *PGA2* (in V/V). These are controlled with the words *Pga2Gain[1:0]* and *Pga2Offset[3:0]*.

Table 11. PGA2 gain and offset settings

Pga2Gain bit field (RegACCfg2[5:4])	PGA2 gain [V/V] *GD2* [V/V]
00	1
01	2
10	5
11	10

Pga2Offset bit field (RegACCfg2[3:0])	PGA2 offset *GDOFF2* [V/V]
0000	0
0001	+0.2
0010	+0.4
0011	+0.6
0100	+0.8
0101	+1
1000	0
1001	-0.2
1010	-0.4
1011	-0.6
1100	-0.8
1101	-1.0

7.6 Third Stage Programmable Gain Amplifier (PGA3)

The finest gain and offset tuning is performed with the third and last *PGA* stage, according to the coding of **Table 12**.

Table 12. PGA3 Gain and Offset Settings

Pga3Gain bit field (RegACCfg3[6:0])	PGA3 Gain *GD3* [V/V]
0000000	0
0000001	1/12 (=0.083)

Pga3Offset bit field (RegACCfg4[6:0])	PGA3 Offset *GDOFF3* [V/V]
0000000	0
0000001	+1/12 (=0.083)

Table 12. PGA3 Gain and Offset Settings

Pga3Gain bit field (RegACCfg3[6:0])	PGA3 Gain *GD3* [V/V]
...	...
0000110	6/12
...	...
0001100	12/12
0010000	16/12
...	...
0100000	32/12
...	...
1000000	64/12
...	...
1111111	127/12 (=10.58)

Pga3Offset bit field (RegACCfg4[6:0])	PGA3 Offset *GDOFF3* [V/V]
...	
0010000	+16/12
...	...
0100000	32/12
...	...
0111111	+63/12 (=+5.25)
1000000	0
1000001	-1/12 (=-0.083)
1000010	-2/12
...	...
1010000	-16/12
...	...
1100000	-32/12
...	...
1111111	-63/12 (=-5.25)

The output of *PGA3* is also the input of the *ADC*. Thus, similarly to *PGA2*, we find that the voltage entering the *ADC* is given by:

$$V_{IN,ADC} = GD_3 \cdot V_{D2} - GDoff_3 \cdot S \cdot V_{REF} \quad [V]$$

Equation 7

where *GD3* and *GDOFF3* are respectively the gain and offset of *PGA3* (in V/V). The control words are *Pga3Gain[6:0]* and *Pga3Offset[6:0]*.

To remain within the signal compliance of the *PGA* stages (no saturation), the condition:

$$|V_{IN}|, |V_{D1}|, |V_{D2}| < \frac{V_{BATT}}{2}$$

Equation 8

must be verified.

To remain within the signal compliance of the *ADC* (no saturation), the condition:

$$\left|V_{IN,ADC}\right| < \left(\frac{V_{REF}}{2}\right)\left(\frac{OSR-1}{OSR}\right)$$

Equation 9

must be verified.
Finally, combining **Equation 5** to **Equation 7** for the three *PGA* stages, the input voltage $V_{IN,ADC}$ of the *ADC* is related to V_{IN} by:

$$V_{IN,ADC} = GD_{TOT} \cdot V_{IN} - GDoff_{TOT} \cdot S \cdot V_{REF} \quad [V]$$

Equation 10

where the total *PGA* gain is defined as:

$$GD_{TOT} = GD_3 \cdot GD_2 \cdot GD_1$$

Equation 11

and the total *PGA* offset is:

$$GDoff_{TOT} = GDoff_3 + GD_3 \cdot GDoff_2$$

Equation 12

7.7 Analog-to-Digital Converter (ADC)

The main performance characteristics of the *ADC* (resolution, conversion time, etc.) are determined by three programmable parameters. The setting of these parameters and the resulting performances are described later.

- *fs*: Over-sampling frequency
- *OSR*: Over-Sampling Ratio
- *NELCONV*: Number of Elementary Conversions

7.7.1 Conversion Sequence

A conversion is started each time the bit *Start* or the *Def* bit is set. As depicted in **Figure 12**, a complete analog-to-digital conversion sequence is made of a set of *NELCONV* elementary incremental conversions and a final quantization step. Each elementary conversion is made of (*OSR*+1) over-sampling periods *Ts*=1/*fs*, i.e.:

$$T_{ELCONV} = (OSR+1)/f_S \quad [s]$$

Equation 13

The result is the mean of the elementary conversion results. An important feature is that the elementary conversions are alternatively performed with the offset of the internal amplifiers contributing in one direction and the other to the output code. Thus, converter internal offset is eliminated if at least two elementary sequences are performed (i.e. if *NELCONV* >= 2). A few additional clock cycles are also required to initiate and end the conversion properly.

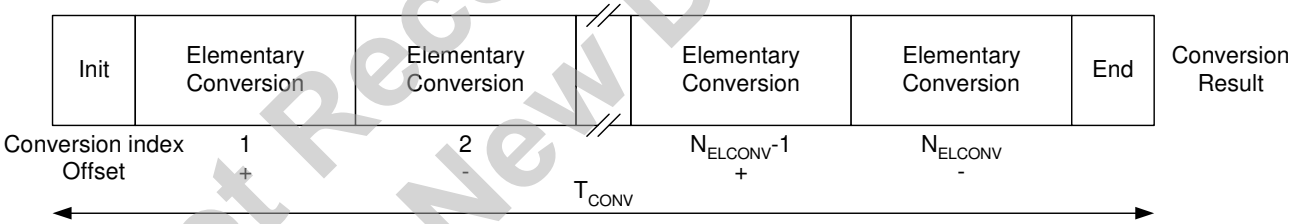


Figure 12. Analog-to-Digital Conversion Sequence

Note The internal bandgap reference state may be forced High or Low, or may be set to toggle during conversion at either the same rate or half the rate of the Elementary Conversion. This may be useful to help eliminate bandgap related internal offset voltage and 1/*fs* noise.