imall

Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from, Europe, America and south Asia, supplying obsolete and hard-to-find components to meet their specific needs.

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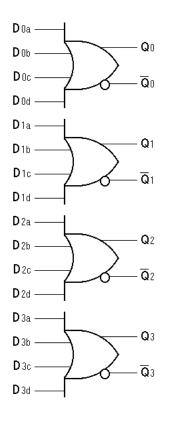
QUAD 4-INPUT OR/NOR GATE

SY10E101 SY100E101

FEATURES

- 500ps max. propagation delay
- Extended 100E VEE range of -4.2V to -5.5V
- True and complementary outputs
- Fully compatible with industry standard 10KH, 100K I/O levels
- Internal 75KΩ input pulldown resistors
- Fully compatible with Motorola MC10E/100E101
- Available in 28-pin PLCC package

BLOCK DIAGRAM



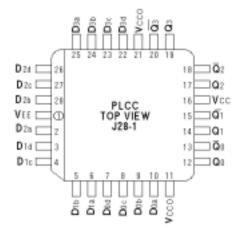
DESCRIPTION

The SY10/100E101 are quad 4-input OR/NOR gates designed for use in new, high-performance ECL systems. The E101 features both true and complementary outputs.

PIN NAMES

Pin	Function
Dna, Dnb, Dnc, Dnd	Data Inputs
Q0-Q3	True Outputs
\overline{Q}_0 - \overline{Q}_3	Inverting Outputs
Vcco	Vcc to Output

PACKAGE/ORDERING INFORMATION



28-Pin PLCC (J28-1)

Ordering Information⁽¹⁾

Part Number	Package Type	Operating Range	Package Marking	Lead Finish		
SY10E101JI	J28-1	Industrial	SY10E101JI	Sn-Pb		
SY10E101JITR ⁽²⁾	J28-1	Industrial	SY10E101JI	Sn-Pb		
SY100E101JI	J28-1	Industrial	SY100E101JI	Sn-Pb		
SY100E101JITR ⁽²⁾	J28-1	Industrial	SY100E101JI	Sn-Pb		
SY10E101JC	J28-1	Commercial	SY10E101JC	Sn-Pb		
SY10E101JCTR ⁽²⁾	J28-1	Commercial	SY10E101JC	Sn-Pb		
SY100E101JC	J28-1	Commercial	SY100E101JC	Sn-Pb		
SY100E101JCTR ⁽²⁾	J28-1	Commercial	SY100E101JC	Sn-Pb		
SY10E101JY ⁽³⁾	J28-1	Industrial	SY10E101JY with Pb-Free bar-line indicator	Matte-Sn		
SY10E101JYTR ^(2, 3)	J28-1	Industrial	SY10E101JY with Pb-Free bar-line indicator	Matte-Sn		
SY100E101JY ⁽³⁾	J28-1	Industrial	SY100E101JY with Pb-Free bar-line indicator	Matte-Sn		
SY100E101JYTR ^(2, 3)	J28-1	Industrial	ustrial SY100E101JY with Pb-Free bar-line indicator			

Notes:

1. Contact factory for die availability. Dice are guaranteed at $T_A = 25^{\circ}C$, DC Electricals only.

2. Tape and Reel.

3. Pb-Free package is recommended for new designs.

LOGIC EQUATION

Qn = Dna + Dnb + Dnc + Dnd

DC ELECTRICAL CHARACTERISTICS⁽¹⁾

VEE = VEE(Min.) to VEE(Max.); VCC = VCCO = GND

		TA = −40°C			TA = 0°C			TA = +25°C			TA = +85°C			
Symbol	Parameter	Min.	Тур.	Max.	Min.	Тур.	Max.	Min.	Тур.	Max.	Min.	Тур.	Max.	Unit
Іін	Input HIGH Current	_	_	150	_	_	150	_	_	150	_	_	150	μA
IEE	Power Supply Current 10EL 100EL		30 30	36 36		30 30	36 36		30 30	36 36		30 35	36 42	mA

Note:

1. Specification for packaged product only.

AC ELECTRICAL CHARACTERISTICS⁽³⁾

VEE = VEE(Min.) to VEE(Max.); VCC = VCCO = GND

		TA = -40°C		TA = 0°C			TA = +25°C			TA = +85°C				
Symbol	Parameter	Min.	Тур.	Max.	Min.	Тур.	Max.	Min.	Тур.	Max.	Min.	Тур.	Max.	Unit
tPD	Propagation Delay to Output D to Q	150	—	550	200	350	500	200	350	500	200	350	500	ps
tskew	Within-Device Skew ⁽¹⁾ Within-Gate Skew ⁽²⁾	_	50 25			50 25			50 25	_	_	50 25	-	ps ps
tr tf	Rise/Fall Time 20% to 80%	275		625	300	380	575	300	380	575	300	380	575	ps

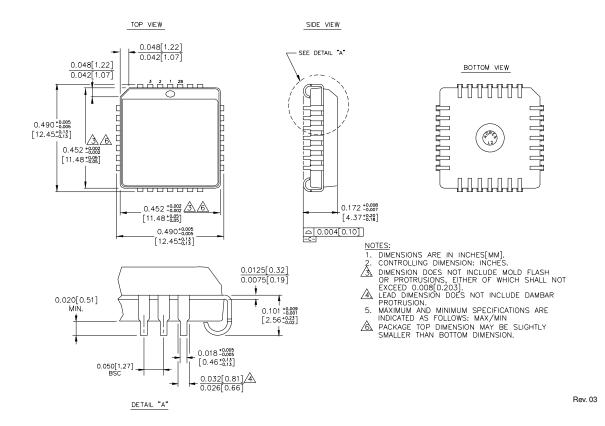
Notes:

1. Within-device skew is defined as identical transitions on similar paths through a device.

2. Within-gate skew is defined as the variation in propagation delays through a single gate when driven from its different inputs.

3. Specification for packaged product only.

28-PIN PLCC (J28-1)



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