Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

4-BIT D FLIP-FLOP

SY10E131
SY100E131

FEATURES

- **1100MHz min. toggle frequency**
- **Extended 100E V_{EE} range of –4.2V to –5.5V**
- **Differential output**
- **Individual and common clocks**
- **Indivldual asynchronous reset**
- **Paired asynchronous sets**
- **Fully compatible with Industry standard 10KH, 100K ECL levels**
- **Internal 75KΩ input pulldown resistors**
- **Fully compatible with Motorola MC10E/100E131**
- **Available in 28-pin PLCC package**

DESCRIPTION

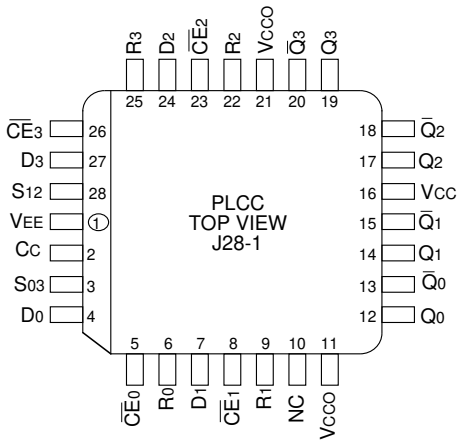
The SY10/100E131 are high-speed quad master slave D-type flip-flops with differential outputs designed for use in new, high-performance ECL systems. The flip-flops may be individually clocked by holding C_C (Common Clock) at a logic LOW and then using the four individual $\overline{CE}$ (Clock Enable $\overline{CE}_0$–$\overline{CE}_3$) inputs to accomplish such clocking. Alternatively, all four flip-flops can be clocked in common by holding the $\overline{CE}$ inputs LOW and then using C_C to clock the data. In the common clock mode, the $\overline{CE}$ input acts as a control that passes the C_C signal to the flip-flop. Data is clocked into the flip-flop on the rising edge of the output of the logical OR operation between $\overline{CE}$ and C_C (data enters the master when both C_C and $\overline{CE}$ are LOW and data transfers to the slave when either $\overline{CE}$ or C_C, or both, go HIGH).

Asynchronous set and reset controls are provided. The reset controls are individual and the set controls are pairwise.

PIN NAMES

Pin	Function
D_0-D_3	Data Inputs
$\overline{CE}_0$-$\overline{CE}_3$	Clock Enables (Individual)
R_0-R_3	Resets
C_C	Common Clock
S_{03}, S_{12}	Sets (paired)
Q_0-Q_3	True Outputs
$\overline{Q}_0$-$\overline{Q}_3$	Inverting Outputs
V_{CCO}	V_{CC} to Output

PACKAGE/ORDERING INFORMATION



28-Pin PLCC (J28-1)

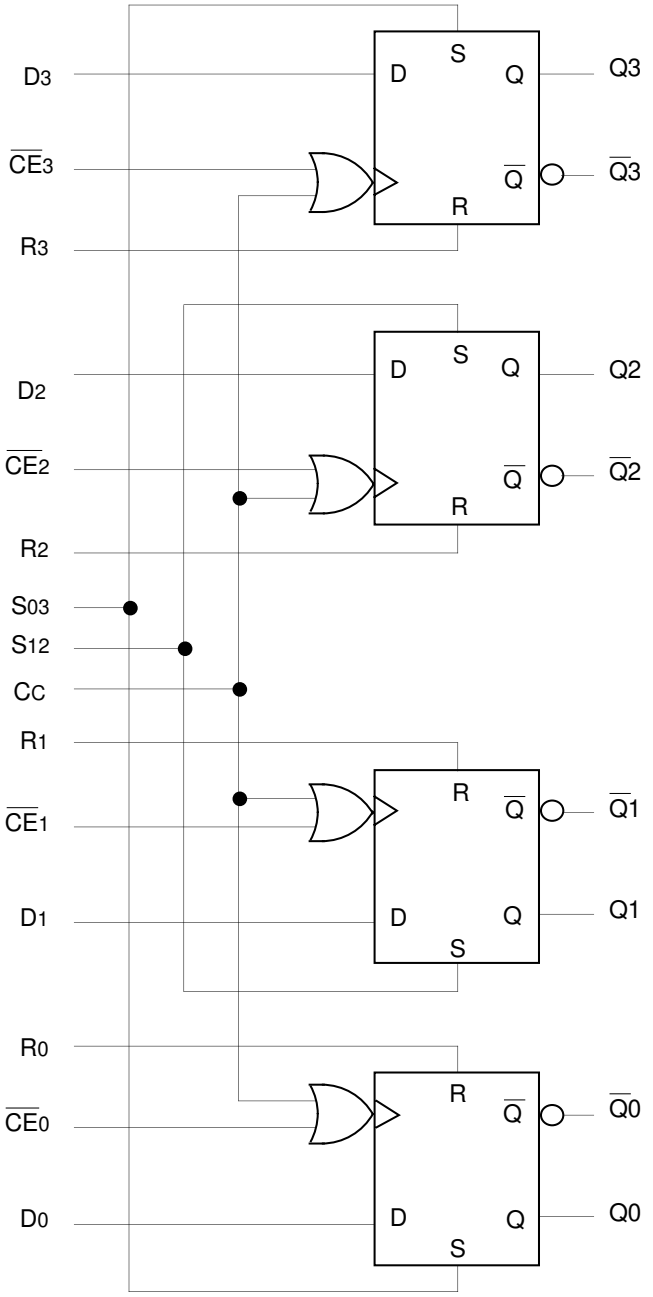
Ordering Information[1]

Part Number	Package Type	Operating Range	Package Marking	Lead Finish
SY10E131JI	J28-1	Industiral	SY10E131JI	Sn-Pb
SY10E131JITR[2]	J28-1	Industrial	SY10E131JI	Sn-Pb
SY100E131JI	J28-1	Industrial	SY100E131JI	Sn-Pb
SY100E131JITR[2]	J28-1	Industrial	SY100E131JI	Sn-Pb
SY10E131JC	J28-1	Commercial	SY10E131JC	Sn-Pb
SY10E131JCTR[2]	J28-1	Commercial	SY10E131JC	Sn-Pb
SY100E131JC	J28-1	Commercial	SY100E131JC	Sn-Pb
SY100E131JCTR[2]	J28-1	Commercial	SY100E131JC	Sn-Pb
SY10E131JY[3]	J28-1	Industiral	SY10E131JY with Pb-Free bar-line indicator	Matte-Sn
SY10E131JYTR[2, 3]	J28-1	Industrial	SY10E131JY with Pb-Free bar-line indicator	Matte-Sn
SY100E131JY[3]	J28-1	Industrial	SY100E131JY with Pb-Free bar-line indicator	Matte-Sn
SY100E131JYTR[2, 3]	J28-1	Industrial	SY100E131JY with Pb-Free bar-line indicator	Matte-Sn

Notes:

1. Contact factory for die availability. Dice are guaranteed at T_A = 25°C, DC Electricals only.
2. Tape and Reel.
3. Pb-Free package is recommended for new designs.

BLOCK DIAGRAM



TRUTH TABLE

Pin	State	Mode
C_C	L	Individual clocking with $\overline{CE}_n$
$\overline{CE}$	L	Common clocking with C_C

DC ELECTRICAL CHARACTERISTICS

V_{EE} = V_{EE}(Min.) to V_{EE}(Max.); V_{CC} = V_{CCO} = GND

Symbol	Parameter	T_A = –40°C			T_A = 0°C			T_A = +25°C			T_A = +85°C			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
I_{IH}	Input HIGH Current													µA
	C_C	—	—	350	—	—	350	—	—	350	—	—	350	
	S	—	—	450	—	—	450	—	—	450	—	—	450	
	R	—	—	300	—	—	300	—	—	300	—	—	300	
	$\overline{CE}$	—	—	300	—	—	300	—	—	300	—	—	300	
	D	—	—	150	—	—	150	—	—	150	—	—	150	
I_{EE}	Power Supply Current													mA
	10E	—	58	70	—	58	70	—	58	70	—	58	70	
	100E	—	58	70	—	58	70	—	58	70	—	67	81	

AC ELECTRICAL CHARACTERISTICS

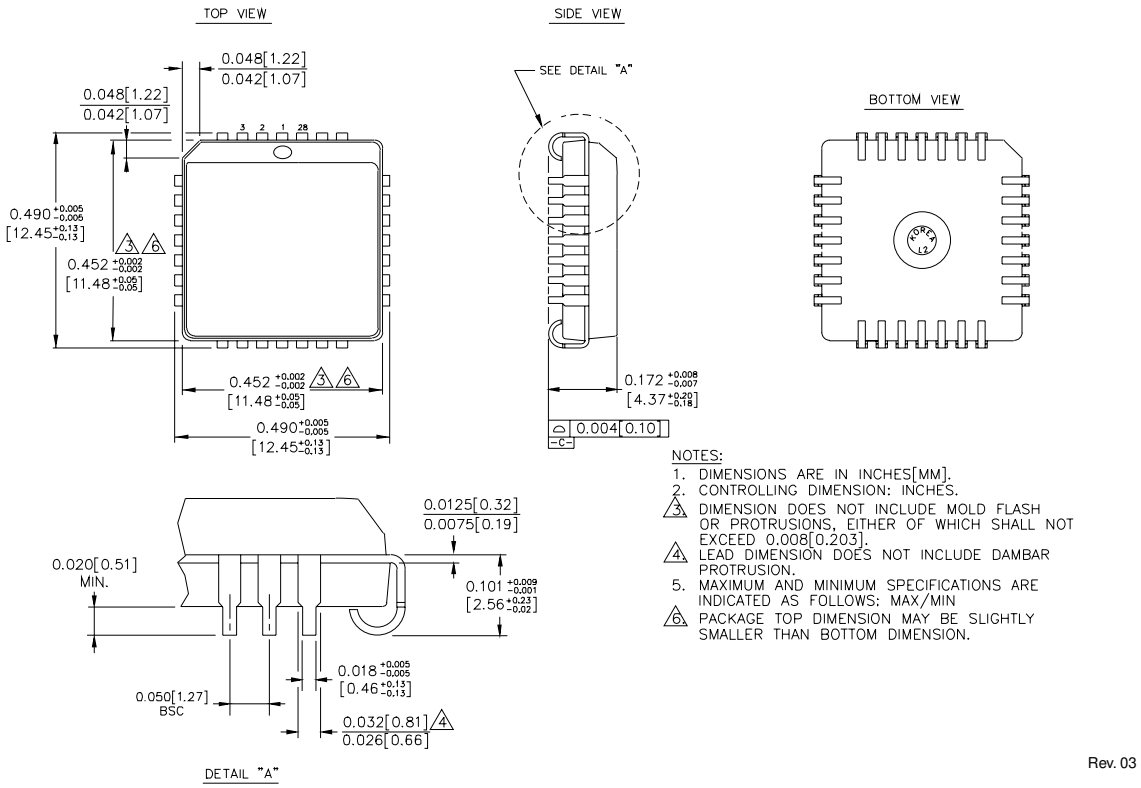
V_{EE} = V_{EE}(Min.) to V_{EE}(Max.); V_{CC} = V_{CCO} = GND

Symbol	Parameter	T_A = –40°C			T_A = 0°C			T_A = +25°C			T_A = +85°C			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
f_{MAX}	Max. Toggle Frequency	1100	1400	—	1100	1400	—	1100	1400	—	1100	1400	—	MHz
t_{PD}	Propagation Delay to													ps
	Output CE	310	600	750	360	500	700	360	500	700	360	500	700	
	C_C	275	600	725	325	500	675	325	500	675	325	500	675	
	R	300	625	775	350	550	725	350	550	725	350	550	725	
	S	300	550	775	350	550	725	350	550	725	350	550	725	
t_S	Set-up Time, D[2]	200	20	—	150	20	—	150	20	—	150	20	—	ps
t_H	Hold Time, D[2]	225	–20	—	175	–20	—	175	–20	—	175	–20	—	ps
t_{RR}	Reset Recovery Time	450	150	—	400	150	—	400	150	—	400	150	—	ps
t_{PW}	Minimum Pulse Width													ps
	Clk	400	—	—	400	—	—	400	—	—	400	—	—	
	R, S	400	—	—	400	—	—	400	—	—	400	—	—	
t_{skew}	Within-Device Skew[1]	—	60	—	—	60	—	—	60	—	—	60	—	ps
t_r t_f	Rise/Fall Time 20% to 80%	275	460	725	300	480	675	300	480	675	300	480	675	ps

Notes:

1. Within-device skew is defined as identical transitions on similar paths through a device.
2. Set-up/hold times guaranteed for both C_C and $\overline{CE}$.

28-PIN PLCC (J28-1)



NOTES:
1. DIMENSIONS ARE IN INCHES[MM].
2. CONTROLLING DIMENSION: INCHES.
3. DIMENSION DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS, EITHER OF WHICH SHALL NOT EXCEED 0.008[0.203].
4. LEAD DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION.
5. MAXIMUM AND MINIMUM SPECIFICATIONS ARE INDICATED AS FOLLOWS: MAX/MIN
6. PACKAGE TOP DIMENSION MAY BE SLIGHTLY SMALLER THAN BOTTOM DIMENSION.

Rev. 03

MICREL, INC. 2180 FORTUNE DRIVE SAN JOSE, CA 95131 USA

TEL + 1 (408) 944-0800 FAX + 1 (408) 474-1000 WEB http://www.micrel.com