Chipsmall

Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of "Quality Parts,Customers Priority,Honest Operation,and Considerate Service",our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

MICREL

The Infinite Bandwidth Company™

3-BIT 4:1 MUX-LATCH

SY10E156
SY100E156
FINAL

FEATURES

- **900ps max. D to output**
- **Extended 100E V_{EE} range of –4.2V to –5.5V**
- **800ps max. LEN to output**
- **Differential outputs**
- **Asynchronous Master Reset**
- **Dual latch enables**
- **Fully compatible with industry standard 10KH, 100K ECL levels**
- **Internal 75KΩ input pulldown resistors**
- **Fully compatible with Motorola MC10E/100E156**
- **Available in 28-pin PLCC package**

DESCRIPTION

The SY10/100E156 offer three 4:1 multiplexers followed by latches with differential outputs, designed for use in new, high-performance ECL systems. The two external latch enable signals (LEN_1 and LEN_2) are gated through a logical OR operation before use as control for the three latches. When both LEN_1 and LEN_2 are at a logic LOW, the latches are transparent, thus presenting the data from the multiplexers at the output pins. If either LEN_1 or LEN_2 (or both) are at a logic HIGH, the outputs are latched.
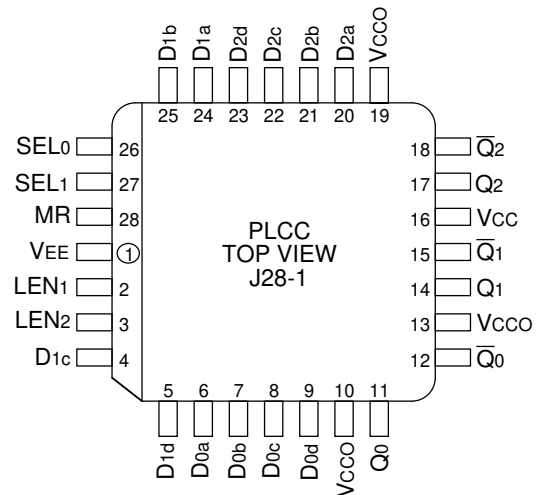
The multiplexer operation is controlled by the Select (SEL_0, SEL_1) signals which select one of the four bits of input data at each mux to be passed through.

The MR (Master Reset) signal operates asynchronously to take all outputs to a logic LOW.

BLOCK DIAGRAM
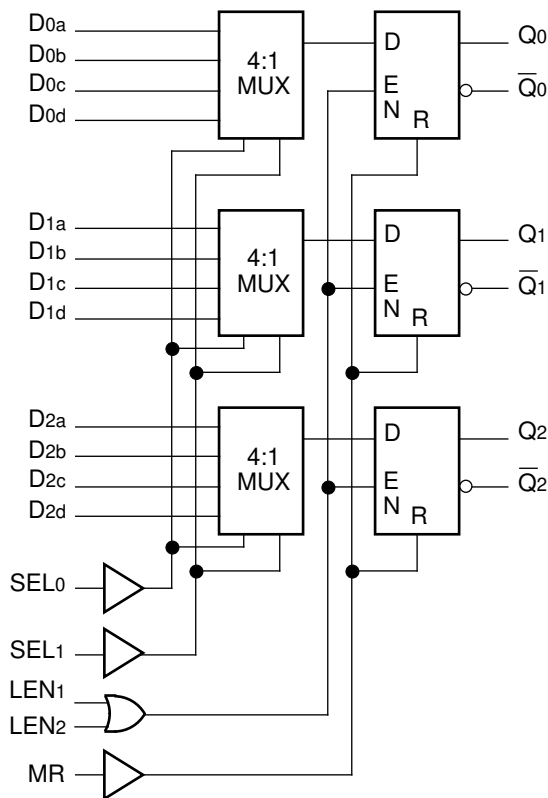
PIN CONFIGURATION

PLCC TOP VIEW J28-1

PIN NAMES

Pin	Function
D_{0x}–D_{2x}	Input Data
SEL_0, SEL_1	Select Inputs
LEN_1, LEN_2	Latch Enables
MR	Master Reset
Q_0–Q_2	True Outputs
$\overline{Q}_0$–$\overline{Q}_2$	Inverted Outputs
V_{CCO}	V_{CC} to Output

TRUTH TABLES

LEN$_1$	LEN$_2$	Latch
L	L	Transparent
H	X	Latched
X	H	Latched

SEL$_0$	SEL$_1$	Data
L	L	a
H	L	b
L	H	c
H	H	d

DC ELECTRICAL CHARACTERISTICS

$V_{EE} = V_{EE}$ (Min.) to V_{EE} (Max.); $V_{CC} = V_{CCO} = $ GND

Symbol	Parameter	$T_A = 0°C$			$T_A = +25°C$			$T_A = +85°C$			Unit	Condition
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
I_{IH}	Input HIGH Current	—	—	150	—	—	150	—	—	150	µA	—
I_{EE}	Power Supply Current										mA	—
	10E	—	75	90	—	75	90	—	75	90		
	100E	—	75	90	—	75	90	—	86	103		

AC ELECTRICAL CHARACTERISTICS

$V_{EE} = V_{EE}$ (Min.) to V_{EE} (Max.); $V_{CC} = V_{CCO} = $ GND

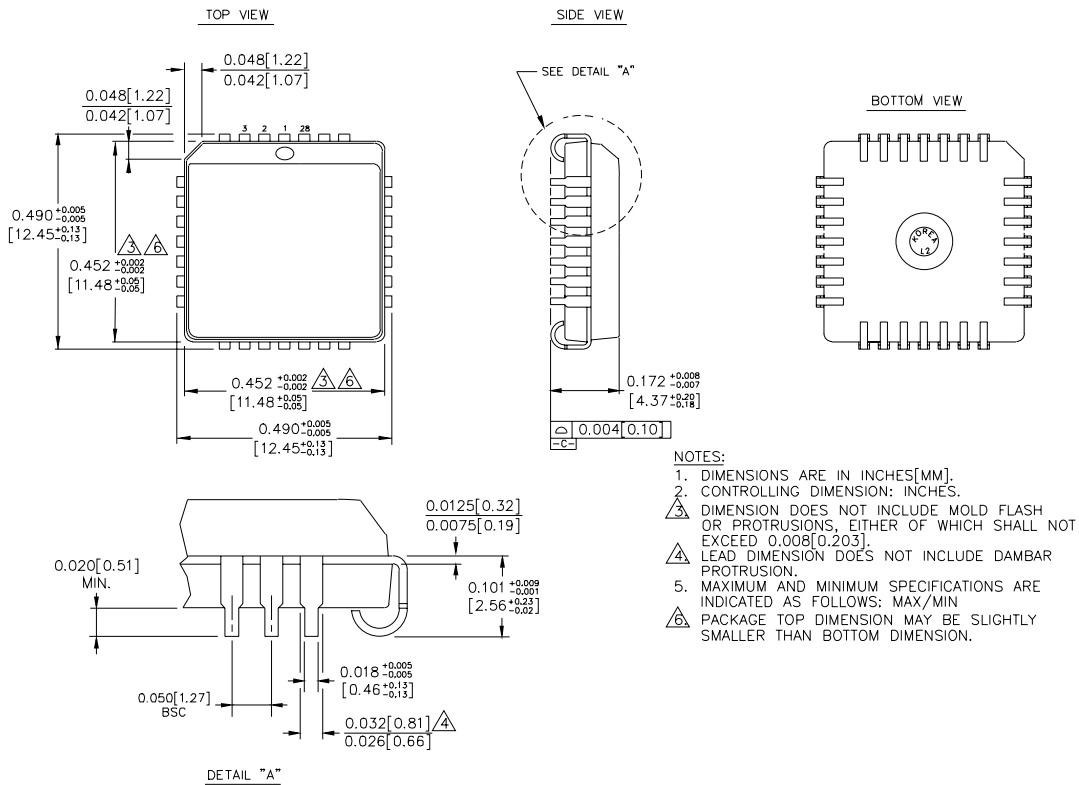| Symbol	Parameter	$T_A = 0°C$			$T_A = +25°C$			$T_A = +85°C$			Unit	Condition
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
t_{PLH} t_{PHL}	Propagation Delay to Output										ps	—
	D	400	600	900	400	600	900	400	600	900		
	SEL$_0$	550	775	1050	550	775	1050	550	775	1050		
	SEL$_1$	450	650	900	450	650	900	450	650	900		
	LEN	350	500	800	350	500	800	350	500	800		
	MR	350	600	825	350	600	825	350	600	825		
t_S	Set-up Time										ps	—
	D	400	275	—	400	275	—	400	275	—		
	SEL$_0$	700	300	—	700	300	—	700	300	—		
	SEL$_1$	600	400	—	600	400	—	600	400	—		
t_H	Hold Time										ps	—
	D	300	−275	—	300	−275	—	300	−275	—		
	SEL$_0$	100	−300	—	100	−300	—	100	−300	—		
	SEL$_1$	200	−400	—	200	−400	—	200	−400	—		
t_{RR}	Reset Recovery Time	800	600	—	800	600	—	800	600	—	ps	—
t_{PW}	Minimum Pulse Width, MR	400	—	—	400	—	—	400	—	—	ps	—
t_{skew}	Within-Device Skew	—	50	—	—	50	—	—	50	—	ps	1
t_r t_f	Rise/Fall Time 20% to 80%	275	475	700	275	475	700	275	475	700	ps	—

NOTE:

1. Within-device skew is defined as identical transitions on similar paths through a device.

PRODUCT ORDERING CODE

Ordering Code	Package Type	Operating Range
SY10E156JC	J28-1	Commercial
SY10E156JCTR	J28-1	Commercial
SY100E156JC	J28-1	Commercial
SY100E156JCTR	J28-1	Commercial

28 LEAD PLCC (J28-1)

TOP VIEW

0.048[1.22]
0.042[1.07]

0.048[1.22]
0.042[1.07]

3 2 1 28

0.490 +0.005 −0.005
[12.45 +0.13 −0.13]

0.452 +0.002 −0.002
[11.48 +0.05 −0.05] △3 △6

0.452 +0.002 −0.002
[11.48 +0.05 −0.05] △3 △6

0.490 +0.005 −0.005
[12.45 +0.13 −0.13]

SIDE VIEW

SEE DETAIL "A"

0.172 +0.008 −0.007
[4.37 +0.20 −0.18]

⌀ 0.004[0.10]
−C−

BOTTOM VIEW

DETAIL "A"

0.020[0.51]
MIN.

0.0125[0.32]
0.0075[0.19]

0.101 +0.009 −0.001
[2.56 +0.23 −0.02]

0.018 +0.005 −0.005
[0.46 +0.13 −0.13]

0.050[1.27]
BSC

0.032[0.81] △4
0.026[0.66]

NOTES:
1. DIMENSIONS ARE IN INCHES[MM].
2. CONTROLLING DIMENSION: INCHES.
△3 DIMENSION DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS, EITHER OF WHICH SHALL NOT EXCEED 0.008[0.203].
△4 LEAD DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION.
5. MAXIMUM AND MINIMUM SPECIFICATIONS ARE INDICATED AS FOLLOWS: MAX/MIN
△6 PACKAGE TOP DIMENSION MAY BE SLIGHTLY SMALLER THAN BOTTOM DIMENSION.

Rev. 03