Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

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FEATURES

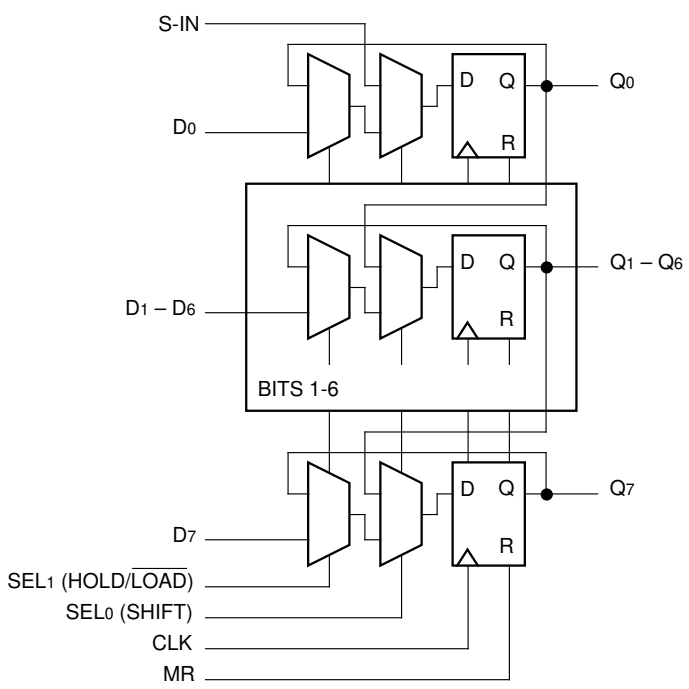
- **1000ps max. CLK to output**
- **Extended 100E VEE range of –4.2V to –5.5V**
- **SHIFT overrides HOLD, /LOAD control**
- **Asynchronous Master Reset**
- **Pin-compatible with E141**
- **Fully compatible with industry standard 10KH, 100K ECL levels**
- **Internal 75KΩ input pulldown resistors**
- **Fully compatible with Motorola MC10E/100E241**
- **Available in 28-pin PLCC package**

DESCRIPTION

The SY10/100E241 are 8-bit shiftable registers designed for use in new, high-performance ECL systems. Unlike the E141, the E241 features internal data feedback organized such that the SHIFT control overrides the HOLD, /LOAD control. Thus, the normal operations of HOLD and LOAD can be toggled with a single control line without the need for external gating. This configuration also enables switching to scan mode with the single SHIFT control line.

The eight inputs D_0–D_7 accept parallel input data, while S-IN accepts serial input data when in shift mode. Data is accepted a set-up time before the rising edge of CLK. Shifting is also accomplished on the rising clock edge. A HIGH on the Master Reset pin (MR) asychronously resets all the registers to zero.

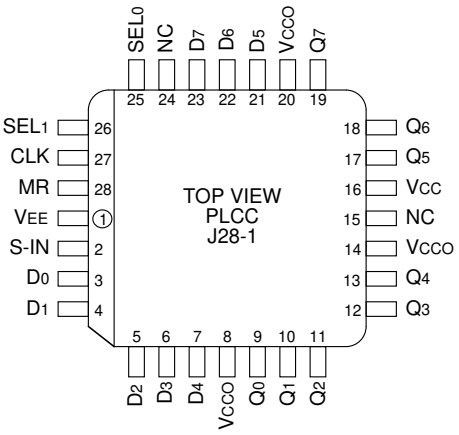
BLOCK DIAGRAM



PIN NAMES

Pin	Function
D_0–D_7	Parallel Data Inputs
S-IN	Serial Data Input
SEL_0	SHIFT Control
SEL_1	HOLD, /LOAD Control
CLK	Clock
MR	Master Reset
Q_0–Q_7	Data Outputs
V_{CCO}	V_{CC} to Output

PACKAGE/ORDERING INFORMATION



28-Pin PLCC (J28-1)

Ordering Information[1]

Part Number	Package Type	Operating Range	Package Marking	Lead Finish
SY10E241JC	J28-1	Commercial	SY10E241JC	Sn-Pb
SY10E241JCTR[2]	J28-1	Commercial	SY10E241JC	Sn-Pb
SY100E241JC	J28-1	Commercial	SY100E241JC	Sn-Pb
SY100E241JCTR[2]	J28-1	Commercial	SY100E241JC	Sn-Pb
SY10E241JZ[3]	J28-1	Commercial	SY10E241JZ with Pb-Free bar-line indicator	Matte-Sn
SY10E241JZTR[2, 3]	J28-1	Commercial	SY10E241JZ with Pb-Free bar-line indicator	Matte-Sn
SY100E241JZ[3]	J28-1	Commercial	SY100E241JZ with Pb-Free bar-line indicator	Matte-Sn
SY100E241JZTR[2, 3]	J28-1	Commercial	SY100E241JZ with Pb-Free bar-line indicator	Matte-Sn

Notes:

1. Contact factory for die availability. Dice are guaranteed at $T_A = 25°C$, DC Electricals only.
2. Tape and Reel.
3. Pb-Free package is recommended for new designs.

TRUTH TABLE

SEL_0	SEL_1	Function
L	L	Load
L	H	Hold
H	X	Shift (D_n to D_{n+1})

DC ELECTRICAL CHARACTERISTICS

V_{EE} = V_{EE} (Min.) to V_{EE} (Max.); V_{CC} = V_{CCO} = GND

Symbol	Parameter	T_A = 0°C			T_A = +25°C			T_A = +85°C			Unit	Condition
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
I_{IH}	Input HIGH Current	—	—	150	—	—	150	—	—	150	µA	—
I_{EE}	Power Supply Current										mA	—
	10E	—	125	150	—	125	150	—	125	150		
	100E	—	125	150	—	125	150	—	144	173		

AC ELECTRICAL CHARACTERISTICS

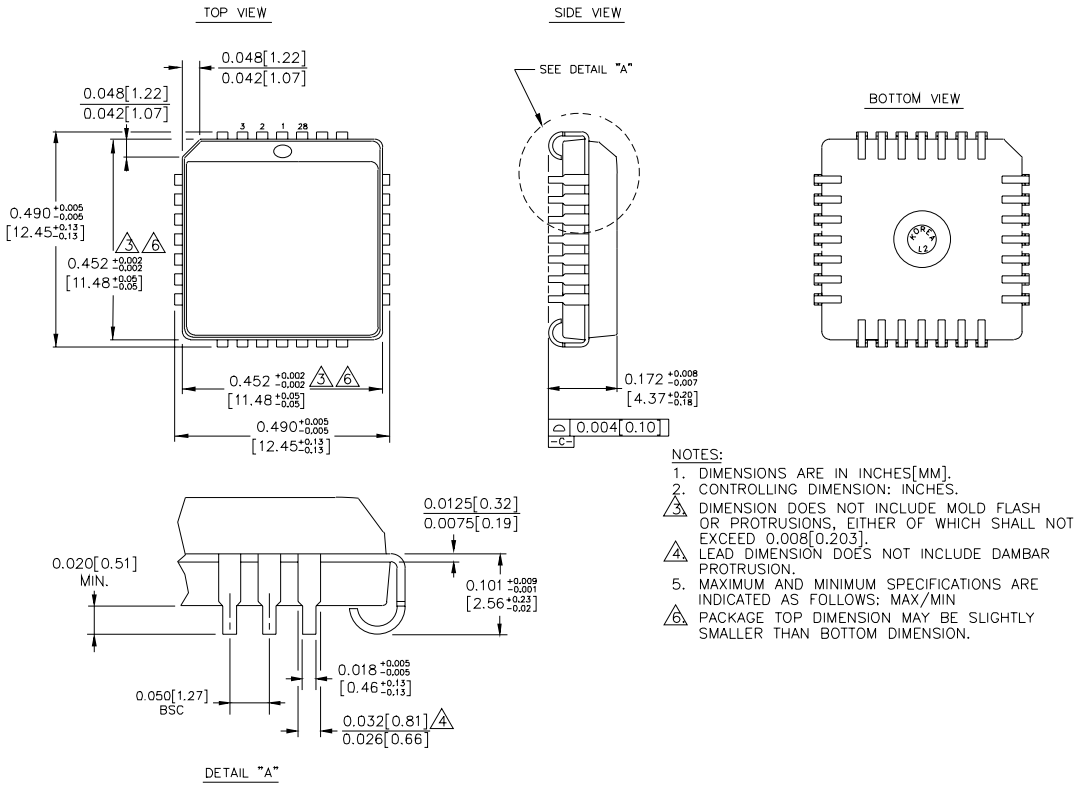
V_{EE} = V_{EE} (Min.) to V_{EE} (Max.); V_{CC} = V_{CCO} = GND

Symbol	Parameter	T_A = 0°C			T_A = +25°C			T_A = +85°C			Unit	Condition
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
f_{SHIFT}	Max. Shift Frequency	700	900	—	700	900	—	700	900	—	MHz	—
t_{PD}	Propagation Delay to Output										ps	—
	CLK	625	750	975	625	750	975	625	750	975		
	MR	600	725	975	600	725	975	600	725	975		
t_S	Set-up Time										ps	—
	D	175	25	—	175	25	—	175	25	—		
	SEL_0 (SHIFT)350	200	—	350	200	—	350	200	—			
	SEL_1 (HOLD/$\overline{LOAD}$)	400	250	—	400	250	—	400	250	—		
	S-IN	125	–100	—	125	–100	—	125	–100	—		
t_H	Hold Time										ps	—
	D	200	–25	—	200	–25	—	200	–25	—		
	SEL_0 (SHIFT)	100	–200	—	100	–200	—	100	–200	—		
	SEL_1 (HOLD/$\overline{LOAD}$)	50	–250	—	50	–250	—	50	–250	—		
	S-IN	300	100	—	300	100	—	300	100	—		
t_{RR}	Reset Recovery Time	900	600	—	900	600	—	900	600	—	ps	—
t_{PW}	Minimum Pulse Width CLK, MR	400	—	—	400	—	—	400	—	—	ps	—
t_{skew}	Within-Device Skew	—	60	—	—	60	—	—	60	—	ps	1
t_r t_f	Rise/Fall Time 20% to 80%	300	525	800	300	525	800	300	525	800	ps	—

Note:

1. Within-device skew is defined as identical transitions on similar paths through a device.

28-PIN PLCC (J28-1)



NOTES:
1. DIMENSIONS ARE IN INCHES[MM].
2. CONTROLLING DIMENSION: INCHES.
3. DIMENSION DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS, EITHER OF WHICH SHALL NOT EXCEED 0.008[0.203].
4. LEAD DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION.
5. MAXIMUM AND MINIMUM SPECIFICATIONS ARE INDICATED AS FOLLOWS: MAX/MIN
6. PACKAGE TOP DIMENSION MAY BE SLIGHTLY SMALLER THAN BOTTOM DIMENSION.

Rev. 03

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