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# 6-BIT REGISTER DIFFERENTIAL DATA CLOCK

**SY10E451**
**SY100E451**

## FEATURES

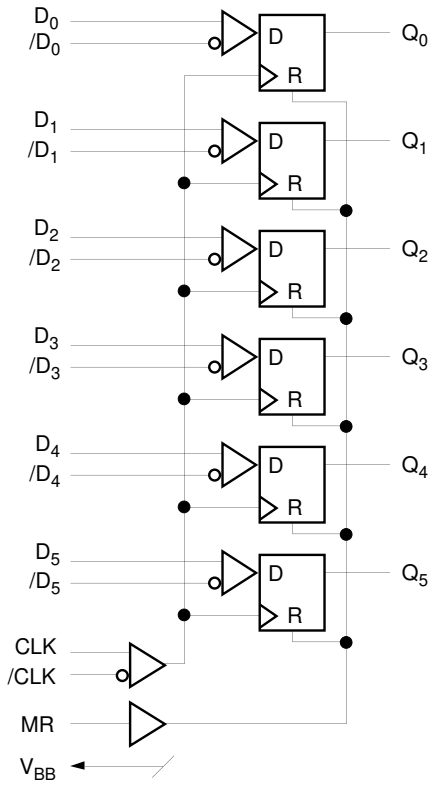
- **1100MHz min. toggle frequency**
- **Extended 100E $V_{EE}$ range of –4.2V to –5.5V**
- **Differential inputs: data and clock**
- **$V_{BB}$ output for single-ended use**
- **Asynchronous Master Reset**
- **Fully compatible with industry standard 10KH, 100K ECL levels**
- **Internal 75KΩ input pulldown resistors**
- **Fully compatible with Motorola MC10E/100E451**
- **Available in 28-pin PLCC package**

## DESCRIPTION

The SY10/100E451 offer six D-type flip-flops with single-ended outputs and differential data and clock inputs, designed for use in new, high-performance ECL systems. The registers are triggered by the rising edge of the CLK input.

A logic HIGH on the Master Reset (MR) input resets all outputs to a logic LOW. The $V_{BB}$ output is provided for use as a reference voltage for single-ended reception of ECL signals to that device only. When used for this purpose, it is recommended that $V_{BB}$ is decoupled to $V_{CC}$ via a 0.01µF capacitor.

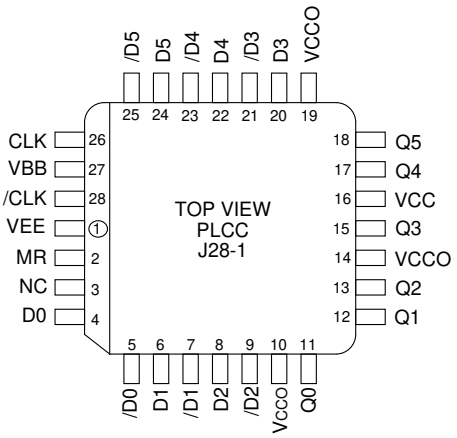
## BLOCK DIAGRAM




## PIN NAMES

| Pin | Function |
|---|---|
| D0–D5 | + Data Input |
| /D0–/D5 | – Data Input |
| CLK | + Clock Input |
| /CLK | – Clock Input |
| Q0–Q5 | Data Outputs |
| MR | Master Reset Input |
| $V_{BB}$ | $V_{BB}$ Output |
| $V_{CCO}$ | $V_{CC}$ to Output |

## PACKAGE/ORDERING INFORMATION




**28-Pin PLCC (J28-1)**

## Ordering Information[1]

| Part Number | Package Type | Operating Range | Package Marking | Lead Finish |
|---|---|---|---|---|
| SY10E451JI | J28-1 | Industrial | SY10E451JI | Sn-Pb |
| SY10E451JITR[2] | J28-1 | Industrial | SY10E451JI | Sn-Pb |
| SY100E451JI | J28-1 | Industrial | SY100E451JI | Sn-Pb |
| SY100E451JITR[2] | J28-1 | Industrial | SY100E451JI | Sn-Pb |
| SY10E451JC | J28-1 | Commercial | SY10E451JC | Sn-Pb |
| SY10E451JCTR[2] | J28-1 | Commercial | SY10E451JC | Sn-Pb |
| SY100E451JC | J28-1 | Commercial | SY100E451JC | Sn-Pb |
| SY100E451JCTR[2] | J28-1 | Commercial | SY100E451JC | Sn-Pb |
| SY10E451JY[3] | J28-1 | Industiral | SY10E451JY with Pb-Free bar-line indicator | Matte-Sn |
| SY10E451JYTR[2, 3] | J28-1 | Industrial | SY10E451JY with Pb-Free bar-line indicator | Matte-Sn |
| SY100E451JY[3] | J28-1 | Industrial | SY100E451JY with Pb-Free bar-line indicator | Matte-Sn |
| SY100E451JYTR[2, 3] | J28-1 | Industrial | SY100E451JY with Pb-Free bar-line indicator | Matte-Sn |

**Notes:**

1. Contact factory for die availability. Dice are guaranteed at $T_A$ = 25°C, DC Electricals only.
2. Tape and Reel.
3. Pb-Free package is recommended for new designs.

## DC ELECTRICAL CHARACTERISTICS

$V_{EE} = V_{EE}$ (Min.) to $V_{EE}$ (Max.); $V_{CC} = V_{CCO}$ = GND

| Symbol | Parameter | $T_A$ = –40°C | | | $T_A$ = 0°C | | | $T_A$ = 25°C | | | $T_A$ = +85°C | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | Min. | Typ. | Max. | Min. | Typ. | Max. | Min. | Typ. | Max. | |
| $V_{BB}$ | Output Reference 10E | | | | –1.38 | — | –1.27 | –1.35 | — | –1.25 | –1.31 | — | –1.19 | V |
| | Voltage 100E | | | | –1.38 | — | –1.26 | –1.38 | — | –1.26 | –1.38 | — | –1.26 | |
| $I_{IH}$ | Input HIGH Current | | | | — | — | 150 | — | — | 150 | — | — | 150 | µA |
| $I_{EE}$ | Power Supply 10E | | | | — | 84 | 101 | — | 84 | 101 | — | 84 | 101 | mA |
| | Current 100E | | | | — | 84 | 101 | — | 84 | 101 | — | 97 | 116 | |
| $V_{CMR}$ | Common Mode Range(1) | | | | –2.0 | — | –0.4 | –2.0 | — | –0.4 | –2.0 | — | –0.4 | V |

**Note:**

1. $V_{CMR}$ is referenced to the most psitive side of the differential input signal. Normal operation is obtained when the "HIGH" input is within the $V_{CMR}$ range and the input swing is greater than $V_{PP}$ (min) and < 1V.

## AC ELECTRICAL CHARACTERISTICS

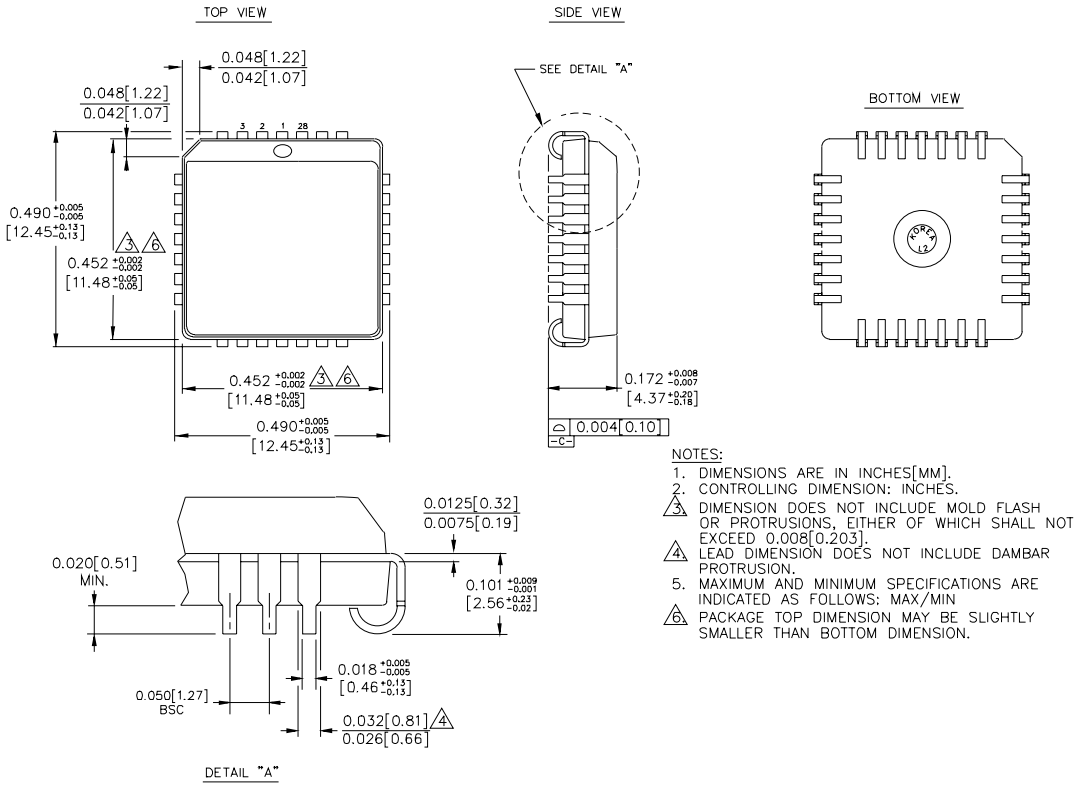
$V_{EE} = V_{EE}$ (Min.) to $V_{EE}$ (Max.); $V_{CC} = V_{CCO}$ = GND

| Symbol | Parameter | $T_A$ = –40°C | | | $T_A$ = 0°C | | | $T_A$ = 25°C | | | $T_A$ = +85°C | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | Min. | Typ. | Max. | Min. | Typ. | Max. | Min. | Typ. | Max. | |
| $f_{MAX}$ | Max. Toggle Frequency | | | | 1100 | 1400 | — | 1100 | 1400 | — | 1100 | 1400 | — | MHz |
| $t_{PD}$ | Propagation Delay to Output CLK (Diff) | | | | 475 | 650 | 800 | 475 | 650 | 800 | 475 | 650 | 800 | ps |
| | CLK (SE) | | | | 425 | 650 | 850 | 425 | 650 | 850 | 425 | 650 | 850 | |
| | MR | | | | 425 | 600 | 850 | 425 | 600 | 850 | 425 | 600 | 850 | |
| $t_S$ | Set-up Time D | | | | 150 | –100 | — | 150 | –100 | — | 150 | –100 | — | ps |
| $t_H$ | Hold Time D | | | | 250 | 100 | — | 250 | 100 | — | 250 | 100 | — | ps |
| $V_{PP\ (AC)}$ | Minimum Input Swing(1) | | | | 150 | — | — | 150 | — | — | 150 | — | — | mV |
| $t_{RR}$ | Reset Recovery Time | | | | 750 | 600 | — | 750 | 600 | — | 750 | 600 | — | ps |
| $t_{PW}$ | Minimum Pulse Width CLK, MR | | | | 400 | — | — | 400 | — | — | 400 | — | — | ps |
| $t_{skew}$ | Within-Device Skew(2) | | | | — | 100 | — | — | 100 | — | — | 100 | — | ps |
| $t_r$ $t_f$ | Rise/Fall Time 20% to 80% | | | | 275 | 450 | 800 | 275 | 450 | 800 | 275 | 450 | 800 | ps |

**Notes:**

1. Minimum input voltage for which AC parameters are guaranteed.
2. Within-device skew is defined as identical transitions on similar paths through a device.

## 28-PIN PLCC (J28-1)




NOTES:
1. DIMENSIONS ARE IN INCHES[MM].
2. CONTROLLING DIMENSION: INCHES.
3. DIMENSION DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS, EITHER OF WHICH SHALL NOT EXCEED 0.008[0.203].
4. LEAD DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION.
5. MAXIMUM AND MINIMUM SPECIFICATIONS ARE INDICATED AS FOLLOWS: MAX/MIN
6. PACKAGE TOP DIMENSION MAY BE SLIGHTLY SMALLER THAN BOTTOM DIMENSION.

Rev. 03

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