Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

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TRIPLE 4-INPUT MULTIPLEXER WITH ENABLE

SY100S371

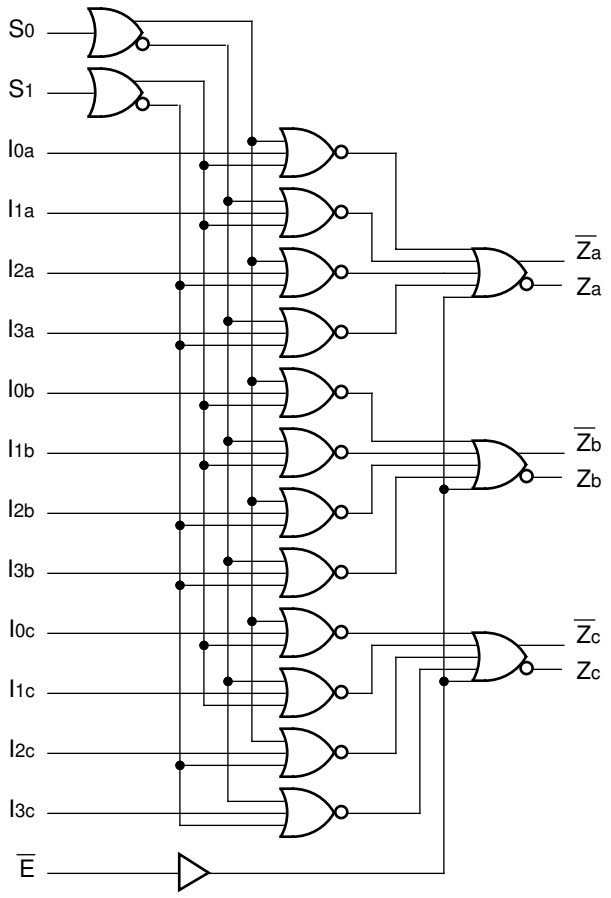
FEATURES

- **Max. propagation delay of 1000ps**
- **I_{EE} min. of –68mA**
- **Industry standard 100K ECL levels**
- **Extended supply voltage option: V_{EE} = –4.2V to –5.5V**
- **Voltage and temperature compensation for improved noise immunity**
- **Internal 75KΩ input pull-down resistors**
- **40% faster than Fairchild**
- **40% lower power than Fairchild**
- **Function and pinout compatible with Fairchild F100K**
- **Available in 24-pin CERPACK and 28-pin PLCC packages**

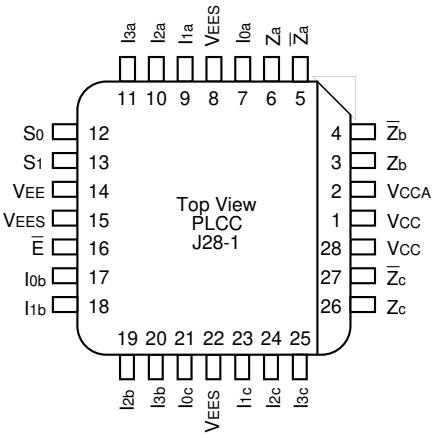
DESCRIPTION

The SY100S371 is an ultra-fast triple 4-input multiplexer with true and complementary outputs designed for use in high-performance ECL systems. The multiplexer is controlled by common select inputs S_0 and S_1. A logic HIGH on the Enable ($\overline{E}$) control input takes the outputs to a logic LOW. The inputs on the device have 75KΩ pull-down resistors.

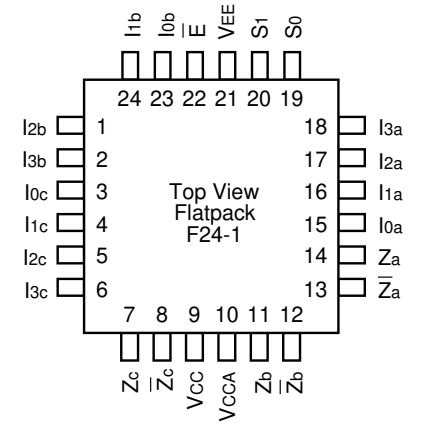
BLOCK DIAGRAM



PACKAGE/ORDERING INFORMATION



28-Pin PLCC (J28-1)



24-Pin Cerpack (F24-1)

Ordering Information

Part Number	Package Type	Operating Range	Package Marking	Lead Finish
SY100S371FC	F24-1	Commercial	SY100S371FC	Sn-Pb
SY100S371FCTR[1]	F24-1	Commercial	SY100S371FC	Sn-Pb
SY100S371JC	J28-1	Commercial	SY100S371JC	Sn-Pb
SY100S371JCTR[1]	J28-1	Commercial	SY100S371JC	Sn-Pb
SY100S371JZ[2]	J28-1	Commercial	SY100S371JZ with Pb-Free bar-line indicator	Matte-Sn
SY100S371JZTR[1, 2]	J28-1	Commercial	SY100S371JZ with Pb-Free bar-line indicator	Matte-Sn

Notes:

1. Tape and Reel.
2. Pb-Free package is recommended for new designs.

PIN NAMES

Pin	Function
$I_{0X} – I_{3X}$	Data Inputs (x = a, b or c)
S_0, S_1	Select Inputs
$\overline{E}$	Enable Input (Active LOW)
$Z_a – Z_c$	Data Outputs
$\overline{Z}_a – \overline{Z}_c$	Complementary Data Outputs
V_{EES}	V_{EE} Substrate
V_{CCA}	V_{CCO} for ECL Outputs

TRUTH TABLE(1)

Inputs			Outputs
$\overline{E}$	S_0	S_1	Z_n
L	L	L	I_{0X}
L	H	L	I_{1X}
L	L	H	I_{2X}
L	H	H	I_{3X}
H	X	X	L

NOTE:

1. H = HIGH Voltage Level
   L = LOW Voltage Level
   X = Don't Care

DC ELECTRICAL CHARACTERISTICS

V_{EE} = –4.2V to –5.5V unless otherwise specified; $V_{CC} = V_{CCA}$ = GND

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
I_{IH}	Input HIGH Current				µA	$V_{IN} = V_{IH}$ (Max.)
	$I_{0X} – I_{3X}$	—	—	250		
	S_0, S_1, $\overline{E}$	—	—	300		
I_{EE}	Power Supply Current	–68	–48	–34	mA	Inputs Open

AC ELECTRICAL CHARACTERISTICS

CERPACK

V_{EE} = –4.2V to –5.5V unless otherwise specified; V_{CC} = V_{CCA} = GND

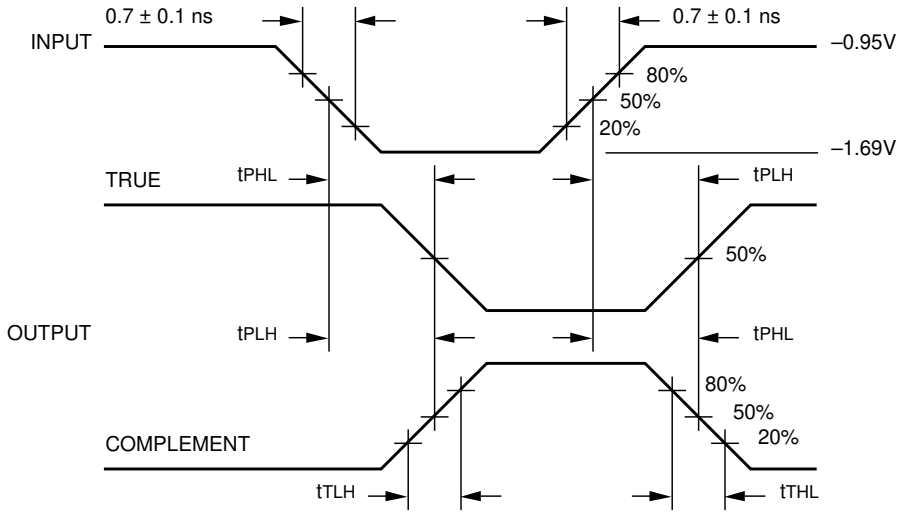
Symbol	Parameter	T_A = 0°C		T_A = +25°C		T_A = +85°C		Unit	Condition
		Min.	Max.	Min.	Max.	Min.	Max.		
t_{PLH} t_{PHL}	Propagation Delay I_{0X} – I_{3X} to Output	300	1100	300	1100	300	1100	ps	
t_{PLH} t_{PHL}	Propagation Delay S_0, S_1 to Output	400	1500	400	1500	400	1500	ps	
t_{PLH} t_{PHL}	Propagation Delay $\overline{S}_0$, S_1 to Output	400	1400	400	1400	400	1400	ps	
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	300	900	300	900	300	900	ps	

PLCC

V_{EE} = –4.2V to –5.5V unless otherwise specified; V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_A = 0°C		T_A = +25°C		T_A = +85°C		Unit	Condition
		Min.	Max.	Min.	Max.	Min.	Max.		
t_{PLH} t_{PHL}	Propagation Delay I_{0X} – I_{3X} to Output	300	1000	300	1000	300	1000	ps	
t_{PLH} t_{PHL}	Propagation Delay S_0, S_1 to Output	400	1400	400	1400	400	1400	ps	
t_{PLH} t_{PHL}	Propagation Delay $\overline{S}_0$, S_1 to Output	400	1300	400	1300	400	1300	ps	
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	300	900	300	900	300	900	ps	

TIMING DIAGRAM

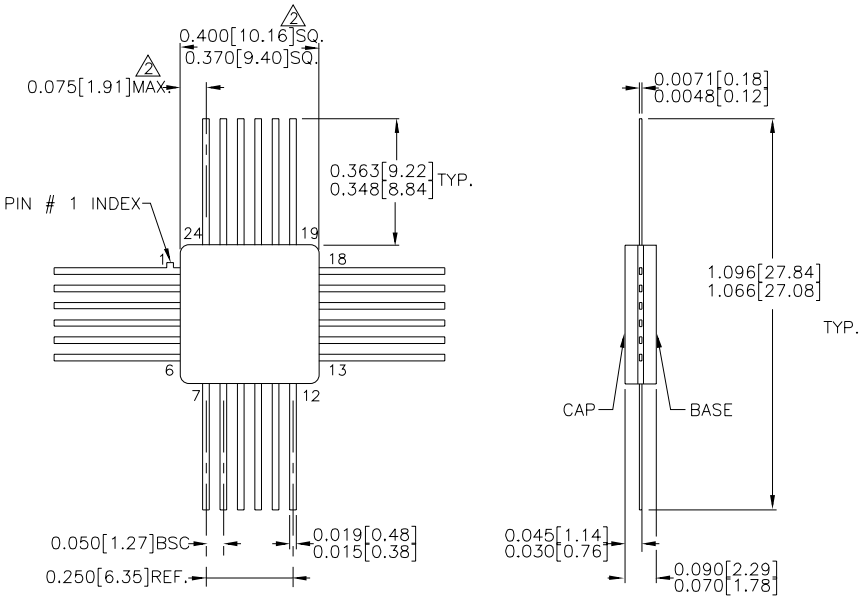


Propagation Delay and Transition Times

Note:

V_{EE} = –4.2V to –5.5V unless otherwise specified; V_{CC} = V_{CCA} = GND

24-PIN CERPACK (F24-1)



NOTES:
1. DIMENSIONS ARE IN INCHES[MM].
2. THIS DIMENSION INCLUDES GLASS PROTRUSION AND CAP TO BASE ALIGNMENT TOLERANCES.
3. DIMENSIONS SHOWN ARE MAX/MIN, WHERE NOTED.

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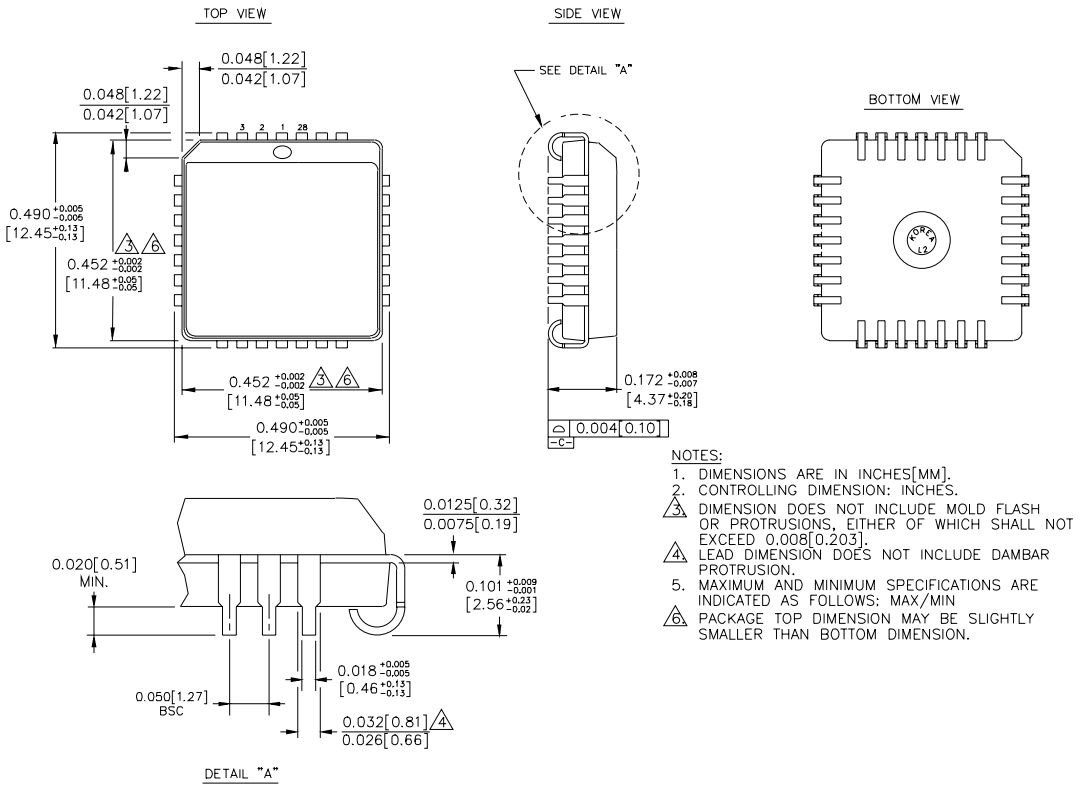
28-PIN PLCC (J28-1)



NOTES:
1. DIMENSIONS ARE IN INCHES[MM].
2. CONTROLLING DIMENSION: INCHES.
3. DIMENSION DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS, EITHER OF WHICH SHALL NOT EXCEED 0.008[0.203].
4. LEAD DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION.
5. MAXIMUM AND MINIMUM SPECIFICATIONS ARE INDICATED AS FOLLOWS: MAX/MIN
6. PACKAGE TOP DIMENSION MAY BE SLIGHTLY SMALLER THAN BOTTOM DIMENSION.

Rev. 03

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