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FEATURES

- ☒ 750ps max. LEN to output
- ☒ Extended 100E VEE range of -4.2V to -5.5V
- ☒ 700ps max. D to output
- ☒ Single-ended outputs
- ☒ Asynchronous Master Reset
- ☒ Dual latch-enables
- ☒ Fully compatible with industry standard 10KH, 100K ECL levels
- ☒ Internal 75KΩ input pulldown resistors
- ☒ Fully compatible with Motorola MC10E/100E155
- ☒ Available in 28-pin PLCC package

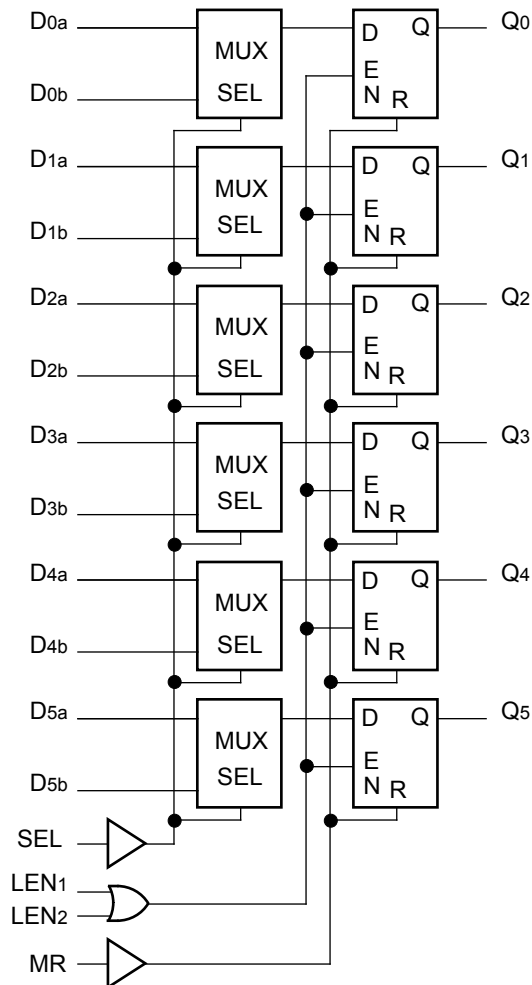
DESCRIPTION

The SY10/100E155 offer six 2:1 multiplexers followed by latches with single-ended outputs, designed for use in new, high-performance ECL systems. The two external latch-enable signals (LEN1 and LEN2) are gated through a logical OR operation before use as control for the six latches. When both LEN1 and LEN2 are at a logic LOW, the latches are transparent, thus presenting the data from the multiplexers at the output pins. If either LEN1 or LEN2 (or both) are at a logic HIGH, the outputs are latched.

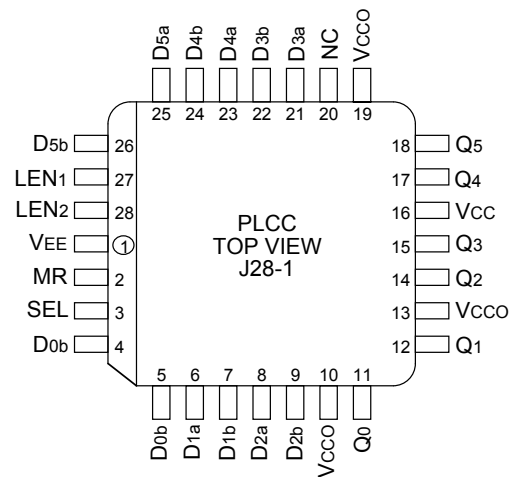
The multiplexer operation is controlled by the SEL (Select) signal which selects one of the two bits of input data at each mux to be passed through.

The MR (Master Reset) signal operates asynchronously to take all outputs to a logic LOW.

BLOCK DIAGRAM



PIN CONFIGURATION



PIN NAMES

Pin	Function
D0a-D5a	Input Data a
D0b-D5b	Input Data b
SEL	Data Select Input
LEN1, LEN2	Latch Enables
MR	Master Reset
Q0-Q5	Outputs
VCCO	Vcc to Output

TRUTH TABLES

SEL	Data
H	a
L	b

LEN1	LEN2	Latch
L	L	Transparent
H	X	Latched
X	H	Latched

DC ELECTRICAL CHARACTERISTICS

V_{EE} = V_{EE} (Min.) to V_{EE} (Max.); V_{CC} = V_{CCO} = GND

Symbol	Parameter	T _A = 0°C			T _A = +25°C			T _A = +85°C			Unit	Condition	
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.			
I _{IH}	Input HIGH Current	—	—	150	—	—	150	—	—	150	μA	—	
I _{EE}	Power Supply Current	—	85	102	—	85	102	—	85	102	mA	—	
		10E	—	85	102	—	85	102	—	85			102
		100E	—	85	102	—	85	102	—	98			117

AC ELECTRICAL CHARACTERISTICS

V_{EE} = V_{EE} (Min.) to V_{EE} (Max.); V_{CC} = V_{CCO} = GND

Symbol	Parameter	T _A = 0°C			T _A = +25°C			T _A = +85°C			Unit	Condition
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
t _{PLH} t _{PHL}	Propagation Delay to Output D SEL LEN MR	325 475 350 450	500 675 500 600	700 925 750 850	325 475 350 450	500 675 500 600	700 925 750 850	325 475 350 450	500 675 500 600	700 925 750 850	ps	—
t _s	Set-up Time D SEL	300 500	100 250	— —	300 500	100 250	— —	300 500	100 250	— —	ps	—
		300 0	-100 -250	— —	300 0	-100 -250	— —	300 0	-100 -250	— —	ps	—
t _{RR}	Reset Recovery Time	800	650	—	800	650	—	800	650	—	ps	—
t _{PW}	Minimum Pulse Width, MR	400	—	—	400	—	—	400	—	—	ps	—
t _{skew}	Within-Device Skew	—	75	—	—	75	—	—	75	—	ps	1
t _r t _f	Rise/Fall Time 20% to 80%	300	450	800	300	450	800	300	450	800	ps	—

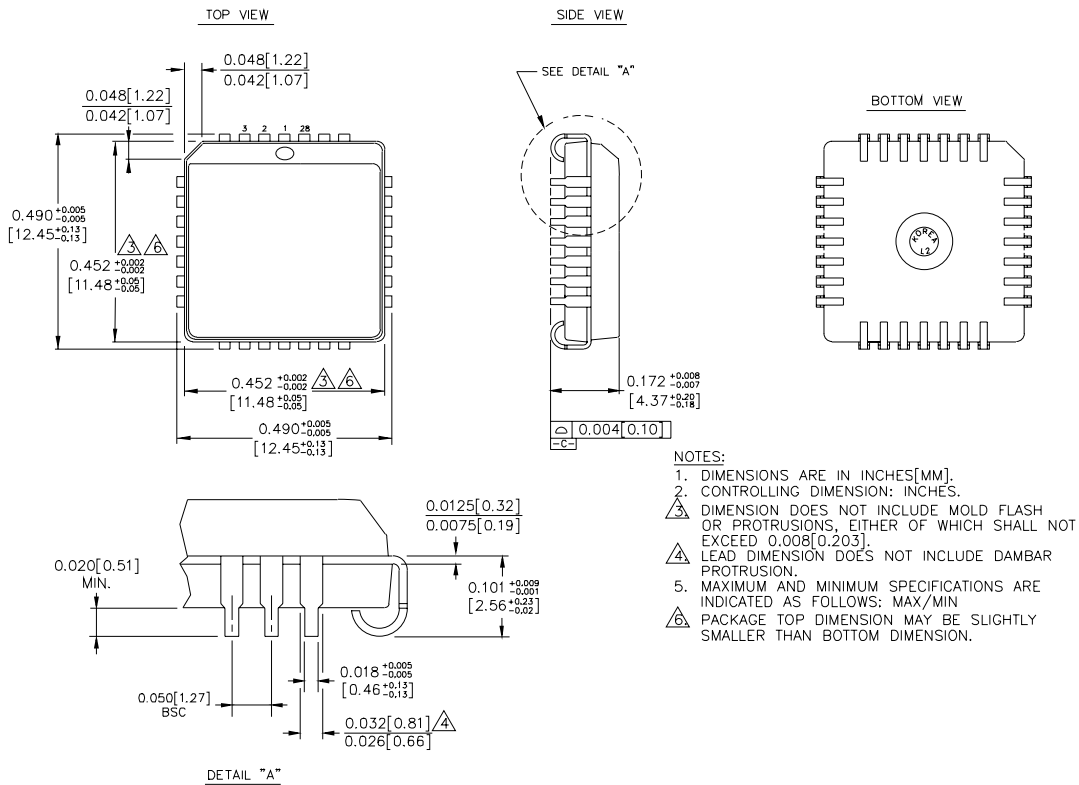
NOTE:

1. Within-device skew is defined as identical transitions on similar paths through a device.

PRODUCT ORDERING CODE

Ordering Code	Package Type	Operating Range
SY10E155JZ	J28-1	Commercial
SY10E155JZTR	J28-1	Commercial
SY100E155JZ	J28-1	Commercial
SY100E155JZTR	J28-1	Commercial

28 LEAD PLCC (J28-1)



Rev. 03

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