



Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!



## Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832

Email & Skype: info@chipsmall.com Web: www.chipsmall.com

Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China



## FEATURES

- 1000MHz min. operating frequency
- Extended 100E VEE range of -4.2V to -5.5V
- 800ps max. clock to output
- Single-ended outputs
- Asynchronous Master Reset
- Dual clocks
- Fully compatible with industry standard 10KH, 100K ECL levels
- Internal 75KΩ input pulldown resistors
- ESD protection of 2000V
- Fully compatible with Motorola MC10E/100E167
- Available in 28-pin PLCC package

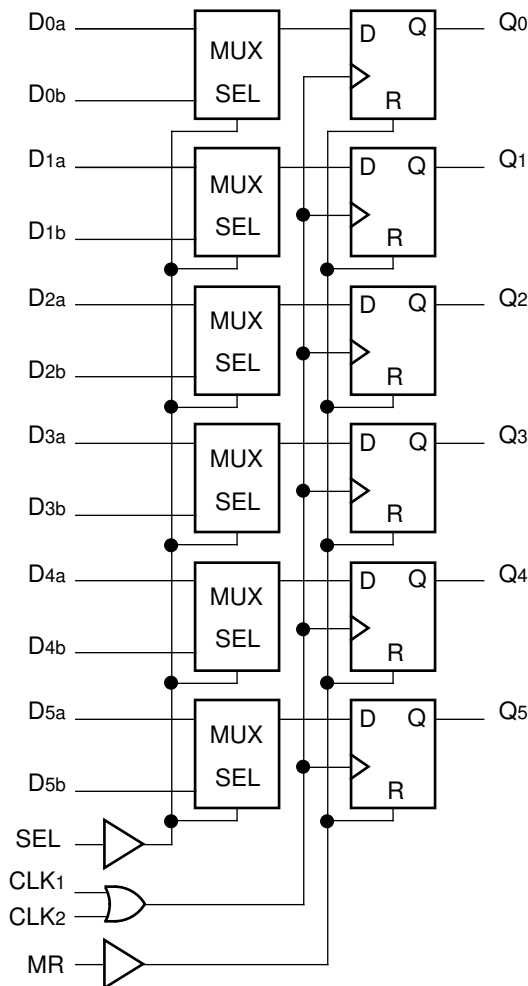
## DESCRIPTION

The SY10/100E167 offer six 2:1 multiplexers followed by D flip-flops with single-ended outputs, designed for use in new, high-performance ECL systems. The Select (SEL) control allows one of the two data inputs to the multiplexer to pass through. The two external clock signals (CLK1, CLK2) are gated through a logical OR operation before use as control for the six flip-flops. The selected data are transferred to the flip-flops on the rising edge of CLK1 or CLK2 (or both).

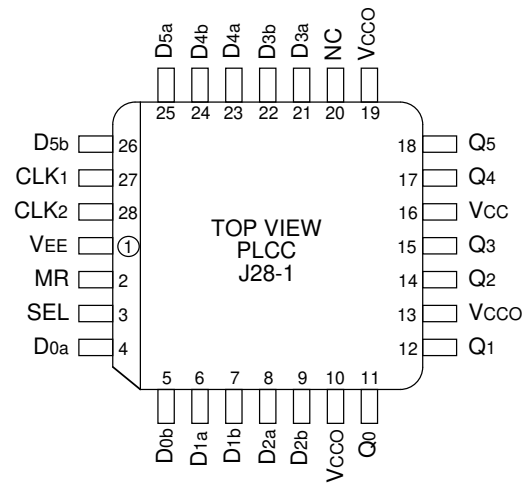
The multiplexer operation is controlled by the Select (SEL) signal which selects one of the two bits of input data at each mux to be passed through.

When a logic HIGH is applied to the Master Reset (MR) signal, it operates asynchronously to take all outputs Q to a logic LOW.

## BLOCK DIAGRAM



## PIN CONFIGURATION



## PIN NAMES

Pin	Function
D0a-D5a	Input Data a
D0b-D5b	Input Data b
SEL	Select Input
CLK1, CLK2	Clock Inputs
MR	Master Reset
Q0-Q5	Data Outputs
VCC0	Vcc to Output

## TRUTH TABLE

SEL	Data
H	a
L	b

## DC ELECTRICAL CHARACTERISTICS

VEE = VEE (Min.) to VEE (Max.); VCC = VCCO = GND

Symbol	Parameter	TA = 0°C			TA = +25°C			TA = +85°C			Unit	Condition	
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.			
I <sub>IH</sub>	Input HIGH Current	—	—	150	—	—	150	—	—	150	μA	—	
I <sub>EE</sub>	Power Supply Current	—	94	113	—	94	113	—	94	113	mA	—	
		10E	—	94	113	—	94	113	—	94			113
		100E	—	94	113	—	94	113	—	108			130

## AC ELECTRICAL CHARACTERISTICS

VEE = VEE (Min.) to VEE (Max.); VCC = VCCO = GND

Symbol	Parameter	TA = 0°C			TA = +25°C			TA = +85°C			Unit	Condition
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
f <sub>MAX</sub>	Max. Toggle Frequency	1000	1400	—	1000	1400	—	1000	1400	—	MHz	—
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay to Output CLK MR	450 450	650 650	800 850	450 450	650 650	800 850	450 450	650 650	800 850	ps	—
t <sub>s</sub>	Set-up Time D SEL	100 275	-50 125	— —	100 275	-50 125	— —	100 275	-50 125	— —	ps	—
		300 75	50 -125	— —	300 75	50 -125	— —	300 75	50 -125	— —	ps	—
t <sub>rr</sub>	Reset Recovery Time	750	550	—	750	550	—	750	550	—	ps	—
t <sub>pw</sub>	Minimum Pulse Width CLK, MR	400	—	—	400	—	—	400	—	—	ps	—
t <sub>skew</sub>	Within-Device Skew	—	75	—	—	75	—	—	75	—	ps	1
t <sub>r</sub> t <sub>f</sub>	Rise/Fall Time 20% to 80%	300	450	800	300	450	800	300	450	800	ps	—

### NOTE:

1. Within-device skew is defined as identical transitions on similar paths through a device.

## PRODUCT ORDERING CODE

Ordering Code	Package Type	Operating Range
SY10E167JC	J28-1	Commercial
SY10E167JCTR	J28-1	Commercial
SY100E167JC	J28-1	Commercial
SY100E167JCTR	J28-1	Commercial

**28 LEAD PLASTIC LEADED CHIP CARRIER (J28-1)**

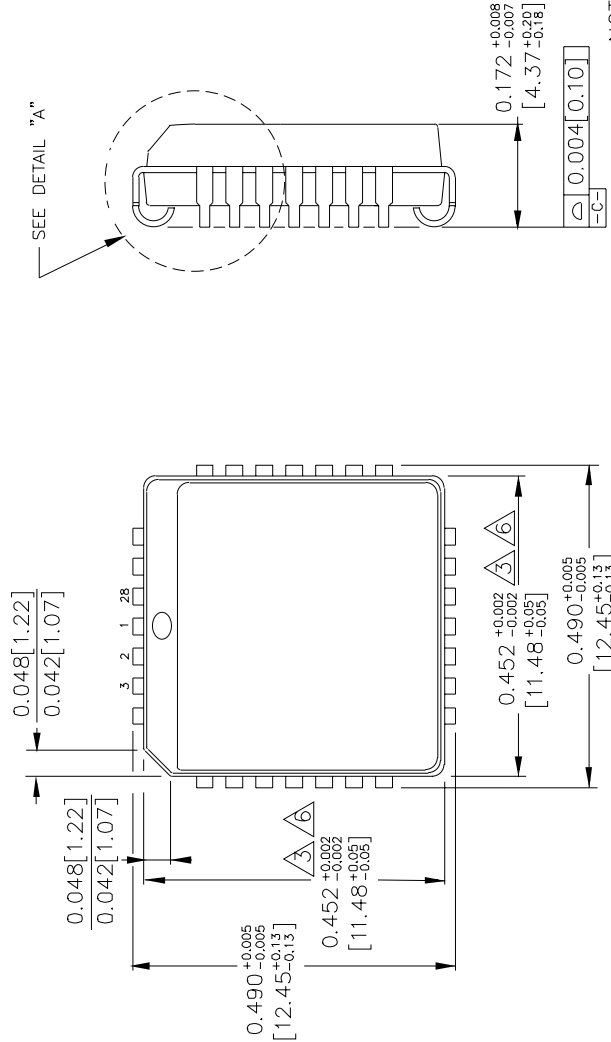
FILE/REV #: PD0008A03

PD/0008/ASCORP

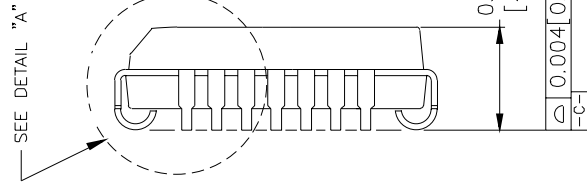
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REV.	REVISION DESCRIPTION	DATE
01	CONVERT TO DESIGNER VERSION 4.0 FORMAT, ADD COVER PAGE TO SPEC, CHANGE BODY WIDTH DIMENSION FROM 0.450[1.43] TO 0.443[1.25], TYPOGRAPHICAL ERROR.	08/18/94
02	CONVERT DWG FROM DESIGNER TO AUTOCAD, REL. 12, REFERENCE ANKOR, DWG. NO. 34865, REV. 00.	02/22/96
03	CONVERT DWG TO REL. 13 AND ONE PAGE DOCUMENT.	02/18/98

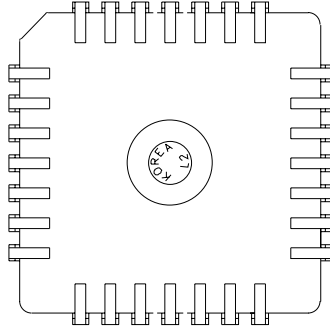
TOP VIEW



SIDE VIEW



BOTTOM VIEW



NOTES:

1. DIMENSIONS ARE IN INCHES[MM].
2. CONTROLLING DIMENSION: INCHES.
3. DIMENSION DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS, EITHER OF WHICH SHALL NOT EXCEED 0.008[0.203].
4. LEAD DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION.
5. MAXIMUM AND MINIMUM SPECIFICATIONS ARE INDICATED AS FOLLOWS: MAX/MIN
6. PACKAGE TOP DIMENSION MAY BE SLIGHTLY SMALLER THAN BOTTOM DIMENSION.



3250 SCOTT BOULEVARD  
SANTA CLARA, CA 95054  
TEL: 408-560-1100  
FAX: 408-567-7878

APPROVALS	DATE	APPROVALS	DATE	SIZE	PACKAGE OUTLINE
ORIGINATOR:	02/23/98	QUALITY:		A	28 LEAD PLCC
CHK'D:		DOCUMENT CONTROL:			
RELEASE DATE:					

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SCALE: N/A  
REVISION: 03

DETAIL "A"