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# ERROR DETECTION/ CORRECTION CIRCUIT

SY10E193 SY100E193

### **FEATURES**

- Hamming code generation
- Extended 100E VEE range of -4.2V to -5.5V
- 8-bit wide
- **■** Expandable for more width
- Provides parity register
- Fully compatible with industry standard 10KH, 100K ECL levels
- Internal75K $\Omega$  input pulldown resistors
- Fully compatible with Motorola MC10E/100E193
- Available in 28-pin PLCC package

### **DESCRIPTION**

The SY10/100E193 are error detection and correction (EDAC) circuits designed for use in new, high-performance ECL systems. The E193 generates hamming parity codes on an 8-bit word as shown in the block diagram. The P5 output gives the parity of the whole word. PGEN provides word parity after Odd/Even parity control and gating with the BPAR input. PGEN also feeds into a 1-bit shiftable register for use as part of a scan ring.

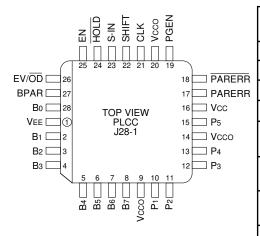
The combinatorial part of the device generates the same code pattern as the Motorola MC10193.

Used in conjunction with 12-bit parity generators, such as the E160, a SECDED (single error correction, double error detection) error system can be designed for a multiple of an 8-bit word.

## **PIN NAMES**

Pin	Function
B0-B7	Check Bit Inputs
BPAR	Check Bit Parity Input
EV/OD	Even/Odd Parity Select
ĒN	Parity Enable
HOLD	Syndrome Hold Input
S-IN	Syndrome Bit Input
SHIFT	Syndrome Bit Shift
CLK	Clock Input
P1-P5	Parity Output
PGEN	Parity Generate Output
PARERR/PARERR	Parity Error Output
Vcco	Vcc to Output

## PACKAGE/ORDERING INFORMATION



28-Pin PLCC (J28-1)

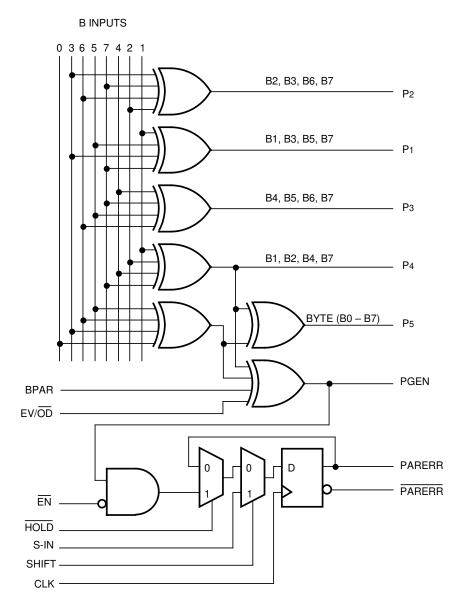
## Ordering Information<sup>(1)</sup>

Part Number	Package Type	Operating Range	Package Marking	Lead Finish	
SY10E193JC	J28-1	Commercial	SY10E193JC	Sn-Pb	
SY10E193JCTR <sup>(2)</sup>	J28-1	Commercial	SY10E193JC	Sn-Pb	
SY100E193JC	J28-1	Commercial	SY100E193JC	Sn-Pb	
SY100E193JCTR <sup>(2)</sup>	J28-1	Commercial	SY100E193JC	Sn-Pb	
SY10E193JZ <sup>(3)</sup>	J28-1	Commercial	SY10E193JZ with Pb-Free bar-line indicator	Matte-Sn	
SY10E193JZTR <sup>(2, 3)</sup>	J28-1	Commercial	SY10E193JZ with Pb-Free bar-line indicator	Matte-Sn	
SY100E193JZ <sup>(3)</sup>	J28-1	Commercial	SY100E193JZ with Pb-Free bar-line indicator	Matte-Sn	
SY100E193JZTR <sup>(2, 3)</sup>	J28-1	Commercial	SY100E193JZ with Pb-Free bar-line indicator	Matte-Sn	

#### Notes

- 1. Contact factory for die availability. Dice are guaranteed at  $T_A$  = 25°C, DC Electricals only.
- 2. Tape and Reel.
- 3. Pb-Free package is recommended for new designs.

## **BLOCK DIAGRAM**



## DC ELECTRICAL CHARACTERISTICS

VEE = VEE (Min.) to VEE (Max.); VCC = VCCO = GND

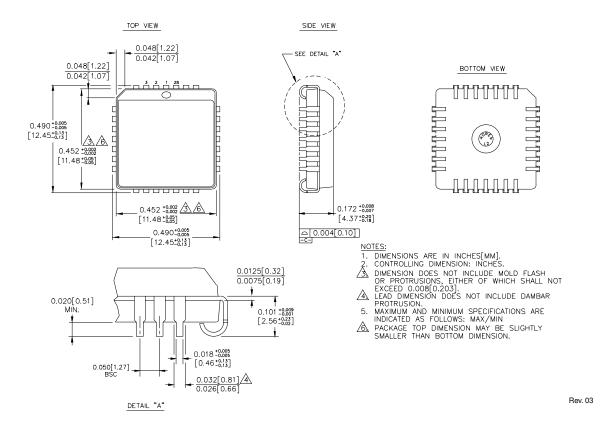
		TA = 0°C			TA = +25°C			TA = +85°C				
Symbol	Parameter	Min.	Тур.	Max.	Min.	Тур.	Max.	Min.	Тур.	Max.	Unit	Condition
Iн	Input HIGH Current	_	_	150	_	_	150	_	_	150	μΑ	
IEE	Power Supply Current 10E 100E	_	112 112	134 134	_	112 112	134 134	_	112 129	134 155	mA	_

## **AC ELECTRICAL CHARACTERISTICS**

VEE = VEE (Min.) to VEE (Max.); VCC = VCCO = GND

		TA = 0°C		TA = +25°C			TA = +85°C					
Symbol	Parameter	Min.	Тур.	Max.	Min.	Тур.	Max.	Min.	Тур.	Max.	Unit	Condition
tPD	Propagation Delay to Output B to P1, P2, P3, P4 B to P5 EV/OD, BPAR to PGEN B to PGEN CLK to PARERR	350 400 350 600 300	700 775 650 1000 550	1000 1150 850 1450 850	350 400 350 600 300	700 775 650 1000 550	1000 1150 850 1450 850	350 400 350 600 300	700 775 650 1000 550	1000 1150 850 1450 850	ps	_
ts	Set-up Time SHIFT S-IN HOLD EN EV/OD BPAR B	400 300 750 500 1300 1300 1700	150 50 350 250 850 850 1100	_ _ _ _	400 300 750 500 1300 1300 1700	150 50 350 250 850 850 1100		400 300 750 500 1300 1300 1700	150 50 350 250 850 850 1100		ps	_
tH	Hold Time SHIFT S-IN HOLD EN EV/OD BPAR B	200 300 100 100 -200 -200 -300	-150 -50 -350 -250 -850 -850 -1100	_ _ _ _	200 300 100 100 -200 -200 -300	-150 -50 -350 -250 -850 -850 -1100		200 300 100 100 -200 -200 -300	-150 -50 -350 -250 -850 -850 -1100		ps	_
tr tf	Rise/Fall Time 20% to 80%	300	700	1100	300	700	1100	300	700	1100	ps	_

## 28-PIN PLCC (J28-1)



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