![Chipsmall logo]

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We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!
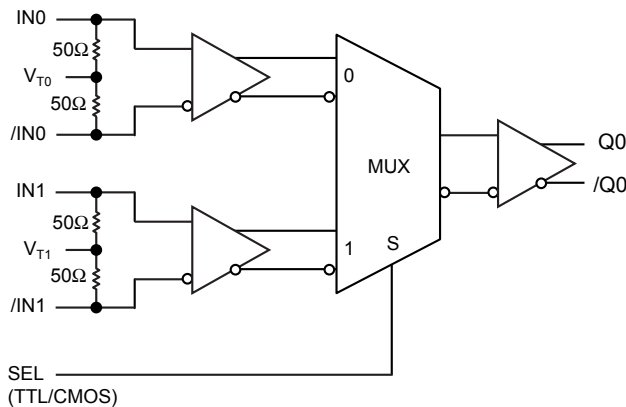

Contact us

FEATURES

- **Guaranteed AC performance over temperature and voltage:**
  - **DC to 5Gbps data throughput**
  - **DC to > 4GHz f_{MAX} (clock)**
  - **< 260ps propagation delay**
  - **< 110ps t_r / t_f times**
- **Ultra-low crosstalk-induced jitter: 0.7ps$_{RMS}$**
- **Ultra-low jitter design:**
  - **< 1ps$_{RMS}$ random jitter**
  - **< 10ps$_{PP}$ deterministic jitter**
  - **< 10ps$_{PP}$ total jitter (clock)**
- **Unique input termination and V_T pin accepts DC- and AC-coupled inputs (CML, PECL, LVDS)**
- **800mV (100k) LVPECL output swing**
- **Power supply 2.5V ±5% or 3.3V ±10%**
- **–40°C to +85°C temperature range**
- **Available in 16-pin (3mm x 3mm) QFN package**

APPLICATIONS

- **Redundant clock distribution**
- **SONET/SDH clock/data distribution**
- **Loopback**
- **Fibre Channel distribution**
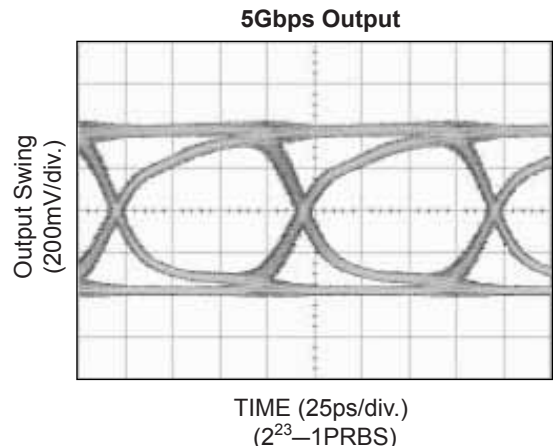
Precision Edge®

DESCRIPTION

The SY58018U is a 2.5V/3.3V precision, high-speed, 2:1 differential MUX capable of handling clocks up to 4GHz and data up to 5Gbps.

The differential input includes Micrel's unique, 3-pin input termination architecture that allows customers to interface to any differential signal (AC- or DC-coupled) as small as 100mV without any level shifting or termination resistor networks in the signal path. The outputs are 800mV, 100k compatible, LVPECL, with extremely fast rise/fall times guaranteed to be less than 110ps.

The SY58018U operates from a 2.5V ±5% supply or a 3.3V ±10% supply and is guaranteed over the full industrial temperature range of –40°C to +85°C. For applications that require CML outputs, consider the SY58017U or for 400mV LVPECL outputs the SY58019U. The SY58018U is part of Micrel's high-speed, Precision Edge® product line.
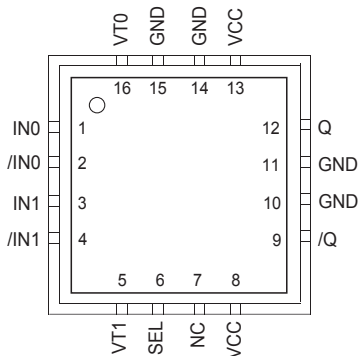
All support documentation can be found on Micrel's web site at www.micrel.com.

FUNCTIONAL BLOCK DIAGRAM

TYPICAL PERFORMANCE

5Gbps Output

Output Swing (200mV/div.)

TIME (25ps/div.)
(2^{23}–1PRBS)

Precision Edge and AnyGate are registered trademarks of Micrel, Inc.

PACKAGE/ORDERING INFORMATION

16-Pin QFN

Ordering Information[1]

Part Number	Package Type	Operating Range	Package Marking	Lead Finish
SY58018UMG	QFN-16	Industrial	018U with Pb-Free bar-line indicator	Pb-Free NiPdAu
SY58018UMGTR[2]	QFN-16	Industrial	018U with Pb-Free bar-line indicator	Pb-Free NiPdAu

Notes:

1. Contact factory for die availability. Dice are guaranteed at $T_A = 25°C$, DC electricals only.

2. Tape and Reel.

PIN DESCRIPTION

Pin Number	Pin Name	Pin Function
1, 2 3, 4	IN0, /IN0 IN1, /IN1	Differential Input: These input pairs are the differential signal inputs to the device. They accept differential AC- or DC-coupled signals as small as 100mV. Each pin of a pair internally terminates to a V_T pin through 50ý. Note that these inputs will default to an indeterminate state if left open. Please refer to the *"Input Interface Applications"* section for more details.
16, 5	VT0, VT1	Input Termination Center-Tap: Each side of the differential input pair terminates to a V_T pin. The V_{T0} and V_{T1} pins provide a center-tap to a termination network for maximum interface flexibility. See *"Input Interface Applications"* section for more details.
6	SEL	This single-ended TTL/CMOS compatible input selects the inputs to the multiplexer. Note that this input is internally connected to a 25ký pull-up resistor and will default to a logic HIGH state if left open.
7	NC	No connect.
8, 13	VCC	Positive Power Supply: Bypass with 0.1µF™™ 0.01µF low ESR capacitors. 0.01µF capacitor should be as close to V_{CC} pin as possible.
12, 9	Q, /Q	Differential Outputs: This 100k compatible LVPECL output pair is the output of the device. Normally terminate with 50ý to V_{CC} – 2V. See *"Output Interface Applications"* section. It is a logic function of the IN0, IN1, and SEL inputs. Please refer to the *"Truth Table"* for details.
10, 11, 14, 15	GND, Exposed Pad	Ground. Ground pins and exposed pad must be connected to the same ground plane.

TRUTH TABLE

SEL	Output
0	CH0 Input Selected
1	CH1 Input Selected

Absolute Maximum Ratings[1]

Power Supply Voltage (V_{CC}) .... –0.5V to +4.0V

Input Voltage (V_{IN}) .... –0.5V to V_{CC}

LVPECL Output Current (I_{OUT})
    Continuous 50mA
    Surge 100mA

Termination Current[3]
    Source or Sink Current on V_T pin ....±100mA

Input Current
    Source or Sink Current on IN, /IN pin ....±50mA

Lead Temperature (soldering, 20 sec.) .... 260°C

Storage Temperature Range (T_S) ....–65°C to +150°C

Operating Ratings[2]

Power Supply Voltage (V_{CC}) .... +2.375V to +2.625V
    .... +3.0V to +3.6V

Ambient Temperature Range (T_A).............–40°C to +85°C

Package Thermal Resistance[4]
    QFN (θ_{JA})
        Still-Air .... 60°C/W
    QFN (ψ_{JB})
        Junction-to-Board .... 38°C/W

DC ELECTRICAL CHARACTERISTICS[5]

T_A= –40°C to +85°C, unless otherwise stated.

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{CC}	Power Supply Voltage	V_{CC} = 2.5V V_{CC} = 3.3V	2.375 3.0	2.5 3.3	2.625 3.6	V V
I_{CC}	Power Supply Current	No load, max. V_{CC}		50	65	mA
R_{DIFF_IN}	Differential Input Resistance (IN0-to-/IN0, IN1-to-/IN1)		80	100	120	Ω
R_{IN}	Input Resistance (IN0-to-V_{T0}, /IN0-to-V_{T0}, IN1-to-V_{T1}, /IN1-to-V_{T1})		40	50	60	Ω
V_{IH}	Input HIGH Voltage (IN0, /IN0, IN1, /IN1)	**Note 6**	V_{CC} – 1.6		V_{CC}	V
V_{IL}	Input LOW Voltage (IN0, /IN0, IN1, /IN1)		0		V_{IH} – 0.1	V
V_{IN}	Input Voltage Swing (IN0, /IN0, IN1, /IN1)	See Figure 1a	0.1		1.7	V
V_{DIFF_IN}	Differential Input Voltage Swing |IN0, /IN0|, |IN1, /IN1|	See Figure 1b	0.2			V
$V_{T IN}$	IN to V_T (IN0, /IN0, IN1, /IN1)				1.28	V

Notes:

1. Permanent device damage may occur if absolute maximum ratings are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.

2. The data sheet limits are not guaranteed if the device is operated beyond the operating ratings.

3. Due to the limited drive capability, use for input of the same package only.

4. Package thermal resistance assumes exposed pad is soldered (or equivalent) to the device's most negative potential (GND) on the PCB. ψ_{JB} uses 4-layer θ_{JA} in still-air number, unless otherwise stated.

5. The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.

6. V_{IH} (min) not lower than 1.2V.

LVPECL OUTPUT DC ELECTRICAL CHARACTERISTICS[7]

V_{CC} = 2.5V ±5% or 3.3V ±10%; T_A= –40°C to +85°C; R_L = 50ý to V_{CC}–2V, unless otherwise stated.

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{OH}	Output HIGH Voltage Q, /Q		V_{CC} – 1.145		V_{CC} – 0.895	V
V_{OL}	Output LOW Voltage Q, /Q		V_{CC} – 1.945		V_{CC} – 1.695	V
V_{OUT}	Output Differential Swing Q, /Q	See Figure 1a	550	800		mV
V_{DIFF_OUT}	Differential Output Voltage Swing Q, /Q	See Figure 1b	1100	1600		mV

LVTTL/CMOS DC ELECTRICAL CHARACTERISTICS[7]

V_{CC} = 2.5V ±5% or 3.3V ±10%; T_A= -40°C to 85°C

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{IH}	Input HIGH Voltage		2.0			V
V_{IL}	Input LOW Voltage				0.8	V
I_{IH}	Input HIGH Current				40	µA
I_{IL}	Input LOW Current		–300			µA

Note:

7. The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.

AC ELECTRICAL CHARACTERISTICS[8]

V_{CC} = 2.5V ±5% or 3.3V ±10%; T_A= –40°C to 85°C, R_L = 50ý to V_{CC} – 2V, unless otherwise stated.

Symbol	Parameter	Condition		Min	Typ	Max	Units
f_{MAX}	Maximum Operating Frequency		NRZ Data	5			Gbps
		V_{OUT} ž 400mV	Clock		4		GHz
t_{pd}	Differential Propagation Delay (IN0 or IN1-to-Q) (SEL-to-Q)			110 50	190 180	240 350	ps ps
t_{pd} Tempco	Differential Propagation Delay Temperature Coefficient				75		fs/°C
t_{SKEW}	Input-to-Input Skew	**Note 9**			4	15	ps
	Part-to-Part Skew	**Note 10**				100	ps
t_{JITTER}	Data Random Jitter	**Note 11**				1	ps$_{RMS}$
	Deterministic Jitter	**Note 12**				10	ps$_{PP}$
	Clock Cycle-to-Cycle Jitter	**Note 13**				1	ps$_{RMS}$
	Total Jitter	**Note 14**				10	ps$_{PP}$
	Crosstalk-Induced Jitter	**Note 15**				0.7	ps$_{RMS}$
t_r, t_f	Output Rise/Fall Time	20% to 80%, at full swing		35	75	110	ps

Notes:

8. High frequency AC parameters are guaranteed by design and characterization.

9. Input-to-input skew is the difference in time from and input-to-output in comparison to any other input-to-output. In addition, the input-to-input skew does not include the output skew.

10. Part-to-part skew is defined for two parts with identical power supply voltages at the same temperature and with no skew of the edges at the respective inputs.

11. RJ is measured with a K28.7 comma detect character pattern, measured at 10.7Gbps and 2.5Gbps/3.2Gbps.

12. DJ is measured at 2.5Gbps/3.2Gbps, with both K28.5 and 2^{23} – 1 PRBS pattern.

13. Cycle-to-cycle jitter definition: the variation of periods between adjacent cycles, $T_n – T_{n-1}$ where T is the time between rising edges of the output signal.

14. Total jitter definition: with an ideal clock input of frequency - f_{MAX} no more than one output edge in 10^{12} output edges will deviate by more than the specified peak-to-peak jitter value.

15. Crosstalk is measured at the output while applying two similar frequencies that are asynchronous with respect to each other at the inputs.

SINGLE-ENDED AND DIFFERENTIAL SWINGS

V_{IN}, V_{OUT} 800mV (Typ.)
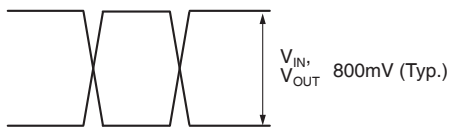
Figure 1a. Single-Ended Voltage Swing
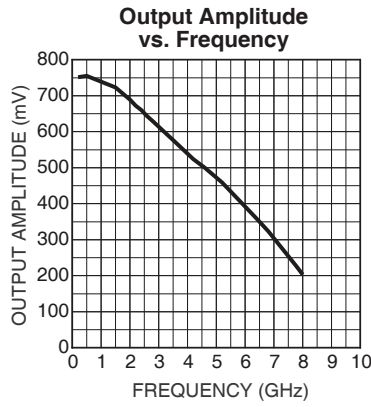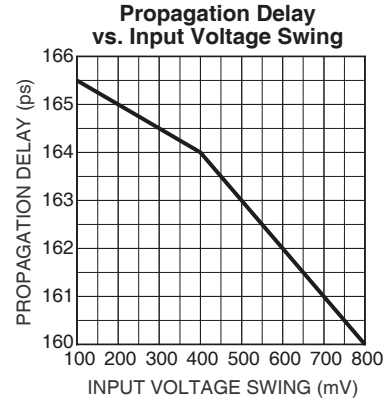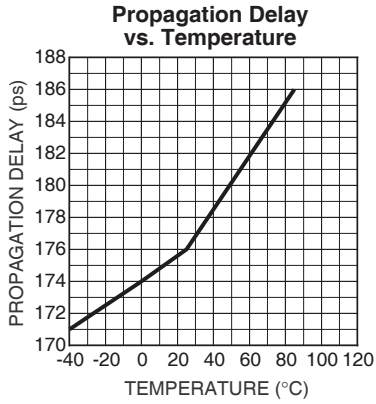

V_{DIFF_IN}, V_{DIFF_OUT} 1600mV (Typ.)
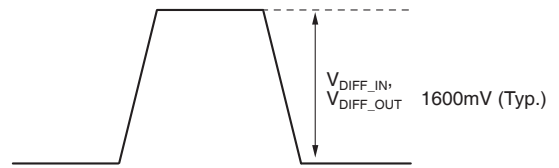
Figure 1b. Differential Voltage Swing

TIMING DIAGRAMS
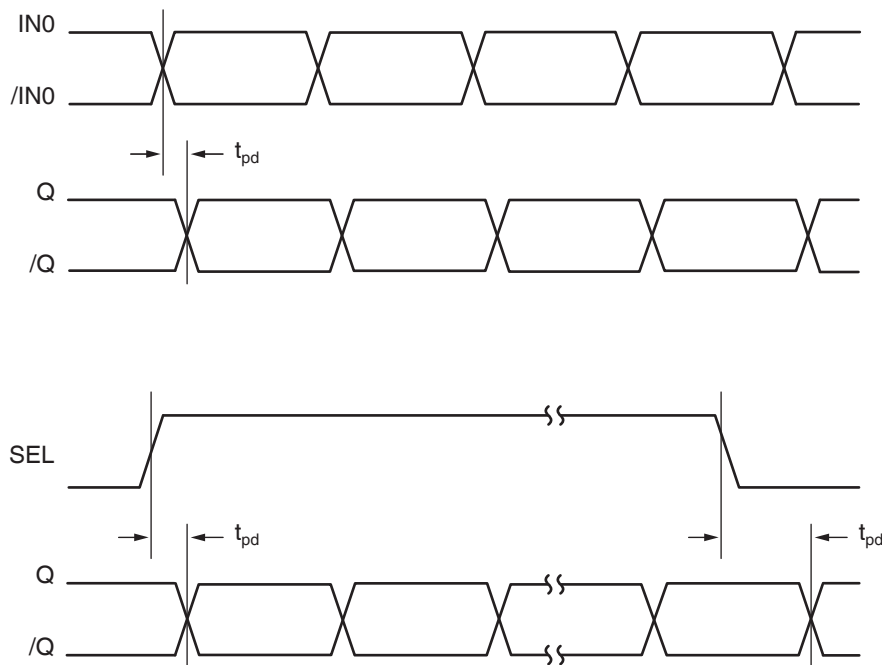
IN0
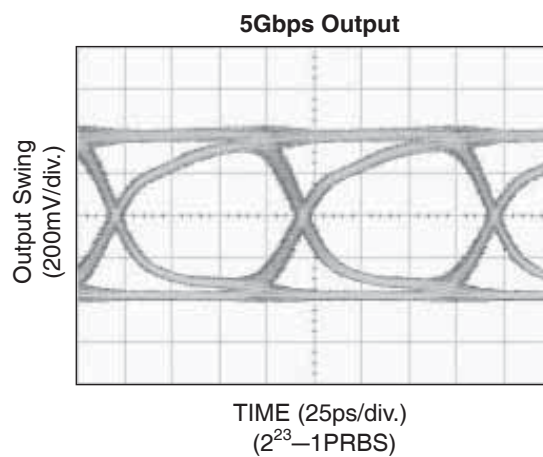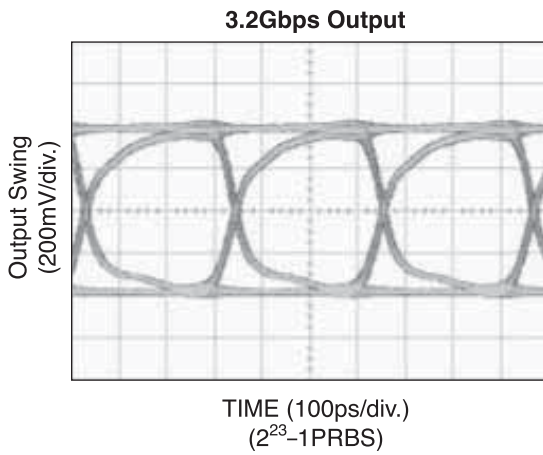
/IN0

t_{pd}

Q

/Q

SEL

t_{pd}

t_{pd}

Q

/Q

TYPICAL OPERATING CHARACTERISTICS

V_{CC} = 3.3V, V_{IN} = 100mV, T_A = 25°C, unless otherwise stated.

**Propagation Delay
vs. Temperature**

**Propagation Delay
vs. Input Voltage Swing**

**Output Amplitude
vs. Frequency**

TYPICAL OPERATING CHARACTERISTICS

V_{CC} = 3.3V, V_{IN} = 100mV, T_A = 25°C, unless otherwise stated.

200MHz Output

Output Swing (200mV/div.)

TIME (600ps/div.)

1.25GHz Output

Output Swing (200mV/div.)

TIME (100ps/div.)

2.5Gbps Output

Output Swing (200mV/div.)

TIME (100ps/div.)
(2^{23}–1PRBS)

3.2Gbps Output

Output Swing (200mV/div.)

TIME (100ps/div.)
(2^{23}–1PRBS)

5Gbps Output

Output Swing (200mV/div.)

TIME (25ps/div.)
(2^{23}–1PRBS)
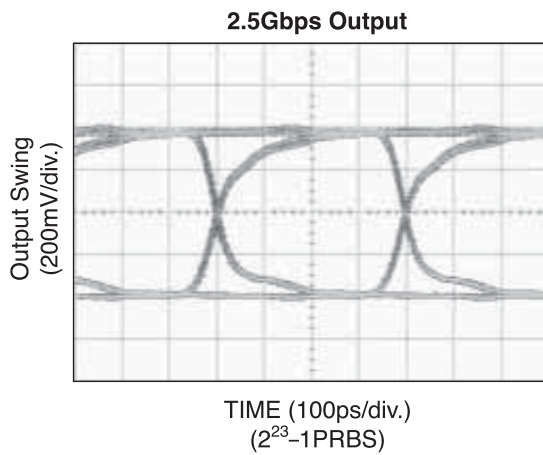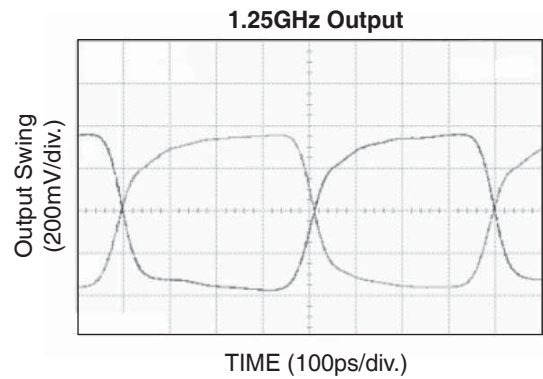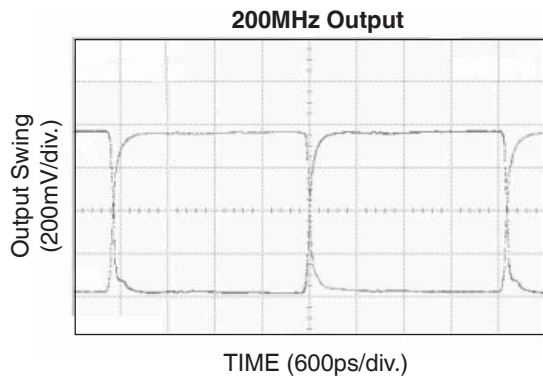
INPUT AND OUTPUT STAGES
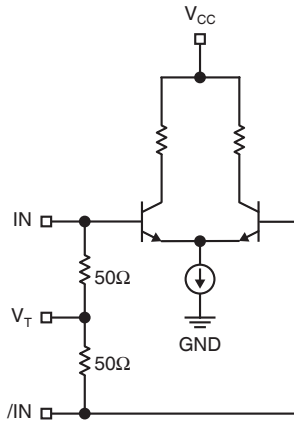
Figure 2a. Simplified Differential Input Stage
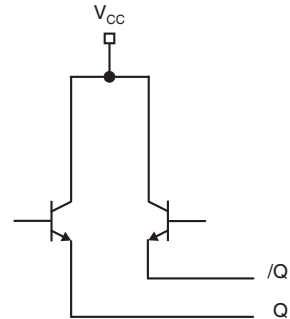
Figure 2b. Simplified LVPECL Output Stage

INPUT INTERFACE APPLICATIONS

For $V_{CC} = 3.3V$, $R_{pd} = 50\Omega$
For $V_{CC} = 2.5V$, $R_{pd} = 19\Omega$
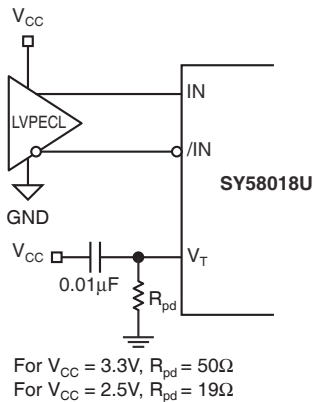
**Figure 3a. DC-Coupled
LVPECL Interface**

For 3.3V, $R_{pd} = 100\Omega$
For 2.5V, $R_{pd} = 50\Omega$
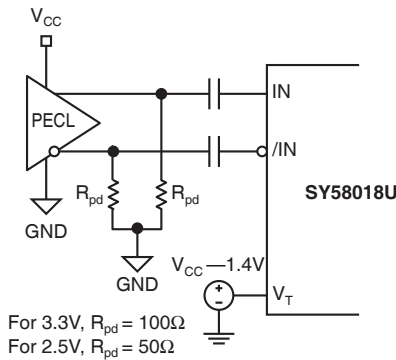
**Figure 3b. AC-Coupled
LVPECL Interface**

(Option: May connect V_T to V_{CC})
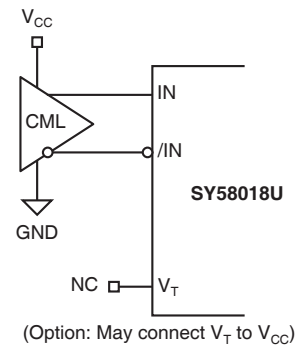
**Figure 3c. DC-Coupled
CML Interface**
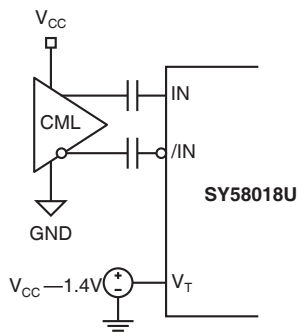
**Figure 3d. AC-Coupled
CML Interface**
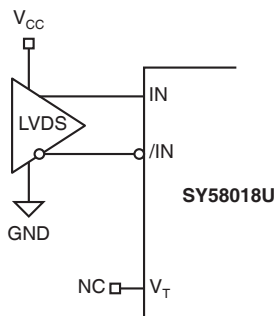
Figure 3e. LVDS Interface

OUTPUT INTERFACE APPLICATIONS
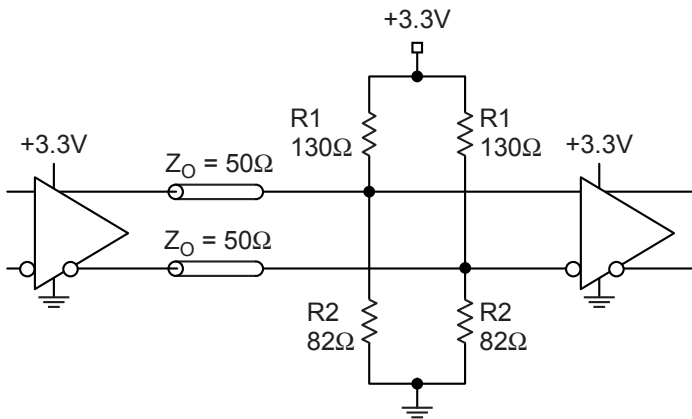
Figure 4a. Parallel Thevenin-Equivalent Termination

For 3.3V, R_b = 50Ω
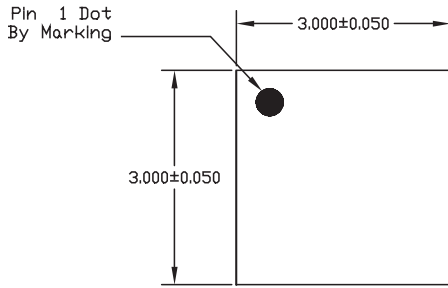For 2.5V, R_b = 19Ω
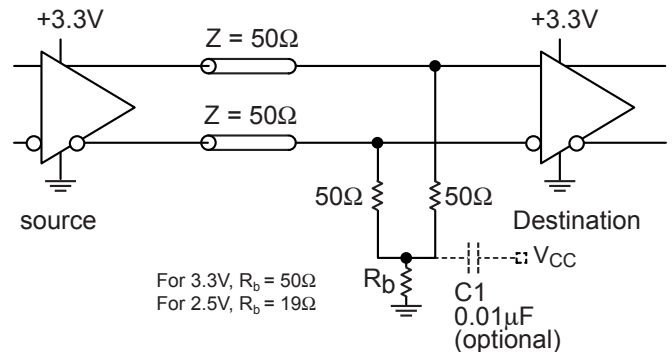
Figure 4b. Three-Resistor "Y" Termination
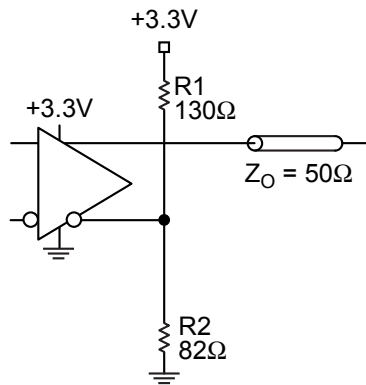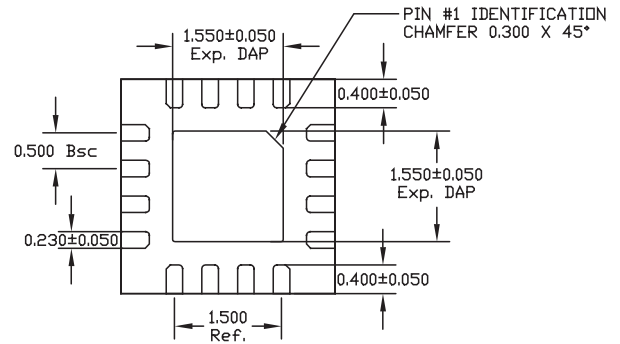

Figure 4c. Terminating Unused I/O

RELATED MICREL PRODUCTS AND SUPPORT DOCUMENTATION

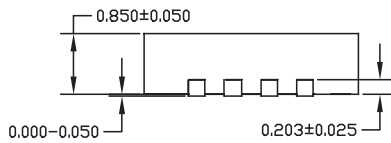| Part Number	Function	Data Sheet Link
SY58016L	3.3V 10Gbps Differential CML Line Driver/Receiver with Internal I/O Termination	http://www.micrel.com/product-info/products/sy58016l.shtml
SY58017U	Ultra Precision Differential CML 2:1 Mux with Internal I/O Termination	http://www.micrel.com/product-info/products/sy58017u.shtml
SY58019U	Ultra Precision Differential 400mV LVPECL 2:1 MUXwith Internal Termination	http://www.micrel.com/product-info/products/sy58019u.shtml
SY58025U	10.7Gbps Dual 2:1 CML MUX with Internal I/O Termination	http://www.micrel.com/product-info/products/sy58025u.shtml
SY58026U	5Gbps Dual 2:1 MUXwith Internal Termination	http://www.micrel.com/product-info/products/sy58026u.shtml
SY58027U	10.7Gbps Dual 2:1 400mV LVPECL MUXwith Internal Termination	http://www.micrel.com/product-info/products/sy58027u.shtml
SY58051U	10.7Gbps AnyGate® with Internal Input and Output Termination	http://www.micrel.com/product-info/products/sy58051u.shtml
SY58052U	10Gbps Clock/Data Retimer with 50Ω Input Termination	http://www.micrel.com/product-info/products/sy58052u.shtml
HBW Solutions	New Products and Applications	www.micrel.com/product-info/products/solutions.shtml

16-PIN QFN   (QFN-16)

Pin 1 Dot
By Marking

3.000±0.050

3.000±0.050

TOP VIEW

1.550±0.050
Exp. DAP

PIN #1 IDENTIFICATION
CHAMFER 0.300 X 45°

0.400±0.050

0.500 Bsc

1.550±0.050
Exp. DAP

0.230±0.050

0.400±0.050

1.500
Ref.
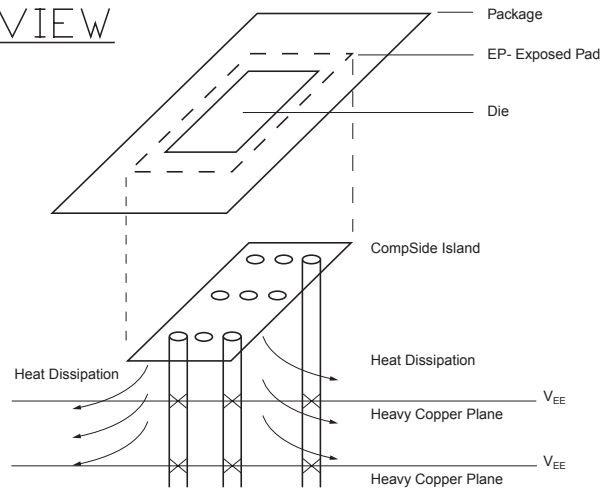
BOTTOM VIEW

NOTE:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. MAX. PACKAGE WARPAGE IS 0.05 mm.
3. MAXIMUM ALLOWABE BURRS IS 0.076 mm IN ALL DIRECTIONS.
4. PIN #1 ID ON TOP WILL BE LASER/INK MARKED.

0.850±0.050

0.000−0.050

0.203±0.025

SIDE VIEW

Package

EP- Exposed Pad

Die

CompSide Island

Heat Dissipation

Heat Dissipation

V_{EE}

Heavy Copper Plane

V_{EE}

Heavy Copper Plane

PCB Thermal Consideration for 16-Pin QFN Package
(Always solder, or equivalent, the exposed pad to the PCB)

Package Notes:

1. Package meets Level 2 qualification.
2. All parts are dry-packaged before shipment.
3. Exposed pads must be soldered to a ground for proper thermal management.