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Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

# SY58051U

## Ultra-Precision CML AnyGate®
## with Internal Input and Output Termination

### Precision Edge®

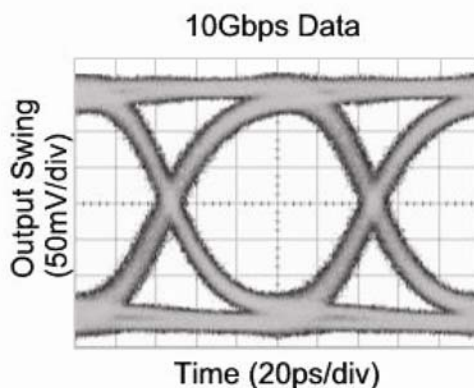**Precision Edge®**

## General Description

The SY58051U is an ultra-fast, low jitter universal logic gate with a guaranteed maximum data or clock throughput of 10.7Gbps or 7GHz, respectively. This AnyGate® differential logic device will produce many logic functions of two Boolean variables, such as AND, NAND, OR, NOR, DELAY, or NEGATION.

The SY58051U differential inputs include a unique internal termination design that allows access to the termination network throughout a $V_T$ pin. This feature allows the device to easily interface to different logic standards, both AC- and DC-coupled without external resistor-bias and termination networks. The result is a clean, stub-free, low-jitter interface solution. The differential CML output is optimized for environments with internal 50Ω source termination and a 400mV output swing.

The SY58051U operates from a 2.5 or 3.3V supply, and is guaranteed over the full industrial temperature range (-40°C to +85°C). The SY58051U is part of Micrel's Precision Edge® product family.

All support documentation can be found on Micrel's web site at www.micrel.com.

## Typical Application



## Features

- Three matched-delay input pair provide any logic function: AND, NAND, OR, NOR
- Guaranteed AC performance over temperature and
- voltage:
  - DC to > 10.7Gbps data rate throughput
  - DC to > 7GHz clock $f_{MAX}$
  - <190ps Any In-to-Out $t_{pd}$
  - $t_r$ / $t_f$ < 60ps
- Ultra low-jitter design:
  - <1ps$_{RMS}$ random jitter
  - <10ps$_{PP}$ deterministic jitter
  - <10ps$_{PP}$ total jitter (clock)
- Unique input termination and $V_T$ pin accepts DC-coupled and AC-coupled inputs (CML, PECL)
- Internal 50Ω output source termination
- Typical 400mV CML output swing ($R_{IN}$ = 50Ω)
- Internal 50Ω input termination
- Power supply 2.5V ±5% or 3.3V ±10%
- –40°C to 85°C temperature range
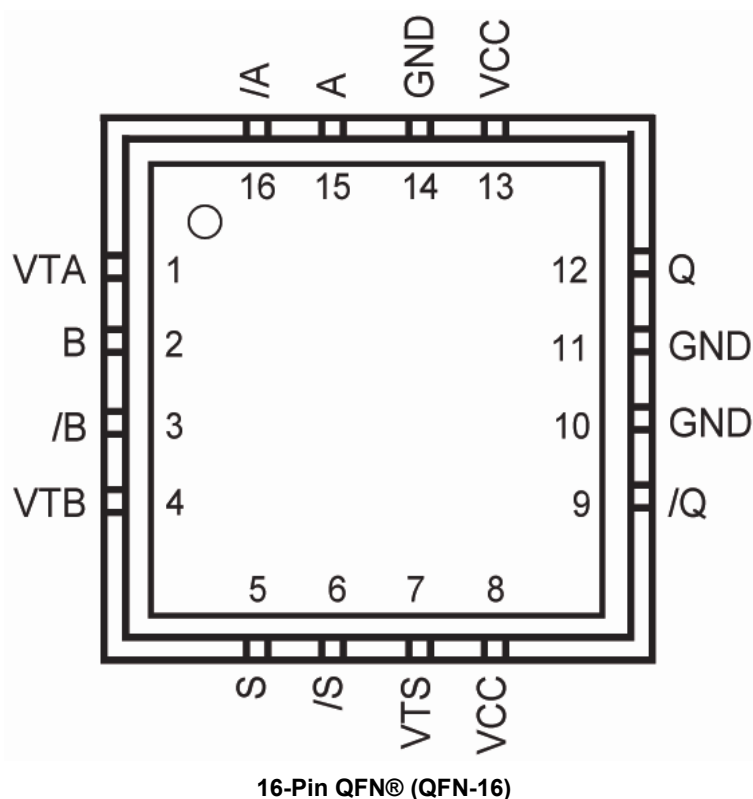- Available in a 16-pin (3mm × 3mm) QFN® package

## Applications

- Data communication systems
- OC-192, OC192+FEC
- All SONET OC-3—OC-768 applications
- All Fibre Channel applications
- All GigE applications

## Ordering Information

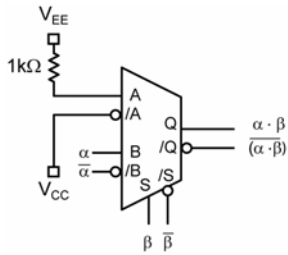| Part Number | Package Type | Operational Range | Package Marking |
|---|---|---|---|
| SY58051UMG[3] | Pb-free QFN-16 | Industrial | 051U with Pb-Free bar-line indicator |
| SY58051UMGTR[2, 3] | Pb-free QFN-16 | Industrial | 051U with Pb-Free bar-line indicator |

# Pin Configuration



**16-Pin QFN® (QFN-16)**

# Pin Description

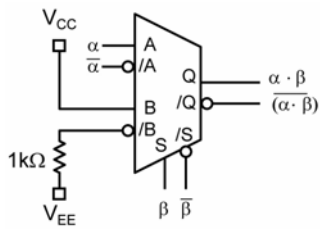| Pin Number | Pin Name | Pin Function |
|---|---|---|
| 1 | VT | Input Termination Center Tap: Each of the two inputs, (A, /A) terminates to this pin through a50Ω resistor. The VTA pin provides a center-tap to a termination network for maximum interface flexibility. See "Input Interface Applications" section for more details. |
| 15, 16<br>2, 3 | A, /A<br>B, /B | Differential Input: These input pairs are the two data inputs to the device. Each pin of a pair 2, 3 B, /B internally terminates to the VTA or VTB pin to 50Ω. Note that these inputs will default to an indeterminate state if left open. See "Input Interface Applications" section for more details. |
| 4 | VTB | Input Termination Center Tap: Each of the two inputs, (B, /B) terminates to this pin through a 50Ω resistor. The VTB pin provides a center-tap to a termination network for maximum interface flexibility. |
| 5, 6 | S, /S | Differential Input: This input pair is the select input to the device. Each pin of this pair internally terminates to the VTS pin to 50Ω. Note that this input will default to an indeterminate state if left open. See "Input Interface Applications" section for more details. |
| 7 | VTS | Input Termination Center Tap: Each of the two inputs, S, /S terminates to this pin. The VTS pin provides a center-tap to a termination network for maximum interface flexibility. |
| 8, 13 | VCC | Positive Power Supply. Bypass with 0.1µF☐☐0.01µF low ESR capacitors. |
| 12, 9 | Q, /Q | Differential Output: This CML output pair is the output of the device. It is a logic function of the A, B, and S inputs. See "Truth Tables" for details. |
| 10, 11, 14 | GND | Ground. Exposed pad must be connected to the same potential as GND pin. |

## Truth Tables

| A | /A | B | /B | S | /S | Q | /Q |
|---|----|---|----|---|----|---|----|
| 0 | 1 | X | X | 0 | 1 | 0 | 1 |
| 1 | 0 | X | X | 0 | 1 | 1 | 0 |
| X | X | 0 | 1 | 1 | 0 | 0 | 1 |
| X | X | 1 | 0 | 1 | 0 | 1 | 0 |

**AND/NAND**

| A | $\alpha$<br>B | $\beta$<br>B | $\alpha \bullet \beta$<br>Q | $\overline{(\overline{\alpha} \bullet \overline{\beta})}$<br>/Q |
|---|---|---|---|---|
| L | L | L | L | H |
| L | H | L | L | H |
| L | L | H | L | H |
| L | H | H | H | L |

**OR/NOR**

| $\alpha$<br>A | B | $\beta$<br>B | $\alpha \bullet \beta$<br>Q | $\overline{(\alpha + \beta)}$<br>/Q |
|---|---|---|---|---|
| L | H | L | L | H |
| H | H | L | H | L |
| L | H | H | H | L |
| H | H | H | H | L |
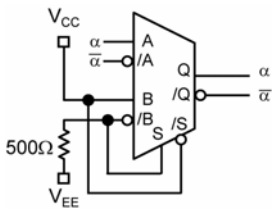
**DELAY/NEGATION**

| $\alpha$<br>A | B | S | $\alpha$<br>Q | $\overline{\alpha}$<br>/Q |
|---|---|---|---|---|
| L | | S | L | H |
| H | | S | H | L |
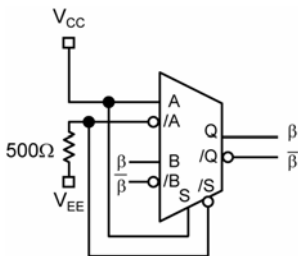
**DELAY/NEGATION**

| A | $\beta$<br>B | S | $\beta$<br>Q | $\overline{\beta}$<br>/Q |
|---|---|---|---|---|
| | L | H | L | H |
| | H | H | H | L |
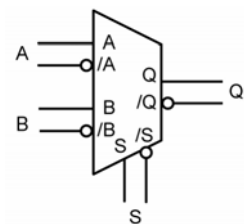
**2:1 MUX**

| S | Q | /Q |
|---|---|---|
| L | A | $\overline{A}$ |
| H | B | $\overline{B}$ |

## Absolute Maximum Ratings [1]

Supply Voltage ($V_{CC}$).......................................$-0.5$ to $+4.0V$
Input Voltage ($V_{IN}$).............................................$-0.5V$ to $V_{CC}$
CML Output Voltage ($V_{OUT}$).........$V_{CC}$ to $-1.0V$ to $V_{CC}$ $+0.5V$
Termination Current [3]
   Source or Sink Current on $V_{TA}$, $V_{TB}$, $V_{TS}$ ................$\pm60mA$
Input Current
   Source or Sink Current on A, /A, B, /B, S, /S .........$\pm30mA$
Lead Temperature (soldering, 20 sec.)....................$+260°C$
Storage Temperature ($T_S$.).........................$-65°C$ to $+150°C$

## Operating Ratings [2]

Supply Voltage ($V_{CC}$)....................... $+2.375V$ to $+2.625V$
                    or $+3.0°C$ to $+85°C$
Ambient Temperature ($T_A$)..................... $-40°C$ to $+85°C$
Package Thermal Resistance [4]
   PDIP ($\theta_{JA}$)
     Still-Air....................................................$61°C/W$
QFN ($\psi_{JB}$).............................................................$38°C/W$

## DC Electrical Characteristics [5]

TA = $-40°C$ to $+85°C$, unless otherwise noted.

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $V_{CC}$ | Power Supply | $V_{CC}$ = 2.5V. | 2.375 | 2.5 | 2.625 | V |
| | | $V_{CC}$ = 3.3V. | 3.0 | 3.3 | 3.6 | V |
| $I_{CC}$ | Power Supply Current | No Load, max. $V_{CC}$. | | 55 | 70 | mA |
| $R_{DIFF\_IN}$ | Differential Input Resistance (A-to/A, B-to-/B or S-to/S) | | 80 | 100 | 120 | $\Omega$ |
| $R_{IN}$ | Input Resistance (A-to-$V_{TA}$, B-to-$V_{TB}$ or S-to-$V_{TS}$) | | 40 | 50 | 60 | $\Omega$ |
| $V_{IH}$ | Input HIGH Voltage (A, /A or B, /B or S, /S) | **Note 6** | 1.2 | | $V_{CC}$ | V |
| $V_{IL}$ | Input LOW Voltage (A, /A or B, /B or S, /S) | **Note 6** | 0 | | $V_{IH}$-0.1 | mV |
| $V_{IN}$ | Input Voltage Swing (A, /A or B, /B or S, /S) | **Note 6** See Figure 2a. | 100 | | | mV |
| $V_{DIFF\_IN}$ | Differential Input Voltage Swing IA-, /AI or IB-, /BI or S-, /SI | **Note 6** See Figure 2b. | 200 | | | mV |
| $I_{IN}$ | Input Current (A, /A or B, /B or S, /S) | **Note 6** | | | 21 | mA |

**Notes:**

1. Permanent device damage may occur if the ratings in the "Absolute Maximum Ratings" section are exceeded. This is a stress rating only and functional operation is not implied for conditions other than those detailed in the operational sections of this data sheet. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.

2. The data sheet limits are not guaranteed if the device is operated beyond the operating ratings.

3. Due to the limited drive capability use for input of the same package only.

4. Package thermal resistance assumes exposed pad is soldered (or equivalent) to the devices most negative potential on the PCB. $\Psi_{JB}$ uses 4-layer $\theta_{JA}$ n still-air, unless otherwise stated.

5. The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.

6. Due to the internal termination (see Figure 1a) the input current depends on the applied voltages at A, /A and $V_{TA}$ inputs, the B, /B and $V_{TB}$ inputs or the S, /S and $V_{TS}$ inputs. Do not apply a combination of voltages that causes the input current to exceed the maximum limit.

## CML Electrical Characteristics [5]

$V_{CC}$ = 2.5V ±5% or 3.3V ±10%; $R_L$ =100Ω across output pair or equivalent; $T_A$ = -40°C to +85°C; unless otherwise noted.

| Symbol | Parameter | Condition | Min. | Typ | Max | Units |
|--------|-----------|-----------|------|-----|-----|-------|
| $V_{CH}$ | Output HIGH Voltage Q, /Q | | $V_{CC}$ 0.020 | | $V_{CC}$ 3.6 | V |
| $V_{OUT}$ | Output Voltage Swing Q, /Q | See Figure 2a. | 325 | 400 | 500 | mV |
| $V_{DIFF\_OUT}$ | Differential Output Voltage Swing Q, /Q | See Figure 2b. | 650 | 800 | 1000 | mV |
| $R_{OUT}$ | Output Source Impedance Q, /Q | | 40 | 50 | 60 | Ω |

## AC Electrical Characteristics [8]

$V_{CC}$ = 2.5V ±5% or 3.3V ±10%; $R_L$ =100Ω across output pair or equivalent; $T_A$ = -40°C to +85°C; unless otherwise noted.

| Symbol | Parameter | Condition | Min | Typ | Max | Units |
|--------|-----------|-----------|-----|-----|-----|-------|
| $F_{MAX}$ | Maximum Operating Frequency | Clock<br>NRZ Data | 10.7 | 7 | | GHz<br>Gbps |
| $t_{pd}$ | Propagation Delay Any Input (A, B, S)-to-Q | | 70 | | 190 | ps |
| $t_{SKEW}$ | Part-to-Part Skew | **Note 9** | | | 100 | ps |
| $t_{JITTER}$ | Data | | | | | |
| | Random Jitter (RJ) | **Note 10** | | | 1 | $ps_{RMS}$ |
| | Deterministic Jitter (DJ) | **Note 11** | | | 10 | $ps_{PP}$ |
| | Clock | | | | | |
| | Cycle-to-Cycle Jitter (RJ) | **Note 12** | | | 1 | $ps_{RMS}$ |
| | Total Jitter (TJ) | **Note 13** | | | 10 | $ps_{PP}$ |
| $T_R$, $t_f$ | Output Rise/Fall Times (20% to 80%) | At full output swing. | 20 | | 60 | ps |

**Notes:**

7.  The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.

8.  Measured with 100mV input swing. See "Timing Diagrams" section for definition of parameters. High-frequency AC parameters are guaranteed by design and characterization.

9.  Skew is defined for two parts with identical power supply voltages at the same temperature and with no skew of the edges at the respective inputs.

10. Random jitter is measured with a K28.7 comma detect character pattern, measured at 2.5Gbps/3.2Gbps.

11. Deterministic jitter is measured at 2.5Gbps/3.2Gbps with both K28.5 and $2^{23}$–1 PRBS pattern.

12. Cycle-to-cycle jitter definition: the variation of periods between adjacent cycles, $T_n$–$T_{n-1}$ where T is the time between rising edges of the output signal.

13. Total jitter definition: with an ideal clock input of frequency $\leq f_{MAX}$, no more than one output edge in $10^{12}$ output edges will deviate by more than the specified peak-to-peak jitter value.

## Functional Block Diagram
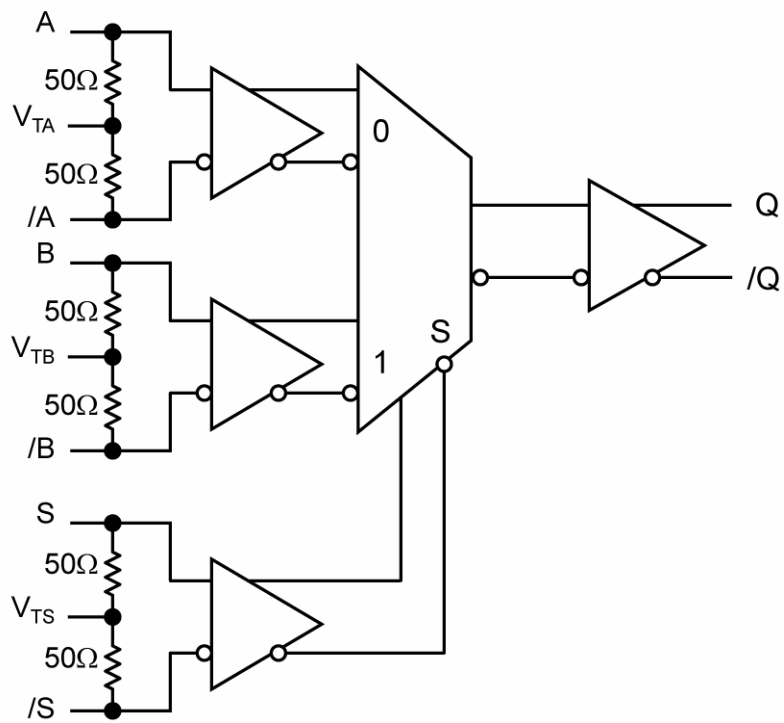
# Timing Diagram
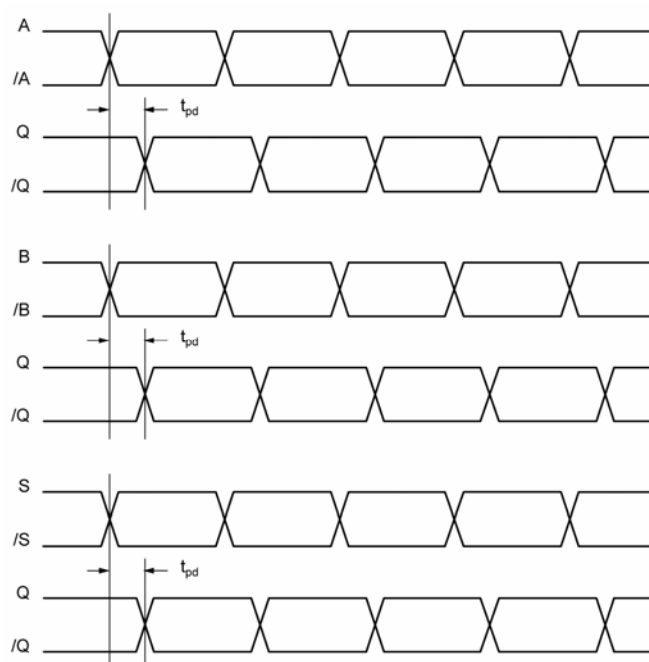


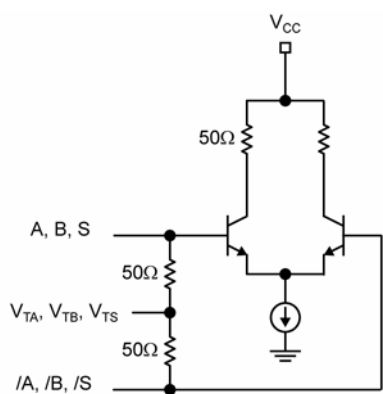# Input and Output Stage Internal Termination
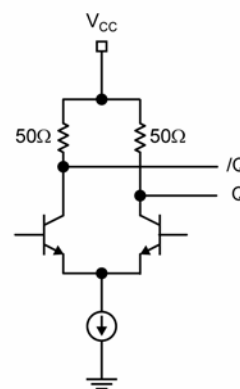


**Figure 1a. Simplified Differential Input Stage**

**Figure 1b. Simplified Differential Output Stage**
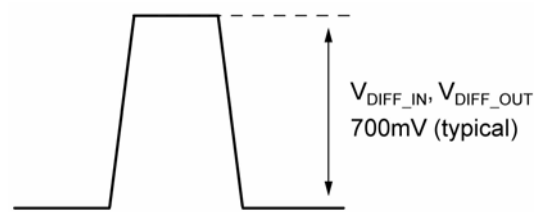
# Definition of Single-Ended and Differential Swings



$V_{IN}$, $V_{OUT}$
350mV
(typical)
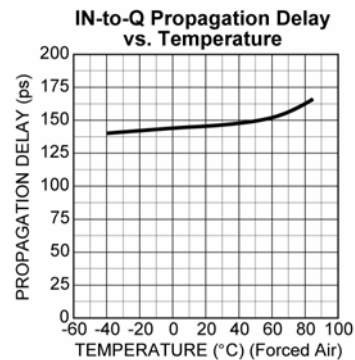
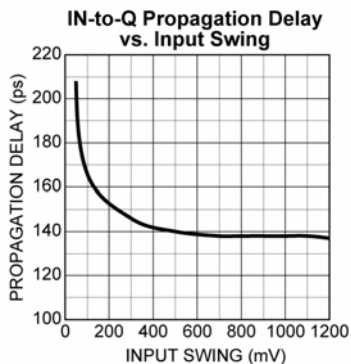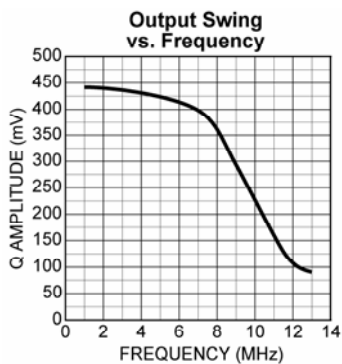**Figure 2a. Single-Ended Swing**



$V_{DIFF\_IN}$, $V_{DIFF\_OUT}$
700mV (typical)
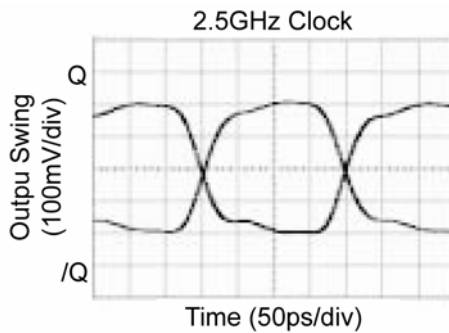
**Figure 2b. Differential Swing**

# Typical Operating Characteristics

**Output Swing vs. Frequency**

**IN-to-Q Propagation Delay vs. Input Swing**

**IN-to-Q Propagation Delay vs. Temperature**

## Functional Characteristics
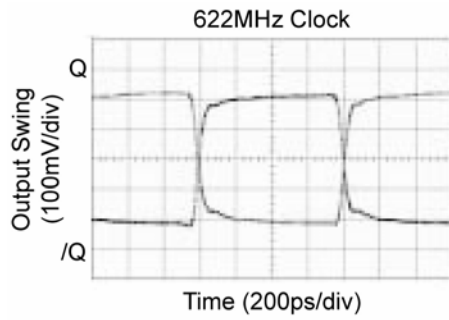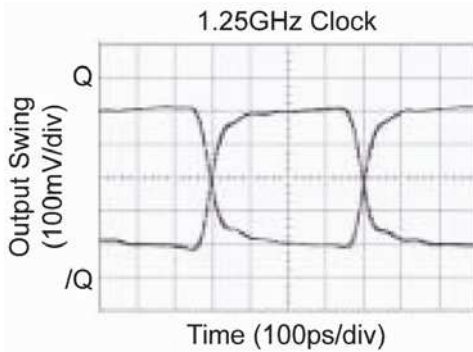


622MHz Clock

Output Swing (100mV/div)

Q

/Q

Time (200ps/div)

**10 K28.7 Clock Pattern**



1.25GHz Clock

Output Swing (100mV/div)

Q

/Q

Time (100ps/div)

**10 K28.7 Clock Pattern**



2.5GHz Clock

Outpu Swing (100mV/div)

Q

/Q

Time (50ps/div)

**10 K28.7 Clock Pattern**



7GHz Clock

Output Swing (50mV/div.)

Q

/Q

Time (20ps/div.)

**10 K28.7 Clock Pattern**



622Mbps Data ($2^{23}$–1 PRBS)

Output Swing (100mV/div)

Time (200ps/div)

**$2^{23}$–1 PRBS Pattern**



2.5Gbps Data ($2^{23}$–1 PRBS)

Output Swing (100mV/div)

Time (50ps/div)

**$2^{23}$–1 PRBS Pattern**



3.2Gbps Data ($2^{23}$–1 PRBS)

Output Swing (100mV/div)

Time (50ps/div)
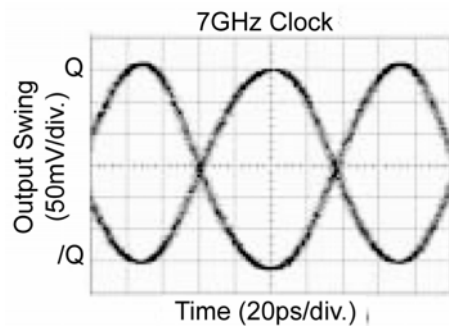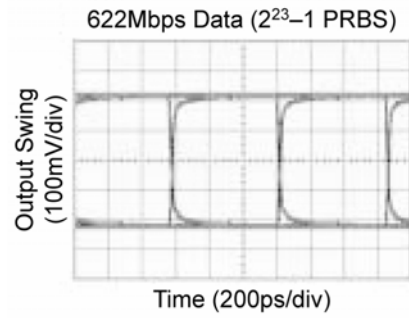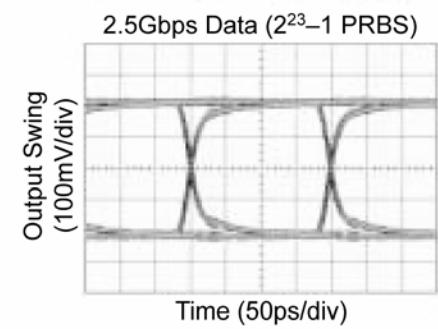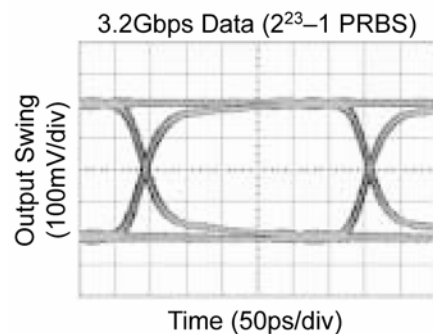
**$2^{23}$–1 PRBS Pattern**

# Input Interface Applications

| | | |
|---|---|---|
| <br>**Figure 3a. Static Input Level** | <br>**Figure 3b. LVDS Interface<br>(DC-Coupled)** | <br>**Figure 3c. CML Interface<br>(DC-Coupled)** |
| <br>**Figure 3d. CML Interface<br>(AC-Coupled)** | <br>**Figure 3e. PECL Interface<br>(DC-Coupled)** | <br>**Figure 3f. PECL Interface<br>(AC-Coupled)** |

# Related Product and Support Documentation

| Part Number | Function | Data Sheet Link |
|---|---|---|
| SY58016L | 3.3V 10Gbps Differential CML Line Driver/Receiver with Internal Termination | http://www.micrel.com/product-info/products/sy58016l.shtml |
| SY58052U | 10Gbps Clock/Data Retimer with 50Ω Input Termination | www.micrel.com/product-info/products/sy58052u.shtml |
| | QFN® Application Note | www.amkor.com/products/notes_papers/MLF_AppNote_0902.pdf |
| HBW Solutions | New Products and Applications | www.micrel.com/product-info/products/solutions.shtml |

## 16-PIN *Micro*LeadFrame® (MLF-16)

Pin 1 Dot
By Marking

3.000±0.050

3.000±0.050

TOP VIEW

PIN #1 IDENTIFICATION
CHAMFER 0.300 X 45°

1.550±0.050
Exp. DAP

0.400±0.050

0.500 Bsc

1.550±0.050
Exp. DAP

0.230±0.050

0.400±0.050
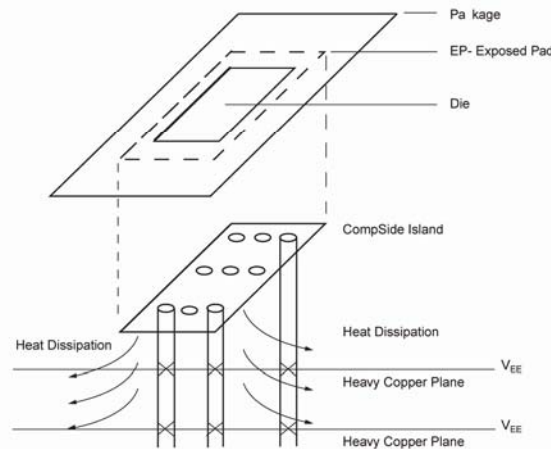
1.500
Ref.

BOTTOM VIEW

0.850±0.050

0.000–0.050

0.203±0.025
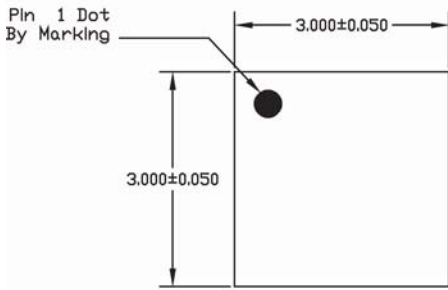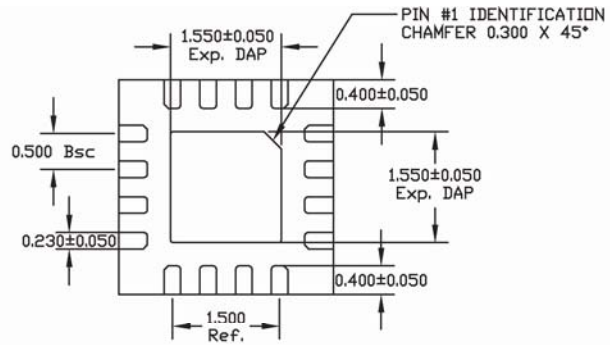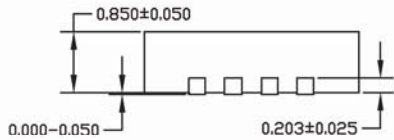
SIDE VIEW

NOTE:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. MAX. PACKAGE WARPAGE IS 0.05 mm.
3. MAXIMUM ALLOWABE BURRS IS 0.076 mm IN ALL DIRECTIONS.
4. PIN #1 ID ON TOP WILL BE LASER/INK MARKED.

Pa kage

EP- Exposed Pad

Die

CompSide Island

Heat Dissipation

Heat Dissipation

V_EE

Heavy Copper Plane

Heavy Copper Plane

V_EE

**PCB Thermal Consideration for 16-Pin QFN® Package**
**(Always solder, or equivalent, the exposed pad to the PCB)**

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TEL +1 (408) 944-0800  FAX +1 (408) 474-1000  WEB http://www.micrel.com