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125MHz TRIGGER PROGRAMMABLE TIMING EDGE VERNIER

FEATURES

■ **True 125MHz retrigger rate**

■ **Pin-compatible with Bt604**

■ **15ps delay resolution**

■ **Less than ± 1 LSB timing accuracy**

■ **Differential TRIGGER inputs**

■ **Delay spans from 4 to 40ns**

■ **Compatible with 10KH ECL logic**

■ **Lower power dissipation 350mW typical**

■ **Available in 28-pin plastic (PLCC) or metal (MLCC) J-lead package**

BLOCK DIAGRAM
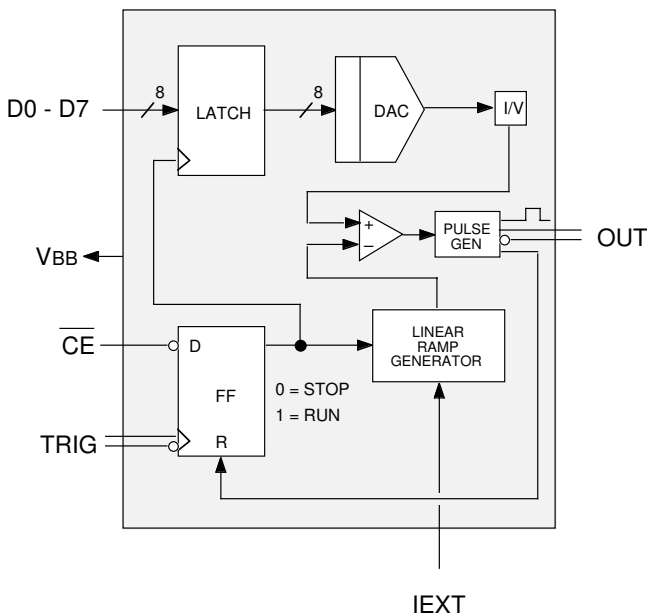
DESCRIPTION

Micrel-Synergy's SY604 is an ECL-compatible timing vernier (delay generator) whose time delay is programmed via an 8-bit code which is loaded concurrently with the circuit trigger. The SY604 is fabricated in Micrel-Synergy's proprietary ASSET™ bipolar process.

This device can be retriggered at speeds up to 125MHz, with a delay span as short as 4ns. At minimum span, the resolution is 4ns/255 = 15.7ps per step. The delay span is externally adjustable up to 40ns. The SY604 employs differential TRIGGER inputs, and produces a differential OUTPUT pulse; all other control signals are single-ended ECL. Edge delay is specified by an 8-bit input which is loaded into the device with the TRIGGER. The output pulse width will typically be 3.5ns.

The SY604 is commonly used in Automatic Test Equipment to provide precise timing edge placement; it is also found in many instrumentation and communications applications.

Micrel-Synergy's circuit design techniques coupled with ASSET™ technology result in not only ultra-fast performance, but allow device operation at lower power dissipation than competing technologies. Outstanding reliability is achieved in volume production.

PIN CONFIGURATION
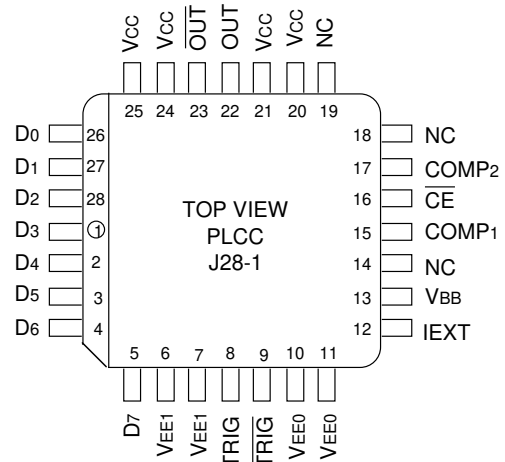
PIN DESCRIPTION

D0 – D7
Data input pins (ECL compatible). On the rising edge of TRIG, a ramp is initiated whereupon D0-D7 are latched into the device. D0 is the LSB. These inputs specify the amount of delay from the rising edge of TRIG to the output pulse.

$\overline{CE}$
Chip enable input (ECL compatible). $\overline{CE}$ must be a logical zero on the rising edge of TRIG to enable the device to respond to the trigger. If $\overline{CE}$ is floating, the trigger will always be enabled.

TRIG, $\overline{TRIG}$
Differential trigger inputs (ECL compatible). The rising edge of TRIG is used to trigger the delay cycle if $\overline{CE}$ is a logical zero. If $\overline{CE}$ is a logical one, no operation occurs. It is recommended that triggering be performed with differential inputs.

OUT, $\overline{OUT}$
Differential outputs (ECL compatible).

IEXT
Current reference pin. The amount of current sourced into this pin determines the span of output delay. The voltage at IEXT is typically –1.25V.

COMP1, COMP2
Compensation pins. A 0.1μF ceramic capacitor must be connected between COMP1 and VEE0, and COMP2 and VEE0 (see Figure 3).

VEE
Device power. All VEE pins must be connected.

VCC
Device ground. All VCC pins must be connected together.

VBB
A –1.36V (typical) output.

FUNCTIONAL DESCRIPTION

The output pulse generation cycle begins with the arrival of TRIG shown in **Figure 1**. When TRIG transitions to a high and $\overline{CE}$ is low, the values on D0 - D7 are latched, thereby setting the DAC values. Simultaneously with the latching of D0 - D7, the linear ramp generator is enabled.

When the ramp level reaches that of the DAC, the comparator initiates the pulse generator to produce an output pulse of fixed width. The generation of an output pulse resets the ramp and the cycle is ready to begin again.
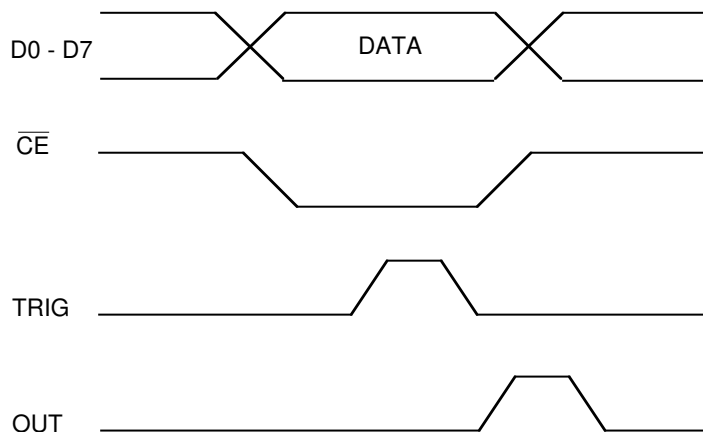

Figure 1.

ABSOLUTE MAXIMUM RATING[1]

Symbol	Parameter	Value	Unit
VEE	Power Supply (VCC = 0V)	-8 to 0	V
VI	Input Voltage (VCC = 0V)	0 to VEE	V
IOUT	Output Current — Continuous — Surge	 50 100	mA
TA	Operating Temperature Range	0 to +85	˚C
VEE	Operating Range[2]	-5.7 to -4.2	V

NOTES:

1. Beyond which device life may be impaired.

2. Parametric values specified at 10E Series: - 4.75V to - 5.5V.

DC CHARACTERISTICS[1]

Symbol	Parameter	TA = +0˚C			TA = +25˚C			TA = +70˚C			Unit
		Min.	Typ.	Max.	MIn.	Typ.	Max.	Min.	Typ.	Max.	
VIH	Input HIGH Voltage (10K)	-1170	—	-840	-1130	—	-810	-1070	—	-735	mV
VIL	Input LOW Voltage (10K)	-1950	—	-1480	-1950	—	-1480	-1950	—	-1450	mV
VOH	Output HIGH Voltage (10K)	-1020	-975	-840	-980	-920	-810	-920	-850	-735	mV
VOL	Output LOW Voltage (10K)	-1950	-1755	-1630	-1950	-1750	-1630	-1950	-1720	-1600	mV
IIH IIH	Input High Current (Vin = VIH max) TRIG, $\overline{TRIG}$	— —	100 100	150 150	— —	100 100	150 150	— —	100 100	150 150	μA μA
IIL IIL	Input Low Current (Vin = VIL min) TRIG, $\overline{TRIG}$	— —	100 100	150 150	— —	100 100	150 150	— —	100 100	150 150	μA μA

DL
IL
	Output Delay Spans
	    Differential Linearity Error**
	    Integral Linearity Error**
		—
		—
			±0.84
			±1.16
				±0.9
				±1.25
					—
					—
						±0.84
						±0.89
							±0.9
							±1.0
								—
								—
									±0.84
									±0.89
										±0.9
										±1.0
											LSB

VBB	VBB Output Voltage	-1.44	—	-1.25	-1.44	-1.35	-1.25	-1.44	—	-1.25	V

IEXT	IEXT for Tspans
	    Tspan = 4ns
	    Tspan = 5ns
	    Tspan = 10ns
	    Tspan = 15ns
	    Tspan = 20ns
	    Tspan = 30ns
		1.80
		1.45
		0.70
		0.45
		0.34
		0.20
			2.38
			1.85
			0.93
			0.62
			0.46
			0.30
				2.80
				2.40
				1.20
				0.80
				0.60
				0.40
					1.80
					1.45
					0.70
					0.45
					0.34
					0.20
						2.38
						1.85
						0.93
						0.62
						0.46
						0.30
							2.80
							2.40
							1.20
							0.80
							0.60
							0.40
								1.80
								1.45
								0.70
								0.45
								0.34
								0.20
									2.38
									1.85
									0.93
									0.62
									0.46
									0.30
										2.80
										2.40
										1.20
										0.80
										0.60
										0.40
											mA
											mA
											mA
											mA
											mA
											mA

	Tspan with IEXT = 1.8 mA (Tspan = Tmax - Tmin)	4.1	—	6.5	4.1	—	6.5	4.1	—	6.5	ns

Tmin	Minimum Delay Time*
	    Data = 00, Tspan = 5ns
	    Tspan = 10ns
	    Tspan = 15ns
	    Tspan = 20ns
	    Tspan = 25ns
	    Tspan = 30ns
		—
		—
		—
		—
		—
		—
			2.8
			3.4
			4.0
			4.6
			5.2
			5.8
				3.8
				4.9
				6.0
				7.1
				8.2
				9.3
					—
					—
					—
					—
					—
					—
						2.8
						3.4
						4.0
						4.6
						5.2
						5.8
							3.8
							4.9
							6.0
							7.1
							8.2
							9.3
								—
								—
								—
								—
								—
								—
									2.8
									3.4
									4.0
									4.6
									5.2
									5.8
										3.8
										4.9
										6.0
										7.1
										8.2
										9.3
											ns
											ns
											ns
											ns
											ns
											ns

IEE	VEE Supply Current	—	—	100	—	70	100	—	—	100	mA

NOTE:

1. 10K series circuits are designed to meet the DC specifications shown in the table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained. Outputs are terminated through a 50Ω resistor to -2.0 volts.

AC CHARACTERISTICS

ECL input values are -0.9 to -1.7V, with input rise/fall times ≤ 2ns, measured between the 20% and 80% points. Timing reference points at 50% for inputs and outputs.

OUT and $\overline{OUT}$ loading with 50Ω to -2.0V. Typical values are based on nominal temperature, i.e., and nominal voltage, i.e., -5.2V.

Symbol	Parameter	$T_A = +0°C$			$T_A = +25°C$			$T_A = +70°C$			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
fMAX	Trigger Rate[1]	—	—	125	—	—	125	—	—	125	MHz
tWI	Trigger Width High	2.0	1.0	—	2.0	1.0	—	2.0	1.0	—	ns
tWO	Output Pulse Width High Time	2.5	3.5	4.5	2.5	3.5	4.5	2.5	3.5	4.5	ns
	Output Pulse Rise/Fall Time (20/80%)	—	550	750	—	550	750	—	550	750	ps
tS	Output Pulse Spacing Span = 4ns @ 1 LSB	8.0	—	—	8.0	—	—	8.0	—	—	ns
	Minimum Delay Time vs. Tspan Δ T00 / ns (Tspan = 5 to 10ns)	—	125	220	—	125	220	—	125	220	ps/ns
1 LSB 1 LSB	Output Delay Tspan (Tspan = Tmax - Tmin)	4.0	—	40	4.0	—	40	4.0	—	ns 40	ns
	Resolution (Tspan / 225)	15.7	—	157	15.7	—	157	15.7	—	157	ps
	Tempo (5ns Span) Δ Tspan / °C	—	2	—	—	2	—	—	2	—	ps/°C
	Δ Tmin / °C	—	2	—	—	2	—	—	2	—	ps/°C
	Power Supply Rejection (Data = 0-FF HEX, Tspan = 5ns)	—	60	—	—	60	—	—	60	—	ps/V
tS	$\overline{CE}$ Setup Time	2.0	—	—	2.0	—	—	2.0	—	—	ns
tH	$\overline{CE}$ Hold Time	1.5	—	—	1.5	—	—	1.5	—	—	ns
tWH	WRITE Pulse Width High Time	2.0	—	—	2.0	—	—	2.0	—	—	ns
tDS	D0 - D7 Setup Time	1.0	—	—	1.0	—	—	1.0	—	—	ns
tDH	D0 - D7 Hold Time	1.5	—	—	1.5	—	—	1.5	—	—	ns

NOTE:

1. See chart below:

Maximum Tspan and Trigger Rates

Maximum Tspan (ns) Maintaining Linearity	Minimum Trigger Periods (ns)
of ± 1 LSB	
4.0	8.0
5.1	10.0
5.8	11.1
6.75	12.5
8.1	14.3
9.9	16.6
12.0	20.0
15.5	25.0
22.0	33.3

The information in this table is guaranteed but not 100% production tested.

See **Figure 2** for a graphical representation.

TIMING DIAGRAMS
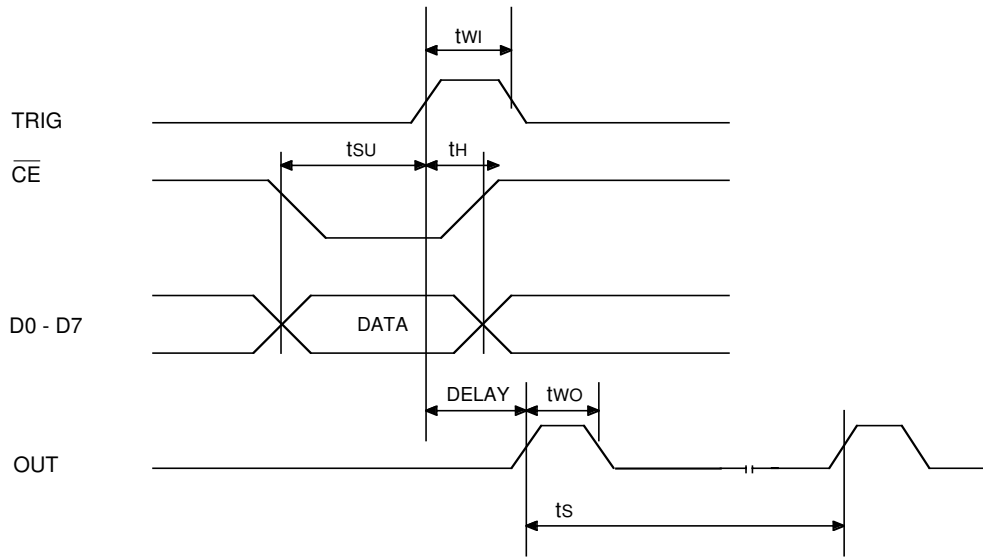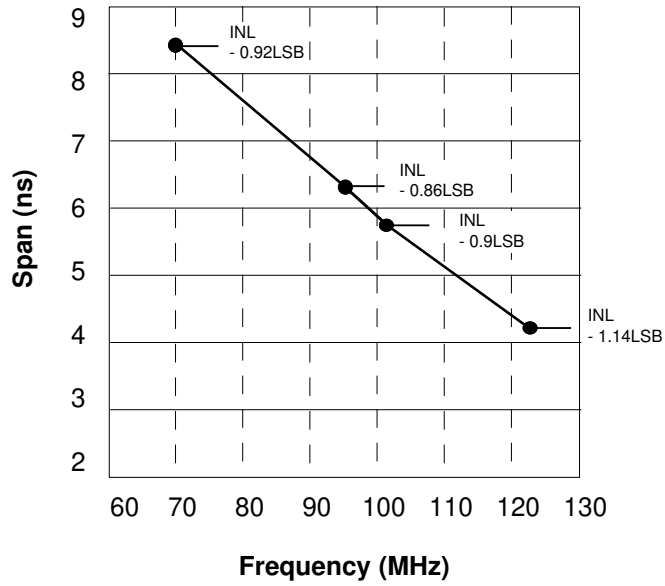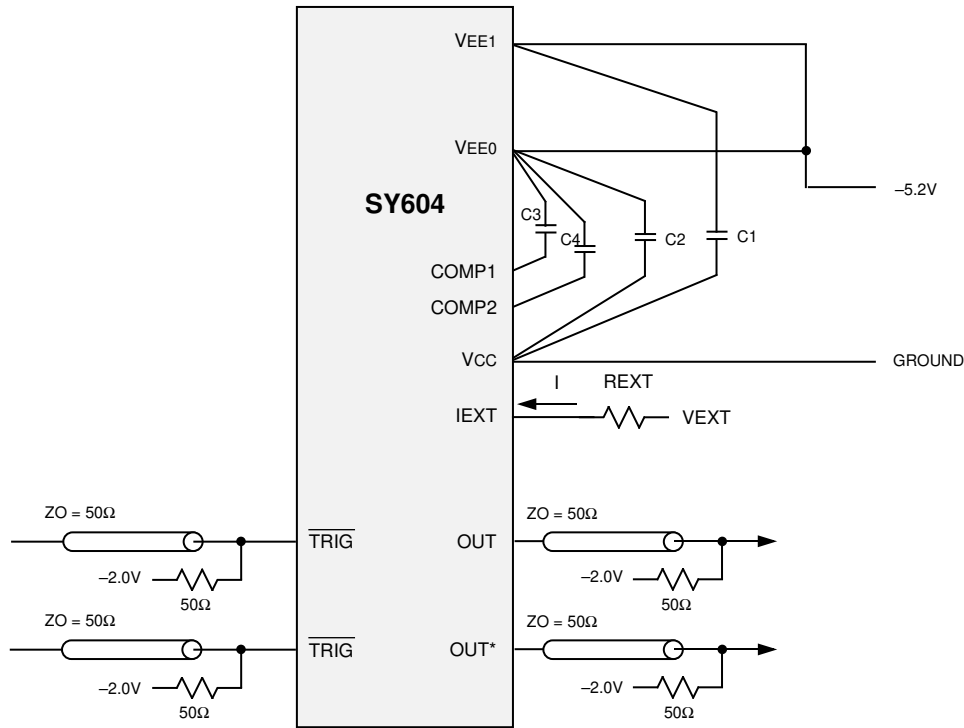

± 1 LSB
Span vs. Trigger Rates

Figure 2.

APPLICATION DIAGRAM

REXT Calculation:

REXT = (VEXT + 1.25V)/IEXT

For Example:

If Tspan is around 15ns, then IEXT is around 0.6mA, (see DC Characteristic Table) and assume IEXT pin is tied to V_{CC} with the resistor.

REXT = 0 + 1.25V/0.6mA

= 2.08K ohm

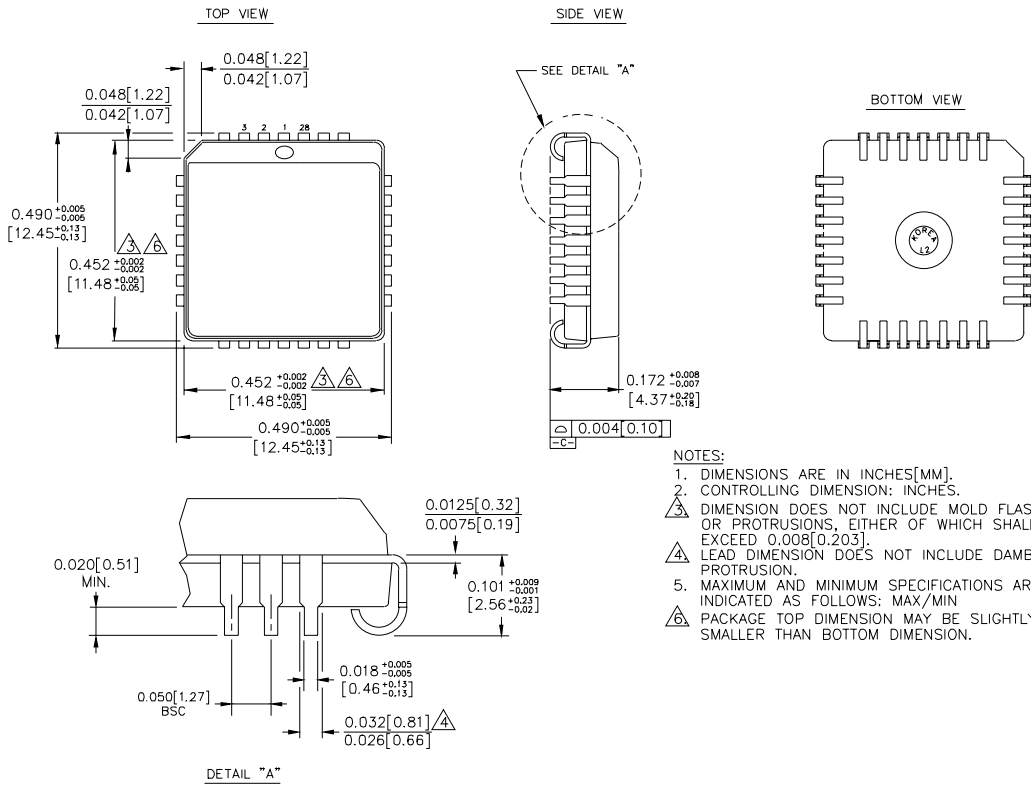| Location	Description	Vendor Part Number
C1–C4	0.1µF ceramic capacitor	Erie RPE112Z5U104M50V
REXT	1% metal film resistor (selected for proper Tspan)	CB301210 Dale CMF-55C

NOTE:

The vendor numbers above are listed only as a guide. Substitution of devices with similar characteristics will not affect the performance of the SY604. All devices should be as close as possible to the SY604.

Figure 3. Typical Connection Diagram and Parts List.

PRODUCT ORDERING CODE

Ordering Code	Package Type	Operating Range
SY604JC	J28-1	Commercial
SY604JCTR	J28-1	Commercial

28 LEAD PLCC (J28-1)

TOP VIEW

SIDE VIEW

BOTTOM VIEW

0.048[1.22] / 0.042[1.07]

0.048[1.22] / 0.042[1.07]

SEE DETAIL "A"

0.490 +0.005 -0.005 [12.45 +0.13 -0.13]

0.452 +0.002 -0.002 [11.48 +0.05 -0.05]

3 6

0.452 +0.002 -0.002 [11.48 +0.05 -0.05] 3 6

0.490 +0.005 -0.005 [12.45 +0.13 -0.13]

0.172 +0.008 -0.007 [4.37 +0.20 -0.18]

0.004[0.10] -C-

DETAIL "A"

0.0125[0.32] / 0.0075[0.19]

0.020[0.51] MIN.

0.101 +0.009 -0.001 [2.56 +0.23 -0.02]

0.018 +0.005 -0.005 [0.46 +0.13 -0.13]

0.050[1.27] BSC

0.032[0.81] 4 / 0.026[0.66]

NOTES:
1. DIMENSIONS ARE IN INCHES[MM].
2. CONTROLLING DIMENSION: INCHES.
3. DIMENSION DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS, EITHER OF WHICH SHALL NOT EXCEED 0.008[0.203].
4. LEAD DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION.
5. MAXIMUM AND MINIMUM SPECIFICATIONS ARE INDICATED AS FOLLOWS: MAX/MIN
6. PACKAGE TOP DIMENSION MAY BE SLIGHTLY SMALLER THAN BOTTOM DIMENSION.

Rev. 03