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SY75578L

PCIe Fanout Buffer
267MHz, 8 HCSL Outputs with 2 Input MUX

PrecisionEdge™

General Description

The SY75578L is a high-speed, fully differential 1:8 clock fanout buffer optimized to provide eight identical output copies with 130fs phase jitter and maximum 100ps output-to-output skew. Designed to be used with PCI-Express applications, SY75578L accepts HCSL/LVDS and outputs HCSL logic levels.

The SY75578L operates from a 3.3V ±5% power supply and is guaranteed over the full industrial temperature range (–40°C to +85°C). It is available in a 32 pin QFN lead-free package.

The SY75578L is part of Micrel's high-speed, ultra-low jitter, PrecisionEdge™ product line.

Datasheets and support documentation are available on Micrel's web site at: www.micrel.com.

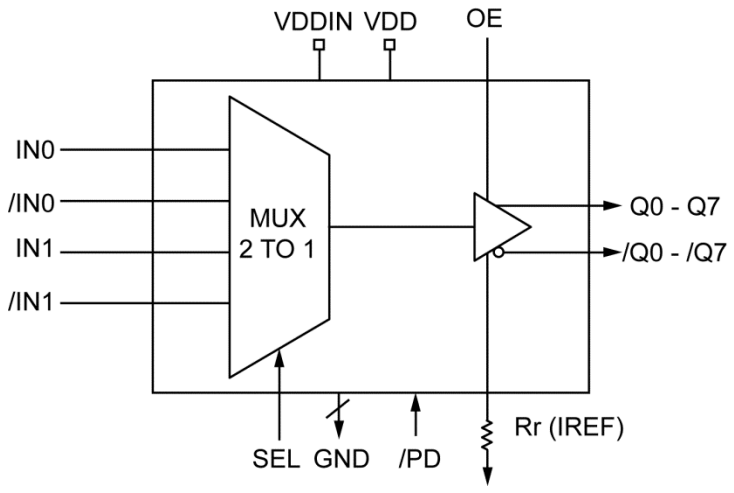
Features

- Eight differential pairs of HCSL outputs
- Two pairs of differential inputs accept LVDS or HCSL logic levels
- 267MHz max frequency
- Ultra low phase jitter:
  - 130fs$_{rms}$, 200MHz (12kHz–20MHz)
- <100ps output-to-output skew
- 3.3V ±5% power supply operation
- –40°C to +85°C Industrial operating temperature
- Available in 32-pin QFN lead-free package

Applications

- Blade servers
- Desktop servers
- Workstations
- Storage area networks
- IP routers and switches
- Telecom and datacom
- High performance computing

Functional Block Diagram



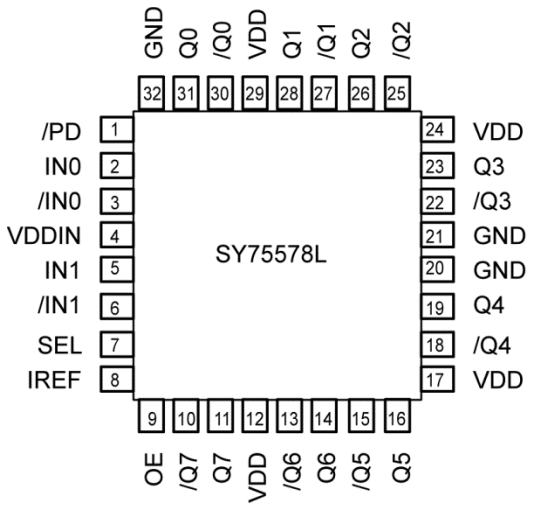
Ordering Information[1]

Part Number	Package Type	Operating Range	Package Marking	Lead Finish
SY75578LMG	QFN-32	Industrial	SY75578L with Pb-Free bar-line indicator	NiPdAu
SY75578LMG TR[2]	QFN-32	Industrial	SY75578L with Pb-Free bar-line indicator	NiPdAu

Notes:

1. Contact factory for die availability. Dice are guaranteed at $T_A = 25°C$, DC Electricals only.
2. Tape and Reel.

Pin Configuration



32-Pin QFN

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Pin Description

Pin Number	Pin Name	Pin Function
7	SEL	Single-Ended Input: This single-ended TTL/CMOS compatible input selects the inputs to the multiplexer. Note that this input is internally connected to a pull-up resistor and will default to logic HIGH state if left open. SEL = 1 propagates IN0, /IN0 to outputs. SEL=0 propagates IN1, /IN1 to outputs.
4	VDDIN	Positive Power Supply: 3.3V Power supply. Bypass with 0.1µF||0.01µF low ESR capacitors as close to the V_{DDIN} pin as possible.
2, 3 5, 6	IN0, /IN0 IN1, /IN1	HCSL/LVDS Differential Input Pairs: These input pairs accept HCSL or LVDS differential signal inputs.
1	/PD	PD = 0 powers down the chip and tri-states outputs. Pin is attached to an internal pull-up resistor.
9	OE	Single-Ended Input: This TTL/CMOS input disables and enables the Q0-Q7outputs. OE is asynchronous. High = enable outputs, Low = tri-state outputs. Internal pull-up resistor makes outputs enabled by default.
20, 21, 32	GND, EXPOSED PAD	Ground: Exposed pad must be connected to a ground plane that is the same potential as the ground pins
8	IREF	External resistor between pin Iref and GND controls reference current.
11, 10 14, 13 16, 15 19, 18 23, 22 26, 25 28, 27 31, 30	Q7, /Q7 Q6, /Q6 Q5, /Q5 Q4, /Q4 Q3, /Q3 Q2, /Q2 Q1, /Q1 Q0, /Q0	HCSL Differential Output Pairs: Differential buffered output copies of the selected input signal. These differential outputs are a logic function of the IN0, IN1, and SEL inputs.
12, 17, 24, 29	VDD	Positive Power Supply: 3.3V Power supply. Bypass with 0.1µF||0.01µF low ESR capacitors as close to the V_{DD} pins as possible.

Absolute Maximum Ratings[3]

Supply Voltage (V_{DD}, V_{DDIN}) 5.5V
Input Voltage (V_{IN}) ..... –0.5V to V_{DDIN} + 0.5V
Lead Temperature (soldering, 20s) ..... 260°C
Maximum Junction Temperature ..... 125°C
Storage Temperature (T_s) ..... –65°C to +150°C
ESD Protection (input) ..... 2000V min.

Operating Ratings[4]

Supply Voltage (V_{DD}, V_{DDIN}) ..... 3.135V to 3.465V
Ambient Op Temperature (T_A) ..... –40°C to +85°C
Package Thermal Resistance[5]
QFN-32
Still-air (θ_{JA}) ..... 50°C/W
Junction-to-Board (θ_{JB}) ..... 20°C/W

Electrical Characteristics[5]

V_{DD} = V_{DDIN} = 3.135V to 3.465V, T_A = –40°C to +85°C, unless otherwise stated. Rref = 475Ω

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{DD}, V_{DDIN}	Power Supply Voltage Range		3.135	3.3	3.465	V
R_{out}	Output Resistance		3			kΩ
$R_{pull\ up}$	Pull up Resistance	SEL, /PD, OE		110		kΩ
V_{IH}	Input High Voltage	SEL, /PD, OE	2		V_{DDIN} + 0.3	V
V_{IL}	Input Low Voltage	SEL, /PD, OE	–0.3		0.8	V
V_{IH}	Input High Voltage	HCSL, IN, /IN	660	750	850	mV
V_{IL}	Input Low Voltage		–150	0		
V_{IN}	Input Voltage Swing	LVDS, IN, /IN	250	350	450	mV
$V_{input\ offset}$	Input Common Mode Voltage	LVDS, IN, /IN,	1.125	1.25	1.375	V
V_{OH}	Output High Voltage	HCSL	660	750	850	mV
V_{OL}	Output Low Voltage	HCSL	–150	0	27	mV
Vcross[7, 8]	Crossing Point Voltage	Absolute	250	350	550	mV
Vcross_variation[7, 8, 9]	Variation of Crossing Point Voltage	Variation over all edges			140	mV
I_{DD}	Power Supply Current For V_{DD} + V_{DDIN}	Load 50Ω, 2pF		140	200	mA
		No load, /PD = Low			0.4	mA
		OE = Logic Low			20	mA
I_{IL}[10]	Input Leakage Current	0 < V_{IN} < V_{DDIN}	–5		5	µA

Notes:

3. Permanent device damage may occur if absolute maximum ratings are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this datasheet. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.
4. The datasheet limits are not guaranteed if the device is operated beyond the operating ratings.
5. Package thermal resistance assumes that the exposed pad is soldered (or equivalent) to the device's most negative potential on the PCB. ψ_{JB} and θ_{JA} values are determined for a 4-layer board in still-air unless otherwise stated. The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.
6. The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.
7. Test setup is R_L = 50Ω with 2pF, Rr = 475Ω ±1%.
8. Measurement taken from Q and /Q.
9. Measured at the crossing point where instantaneous voltages of Q and /Q are equal.
10. Inputs with pull-up/pull-down resistances are not included.

AC Electrical Characteristics[6]

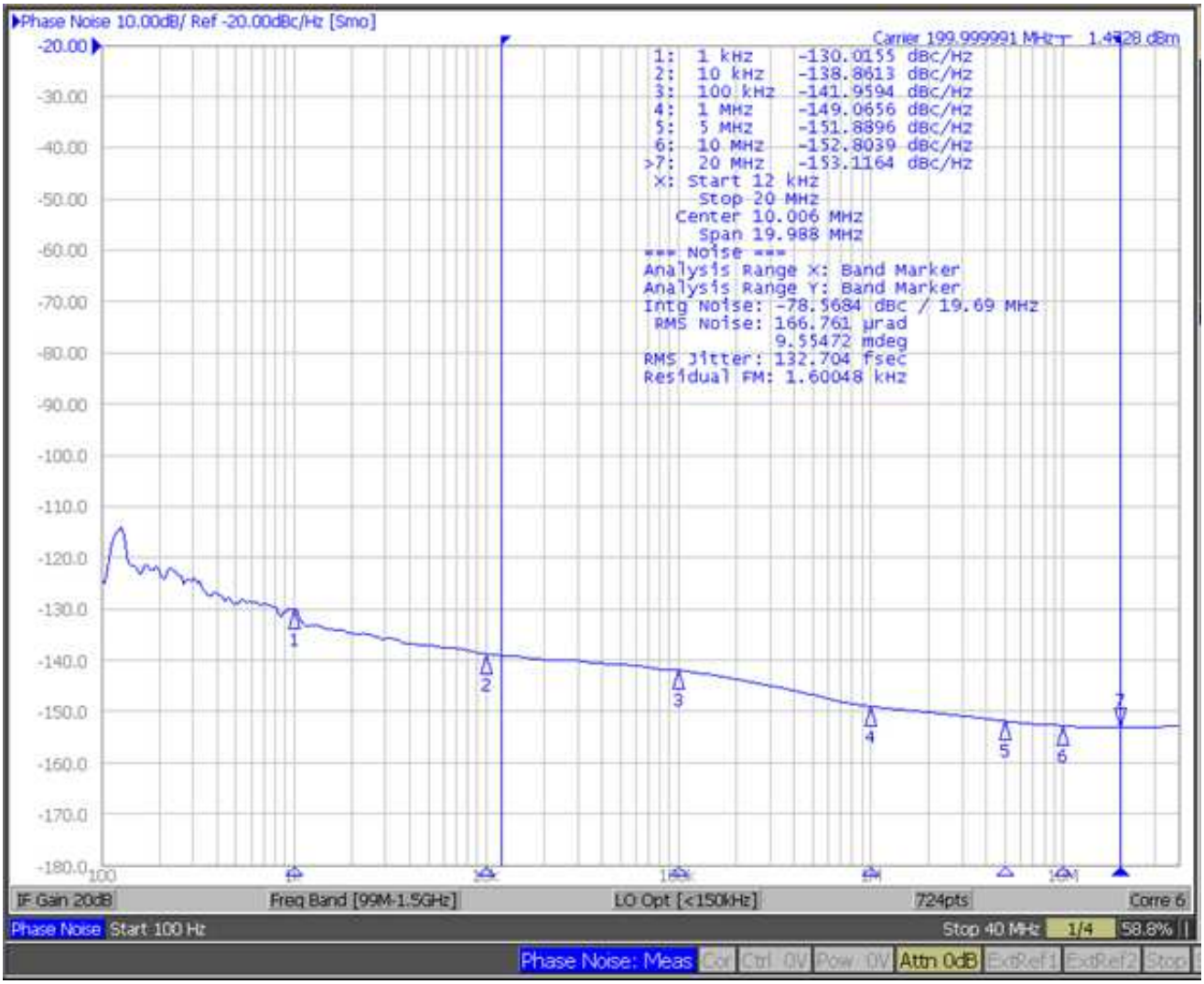
V_{DD} = V_{DDIN} = 3.135V to 3.465V, T_A = –40°C to +85°C, unless otherwise stated.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
f_{MAX}	Maximum Frequency		267			MHz
t_{PD}	Propagation Delay	Note 11		2	3	ns
t_{Skew}	Output-to-Output skew	Notes 12, 13			100	ps
t_R, t_F	Output Rise/Fall Times 0.175V to 0.525V / 0.525V to 0.175V	At full output swing. 50Ω, 2pF	150	350	650	ps
T_{RJ_Jitter}	Phase Jitter	At 200MHz		130		fs_{rms}
		At 156.25MHz		150		fs_{rms}
		At 100MHz		200		fs_{rms}
T_{OE_enable}	Output Enable Time	All Outputs		2		µs
$T_{OE\_disable}$	Output Disable Time	All Outputs		10		ns
T_{DCY}	Duty Cycle		45	50	55	%

Notes:

11. Measured from the differential input crossing point to the differential output crossing point.
12. Output-to-Output skew is the difference in time between outputs, receiving data from the same input, for the same temperature, voltage, and transition.
13. This parameter is defined in accordance with JEDEC Standard 65.

Phase Noise Plots



Phase jitter = 132fs$_{rms}$, 200MHz carrier frequency; integration range: 12kHz–20MHz

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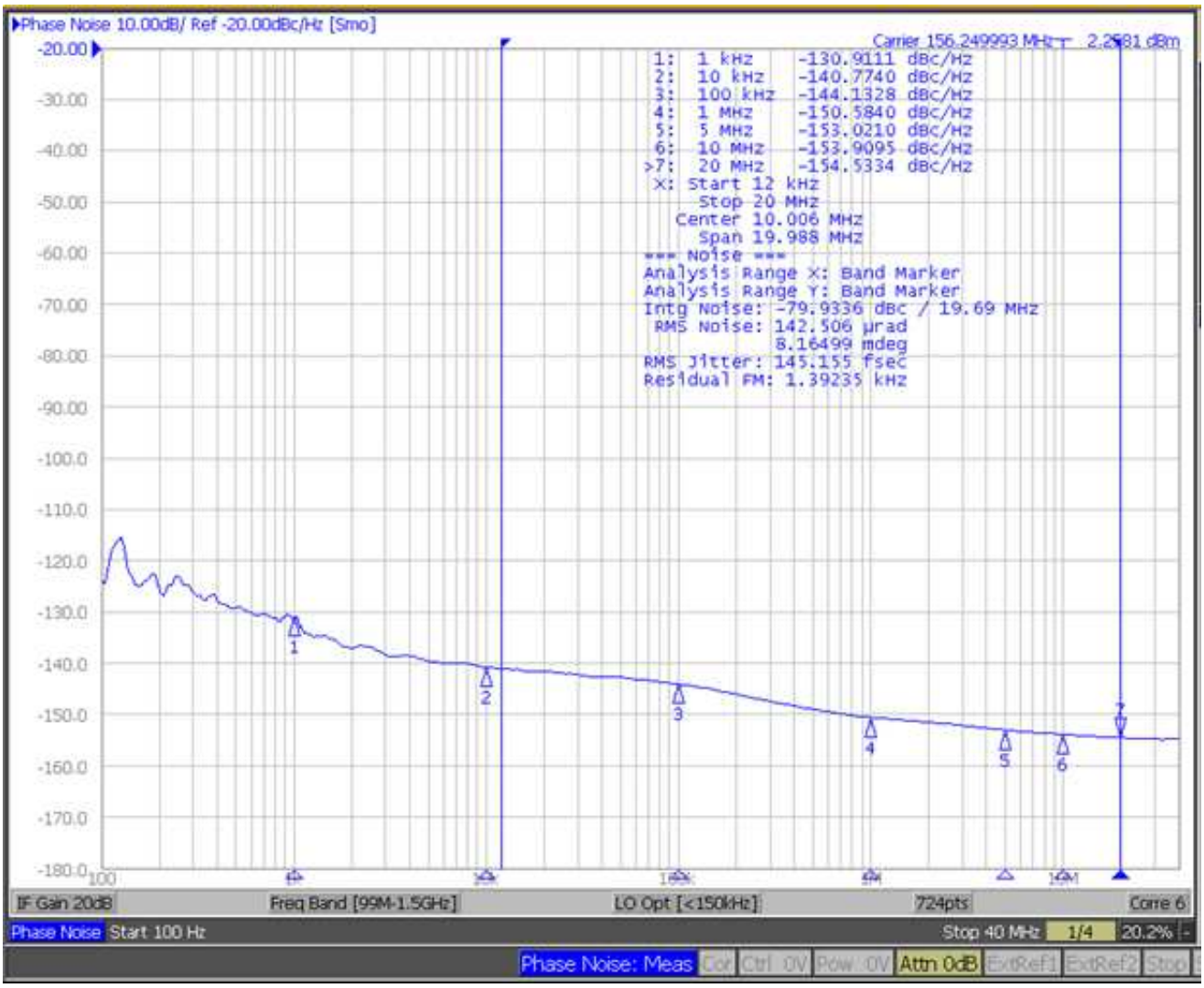

Phase jitter = 145fs$_{rms}$, 156.25MHz carrier frequency; integration range: 12kHz–20MHz

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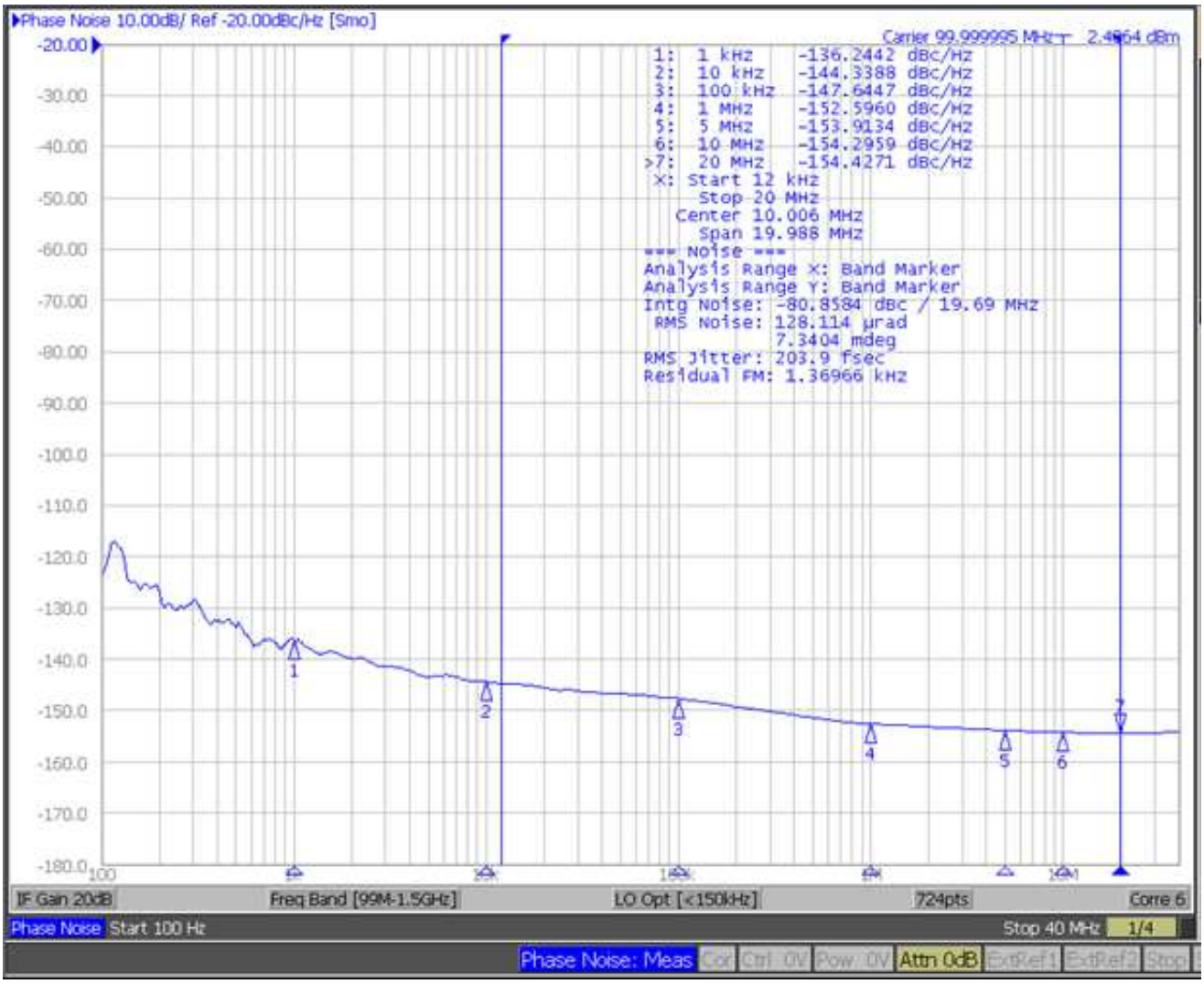
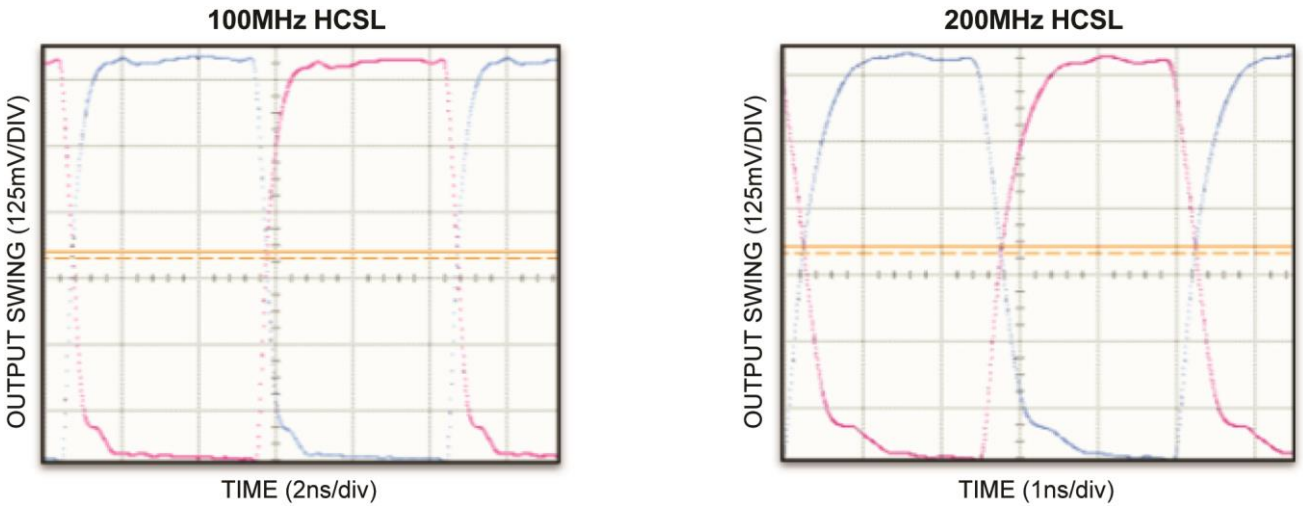
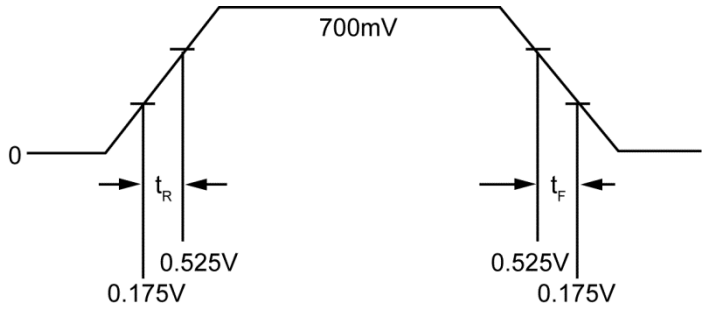


Phase jitter = 204fs$_{rms}$, 100MHz carrier frequency; integration range: 12kHz–20MHz

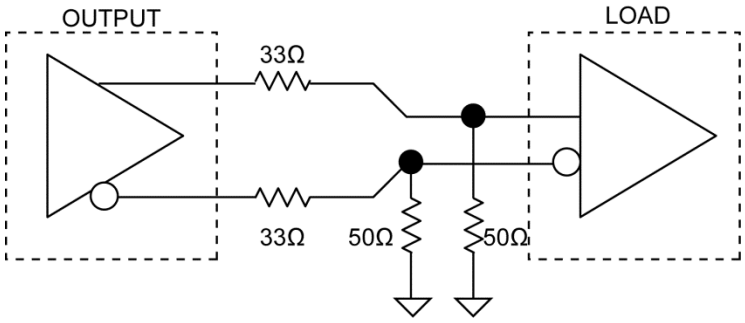
Functional Characteristics



HCSL Waveform Diagram



HCSL Interface Application



PCI-Express Device Routing

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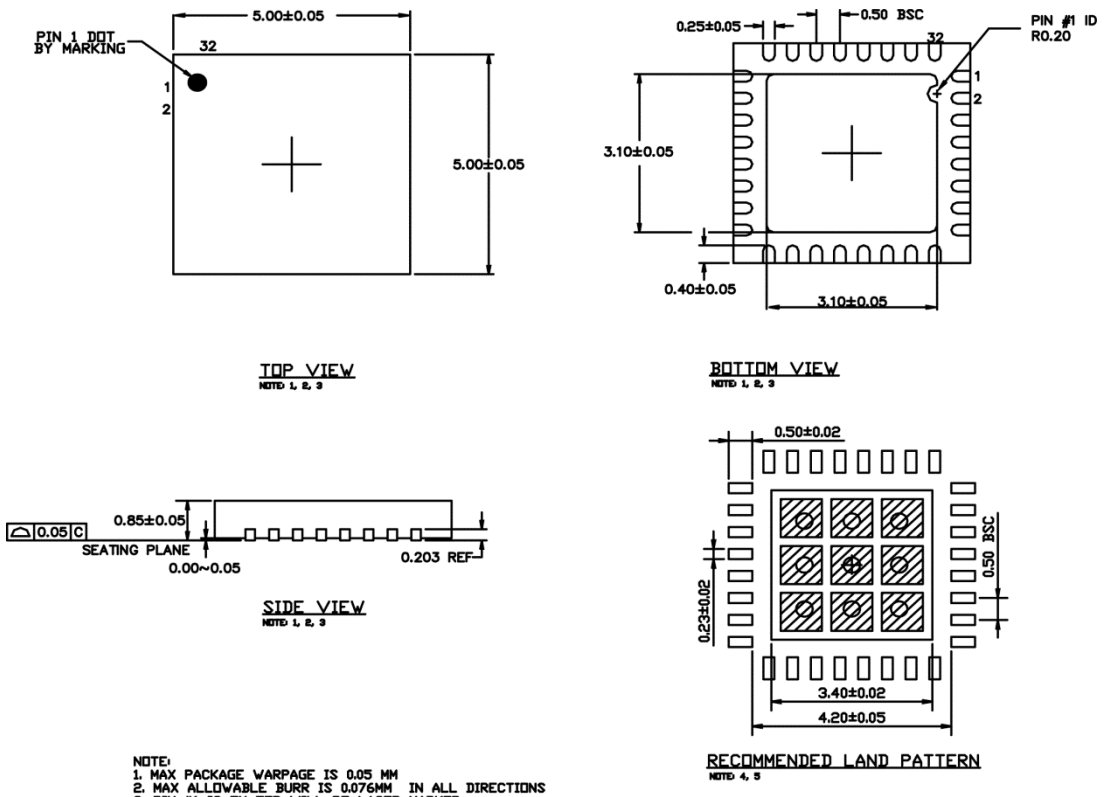
Package Information[14]



32-Pin QFN

Note:

14. Package information is correct as of the publication date. For updates and most current information, go to www.micrel.com.

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