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## SY88347DL

### 3.3V, 3.2Gbps PECL Limiting Post Amplifier with High-Gain TTL Loss-of-Signal

#### General Description

The SY88347DL low-power limiting post amplifier is designed for use in fiber-optic receivers. The device connects to typical transimpedance amplifiers (TIAs). The linear signal output, from TIAs, can contain significant amounts of noise and may vary in amplitude over time. The SY88347DL quantizes these signals and outputs PECL-level waveforms.

The SY88347DL operates from a single +3.3V power supply, over temperatures ranging from  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ . With its wide bandwidth and high gain, signals with data rates up to 3.2Gbps, and as small as  $5\text{mV}_{\text{PP}}$ , can be amplified to drive devices with PECL inputs.

The SY88347DL generates a high-gain loss-of-signal (LOS) open-collector TTL output. The LOS function has a high-gain input stage for increased sensitivity. A programmable loss-of-signal level set pin ( $\text{LOS}_{\text{LVL}}$ ) sets the sensitivity of the input amplitude detection. LOS asserts high if the input amplitude falls below the threshold sets by  $\text{LOS}_{\text{LVL}}$  and de-asserts low otherwise. The enable bar input ( $/\text{EN}$ ) de-asserts the true output signal without removing the input signal. The LOS output can be fed back to the  $/\text{EN}$  input to maintain output stability under a loss-of-signal condition. Typically, 3.3dB LOS hysteresis is provided to prevent chattering.

Datasheet and support documentation can be found on Micrel's web site at: [www.micrel.com](http://www.micrel.com).

#### Features

- Single 3.3V power supply
- 155Mbps to 3.2Gbps operation
- Low-noise PECL data outputs
- High-gain LOS output
- Chatter-free Open-Collector TTL Loss-of-Signal (LOS) output
- TTL  $/\text{EN}$  input
- Programmable LOS level set ( $\text{LOS}_{\text{LVL}}$ )
- Ideal for multi-rate applications
- Available in a tiny 10-pin EPAD-MSOP

#### Applications

- APON, BPON, EPON, GEPON, and GPON
- Gigabit Ethernet
- 1X and 2X Fibre Channel
- SONET/SDH:OC-3/12/24/48 – STM 1/4/8/16
- High-gain line driver and line receiver

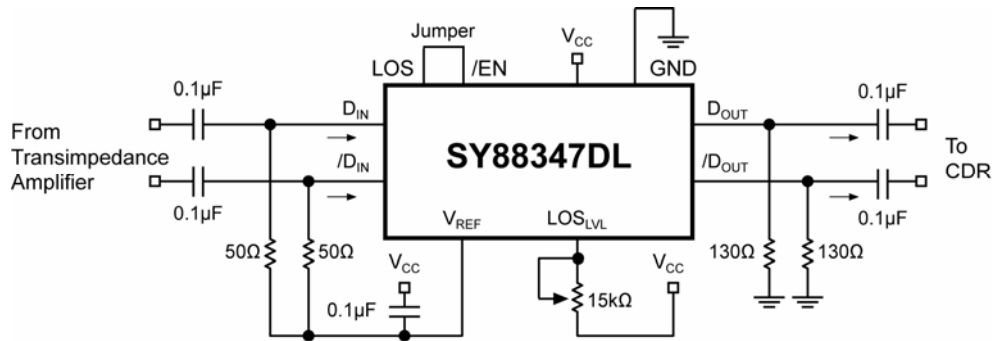
#### Markets

- FTTP
- Optical transceivers
- Datacom/Telecom
- Low-gain TIA interface
- Long reach FOM

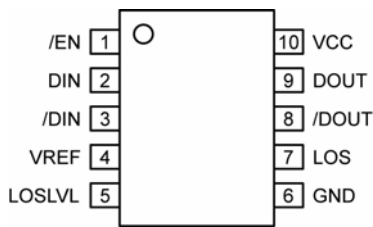
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### Typical Application



### Pin Configuration



10-Pin EPAD-MSOP (K10-2)

### Ordering Information

| Part Number                  | Package Type | Operating Range | Package Marking                      | Lead Finish |
|------------------------------|--------------|-----------------|--------------------------------------|-------------|
| SY88347DLEY                  | K10-2        | Industrial      | 347D with Pb-Free bar line indicator | Matte-Sn    |
| SY88347DLEYTR <sup>(1)</sup> | K10-2        | Industrial      | 347D with Pb-Free bar line indicator | Matte-Sn    |

**Note:**

- 1. Tape and Reel.

## Pin Description

| Pin Number MSOP | Pin Name            | Type                        | Pin Function   |
|-----------------|---------------------|-----------------------------|--|
| 1               | /EN                 | TTL Input: Default is HIGH. | /Enable: This input enables the outputs when it is LOW. Note that this input is internally connected to a 25k $\Omega$ pull-up resistor and will default to logic HIGH state if left open. |
| 2               | DIN                 | Data Input                  | True data input.   |
| 3               | /DIN                | Data Input                  | Complementary data input.  |
| 4               | VREF                |                             | Reference Voltage: Bypass with 0.1 $\mu$ F low ESR capacitor from VREF to V <sub>CC</sub> to stabilize LOS <sub>LVL</sub> and V <sub>REF</sub> .   |
| 5               | LOSLVL              | Input                       | Loss-of-Signal Level Set: a resistor from this pin to V <sub>CC</sub> sets the threshold for the data input amplitude at which LOS will be asserted.                                       |
| 6               | GND,<br>Exposed Pad | Ground                      | Device ground. GND and Exposed pad are to be tied to the same ground plane.  |
| 7               | LOS                 | Open-collector TTL output   | Loss-of-Signal: asserts high when the data input amplitude falls below the threshold set by LOS <sub>LVL</sub> .   |
| 8               | /DOUT               | PECL Output                 | Complementary data output.   |
| 9               | DOUT                | PECL Output                 | True data output.  |
| 10              | VCC                 | Power Supply                | Positive power supply.   |



### Absolute Maximum Ratings<sup>(1)</sup>

Supply Voltage (V<sub>CC</sub>) ..... 0V to +4.0V  
 Input Voltage (DIN, /DIN) ..... 0 to V<sub>CC</sub>  
 Output Current (I<sub>OUT</sub>)  
     Continuous ..... ±50mA  
     Surge ..... ±100mA  
 /EN Voltage ..... 0 to V<sub>CC</sub>  
 V<sub>REF</sub> Current ..... -800µA to +500µA  
 LOS<sub>LVL</sub> Voltage ..... V<sub>REF</sub> to V<sub>CC</sub>  
 Lead Temperature (soldering, 20sec.) ..... 260°C

Storage Temperature (T<sub>s</sub>) ..... -65°C to +150°C

### Operating Ratings<sup>(2)</sup>

Supply Voltage (V<sub>CC</sub>) ..... +3.0V to +3.6V  
 Ambient Temperature (T<sub>A</sub>) ..... -40°C to +85°C  
 Junction Temperature (T<sub>J</sub>) ..... -40°C to +125°C  
 Junction Thermal Resistance<sup>(3)</sup>  
     EPAD-MSOP  
     θ<sub>JA</sub> (Still-Air) ..... 38°C/W  
     ψ<sub>JB</sub> ..... 22°C/W

### DC Electrical Characteristics

V<sub>CC</sub> = 3.0V to 3.6V; R<sub>L</sub> = 50Ω to V<sub>CC</sub>-2V; T<sub>A</sub> = -40°C to +85°C; typical values at V<sub>CC</sub> = 3.3V, T<sub>A</sub> = 25°C.

| Symbol              | Parameter                  | Condition      | Min                    | Typ                    | Max                    | Units |
|---------------------|----------------------------|----------------|------------------------|------------------------|------------------------|-------|
| I <sub>CC</sub>     | Power Supply Current       | No output load |                        | 40                     | 60                     | mA    |
| V <sub>LOSLVL</sub> | LOS <sub>LVL</sub> Voltage |                | V <sub>REF</sub>       |                        | V <sub>CC</sub>        | V     |
| V <sub>OH</sub>     | PECL Output HIGH Voltage   |                | V <sub>CC</sub> -1.085 | V <sub>CC</sub> -0.955 | V <sub>CC</sub> -0.880 | V     |
| V <sub>OL</sub>     | PECL Output LOW Voltage    |                | V <sub>CC</sub> -1.880 | V <sub>CC</sub> -1.705 | V <sub>CC</sub> -1.555 | V     |
| V <sub>OFFSET</sub> | Differential Output Offset |                |                        |                        | ±120                   | mV    |
| V <sub>REF</sub>    | Reference Voltage          |                | V <sub>CC</sub> -1.48  | V <sub>CC</sub> -1.32  | V <sub>CC</sub> -1.16  | V     |
| V <sub>IHCMR</sub>  | Input Common Mode Range    |                | GND+2.0                |                        | V <sub>CC</sub>        | V     |

### TTL DC Electrical Characteristics

V<sub>CC</sub> = 3.0V to 3.6V; T<sub>A</sub> = -40°C to +85°C.

| Symbol          | Parameter              | Condition   | Min  | Typ | Max       | Units    |
|-----------------|------------------------|---|------|-----|-----------|----------|
| V <sub>IH</sub> | /EN Input HIGH Voltage |   | 2.0  |     |           | V        |
| V <sub>IL</sub> | /EN Input LOW Voltage  |   |      |     | 0.8       | V        |
| I <sub>IH</sub> | /EN Input HIGH Current | V <sub>IN</sub> = 2.7V<br>V <sub>IN</sub> = V <sub>CC</sub> |      |     | 20<br>100 | µA<br>µA |
| I <sub>IL</sub> | /EN Input LOW Current  | V <sub>IN</sub> = 0.5V                                      | -300 |     |           | µA       |
| I <sub>OH</sub> | LOS Output Leakage     | V <sub>OH</sub> = 3.6V                                      |      |     | 100       | µA       |
| V <sub>OL</sub> | LOS Output LOW Level   | I <sub>OL</sub> = +2mA                                      |      |     | 0.5       | V        |

#### Notes:

1. Permanent device damage may occur if absolute maximum ratings are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. The data sheet limits are not guaranteed if the device is operated beyond the operating ratings.
3. Thermal performance assumes the use of a 4-layer PCB. Exposed pad must be soldered (or equivalent) to the device's most negative potential on the PCB.

## AC Electrical Characteristics

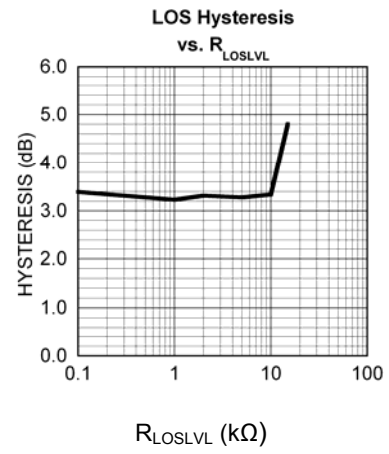
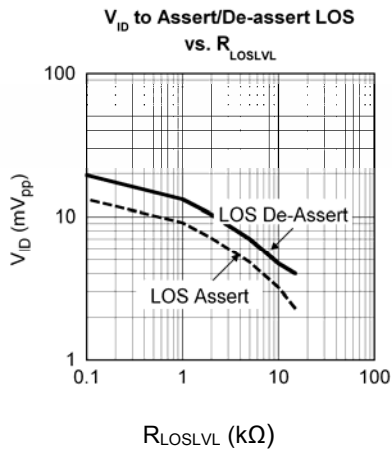
$V_{CC} = 3.0V$  to  $3.6V$ ;  $R_L = 50\Omega$  to  $V_{CC}-2V$ ;  $T_A = -40^\circ C$  to  $+85^\circ C$ ; typical values at  $V_{CC} = 3.3V$ ,  $T_A = +25^\circ C$ .

| Symbol        | Parameter                             | Condition                          | Min | Typ     | Max  | Units                                 |
|---------------|---------------------------------------|------------------------------------|-----|---------|------|---------------------------------------|
| $t_r, t_f$    | Output Rise/Fall Time<br>(20% to 80%) | Note 4                             |     |         | 150  | ps                                    |
| $t_{JITTER}$  | Deterministic<br>Random               | Note 5<br>Note 6                   |     | 15<br>5 |      | ps <sub>PP</sub><br>ps <sub>RMS</sub> |
| $V_{ID}$      | Differential Input Voltage Swing      | Figure 1                           | 5   |         | 1800 | mV <sub>PP</sub>                      |
| $V_{OD}$      | Differential Output Voltage Swing     | $V_{ID} \geq 12mV_{PP}$ , Figure 1 |     | 1500    |      | mV <sub>PP</sub>                      |
| $T_{OFF}$     | LOS Release Time                      |                                    |     | 2       | 10   | μs                                    |
| $T_{ON}$      | LOS Assert Time                       |                                    |     | 2       | 10   | μs                                    |
| $LOS_{AL}$    | Low LOS Assert Level                  | $R_{LOSLVL} = 15k\Omega$ , Note 8  |     | 2.3     |      | mV <sub>PP</sub>                      |
| $LOS_{DL}$    | Low LOS De-assert Level               | $R_{LOSLVL} = 15k\Omega$ , Note 8  |     | 4.0     |      | mV <sub>PP</sub>                      |
| $HYS_L$       | Low LOS Hysteresis                    | $R_{LOSLVL} = 15k\Omega$ , Note 7  |     | 4.8     |      | dB                                    |
| $LOS_{AM}$    | Medium LOS Assert Level               | $R_{LOSLVL} = 5k\Omega$ , Note 8   | 2   | 4.8     |      | mV <sub>PP</sub>                      |
| $LOS_{DM}$    | Medium LOS De-assert Level            | $R_{LOSLVL} = 5k\Omega$ , Note 8   |     | 7       | 9    | mV <sub>PP</sub>                      |
| $HYS_M$       | Medium LOS Hysteresis                 | $R_{LOSLVL} = 5k\Omega$ , Note 7   | 2   | 3.3     | 4.5  | dB                                    |
| $LOS_{AH}$    | High LOS Assert Level                 | $R_{LOSLVL} = 100\Omega$ , Note 8  | 10  | 13.2    |      | mV <sub>PP</sub>                      |
| $LOS_{DH}$    | High LOS De-assert Level              | $R_{LOSLVL} = 100\Omega$ , Note 8  |     | 19.5    | 23   | mV <sub>PP</sub>                      |
| $HYS_H$       | High LOS Hysteresis                   | $R_{LOSLVL} = 100\Omega$ , Note 7  | 2   | 3.4     | 4.5  | dB                                    |
| $B_{-3dB}$    | 3dB Bandwidth                         |                                    |     | 2       |      | GHz                                   |
| $A_{V(Diff)}$ | Differential Voltage Gain             |                                    |     | 42      |      | dB                                    |
| $S_{21}$      | Single-ended Small-Signal Gain        |                                    | 30  | 36      |      | dB                                    |

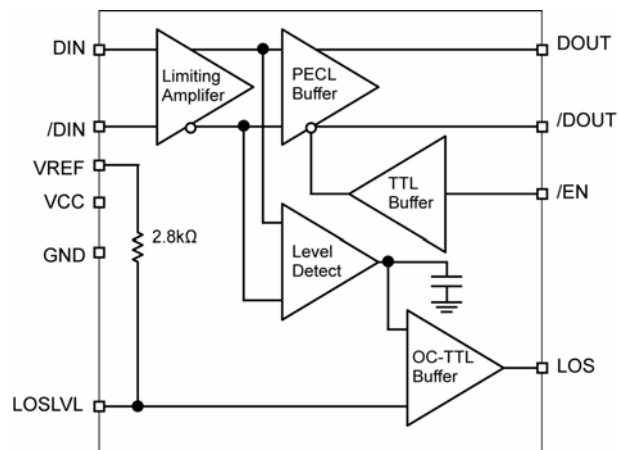
### Notes:

- Amplifier in limiting mode. Input is a 200MHz, 100mVpp square wave.
- Deterministic jitter measured using 3.2Gbps K28.5 pattern,  $V_{ID} = 10mV_{PP}$ .
- Random jitter measured using 3.2Gbps K28.7 pattern,  $V_{ID} = 10mV_{PP}$ .
- This specification defines electrical hysteresis as  $20\log(\text{LOS De-assert/LOS Assert})$ . The ratio between optical hysteresis and electrical hysteresis is found to vary between 1.5 and 2, depending upon the level of received optical power and ROSA characteristics. Based upon that ratio, the optical hysteresis corresponding to the electrical hysteresis range 2dB-4.5dB, shown in the AC characteristics table, will be 1dB-3dB Optical Hysteresis.
- See "Typical Operating Characteristics" for a graph showing how to choose a particular  $R_{LOSLVL}$  for a particular LOS assert and its associated de-assert amplitude.

### Typical Characteristics



## Functional Block Diagram



### Detailed Description

The SY88347DL low-power, high-sensitivity limiting post amplifier operates from a single +3.3V power supply, over temperatures from  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ . Signals with data rates up to 3.2Gbps and as small as  $5\text{mV}_{\text{PP}}$  can be amplified. Figure 1 shows the allowed input voltage swing. The SY88347DL generates a LOS output allowing feedback to /EN for output stability.  $\text{LOS}_{\text{LVL}}$  sets the sensitivity of the input amplitude detection.

#### Input Amplifier/Buffer

Figure 2 shows a simplified schematic of the SY88347DL's input stage. The high-sensitivity of the input amplifier allows signals as small as  $5\text{mV}_{\text{PP}}$  to be detected and amplified. The input amplifier also allows input signals as large as  $1800\text{mV}_{\text{PP}}$ . Input signals are linearly amplified with a typical 42dB differential voltage gain. Since it is a limiting amplifier, the SY88347DL outputs typically  $1500\text{mV}_{\text{PP}}$  voltage-limited waveforms for input signals that are greater than  $12\text{mV}_{\text{PP}}$ . Applications requiring the SY88347DL to operate with high-gain should have the upstream TIA placed as close as possible to the SY88347DL's input pins. This ensures the best performance of the device.

#### Output Buffer

The SY88347DL's PECL output buffer is designed to drive  $50\Omega$  lines. The output buffer requires appropriate termination for proper operation. An external  $50\Omega$  resistor to  $V_{\text{CC}}-2\text{V}$  for each output pin provides this. Figure 3 shows a simplified schematic of the output stage.

### Loss-of-Signal

The SY88347DL generates a chatter-free LOS open-collector TTL output, as shown in Figure 4. LOS is used to determine that the input amplitude is large enough to be considered a valid input. LOS asserts high if the input amplitude falls below the threshold sets by  $\text{LOS}_{\text{LVL}}$  and de-asserts low otherwise. LOS can be fed back to the enable bar (/EN) input to maintain output stability under a loss-of-signal condition. /EN de-asserts the true output signal without removing the input signals. Typically, 3.3dB LOS hysteresis is provided to prevent chattering.

#### Loss-of-Signal Level Set

A programmable LOS level set pin ( $\text{LOS}_{\text{LVL}}$ ) sets the threshold of the input amplitude detection. Connecting an external resistor between  $V_{\text{CC}}$  and  $\text{LOS}_{\text{LVL}}$  sets the voltage at  $\text{LOS}_{\text{LVL}}$ . This voltage ranges from  $V_{\text{CC}}$  to  $V_{\text{REF}}$ . The external resistor creates a voltage divider between  $V_{\text{CC}}$  and  $V_{\text{REF}}$ , as shown in Figure 5.

#### Hysteresis

The SY88347DL typically provides 3.3dB LOS electrical hysteresis. By definition, a power ratio, measured in dB, is  $10\log(\text{power ratio})$ . Power is calculated as  $V_{\text{IN}}^2/R$  for an electrical signal. Hence, the same ratio can be stated as  $20\log(\text{voltage ratio})$ . While in linear mode, the electrical voltage input changes linearly with the optical power and therefore, the ratios will change linearly. Thus, the optical hysteresis in dB is half the electrical hysteresis in dB given in the data sheet. Since the SY88347DL is an electrical device, this data sheet refers to hysteresis in electrical terms. With 3.3dB LOS hysteresis, a voltage factor of 1.46 is required to assert or de-assert LOS.



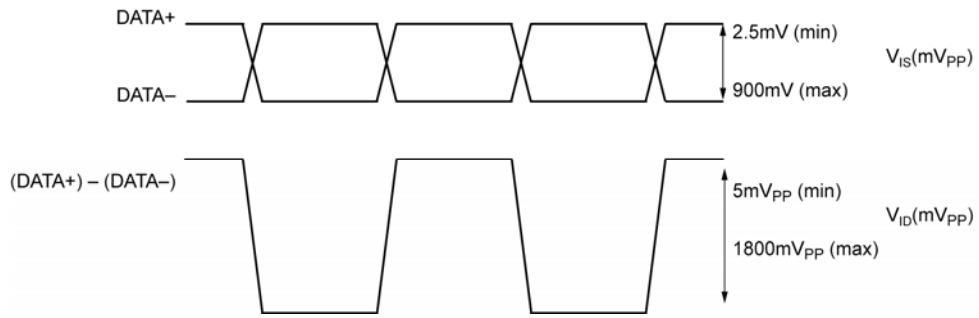


Figure 1.  $V_{IS}$  and  $V_{ID}$

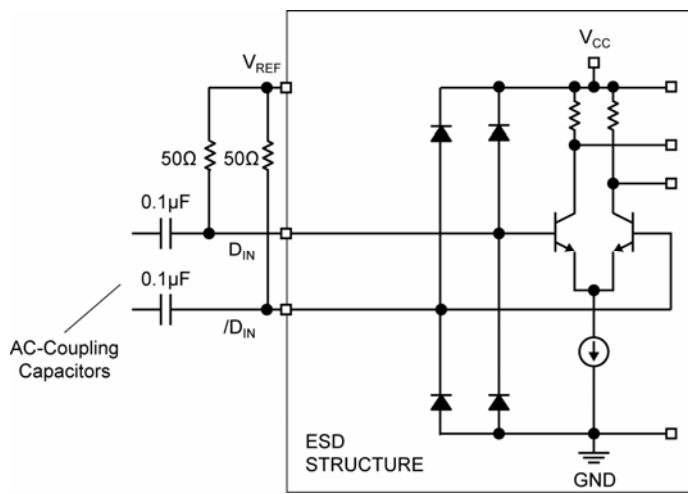


Figure 2. Input Structure

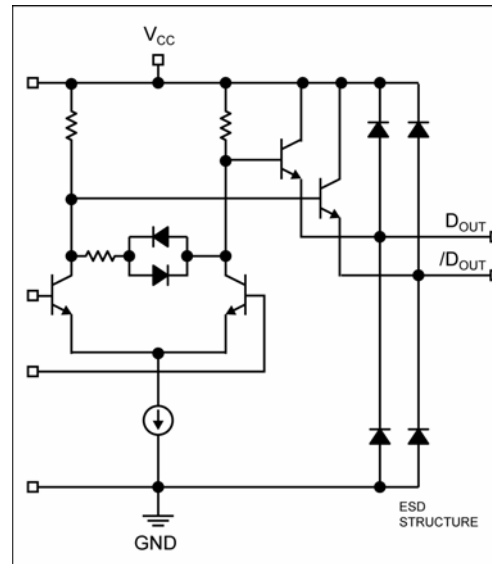


Figure 3. Output Structure

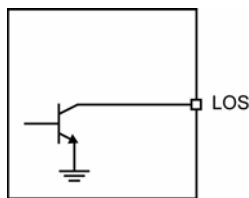


Figure 4. LOS Output Structure

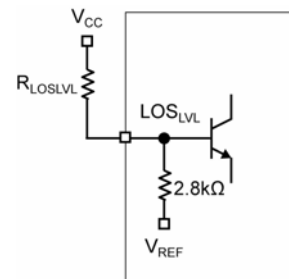
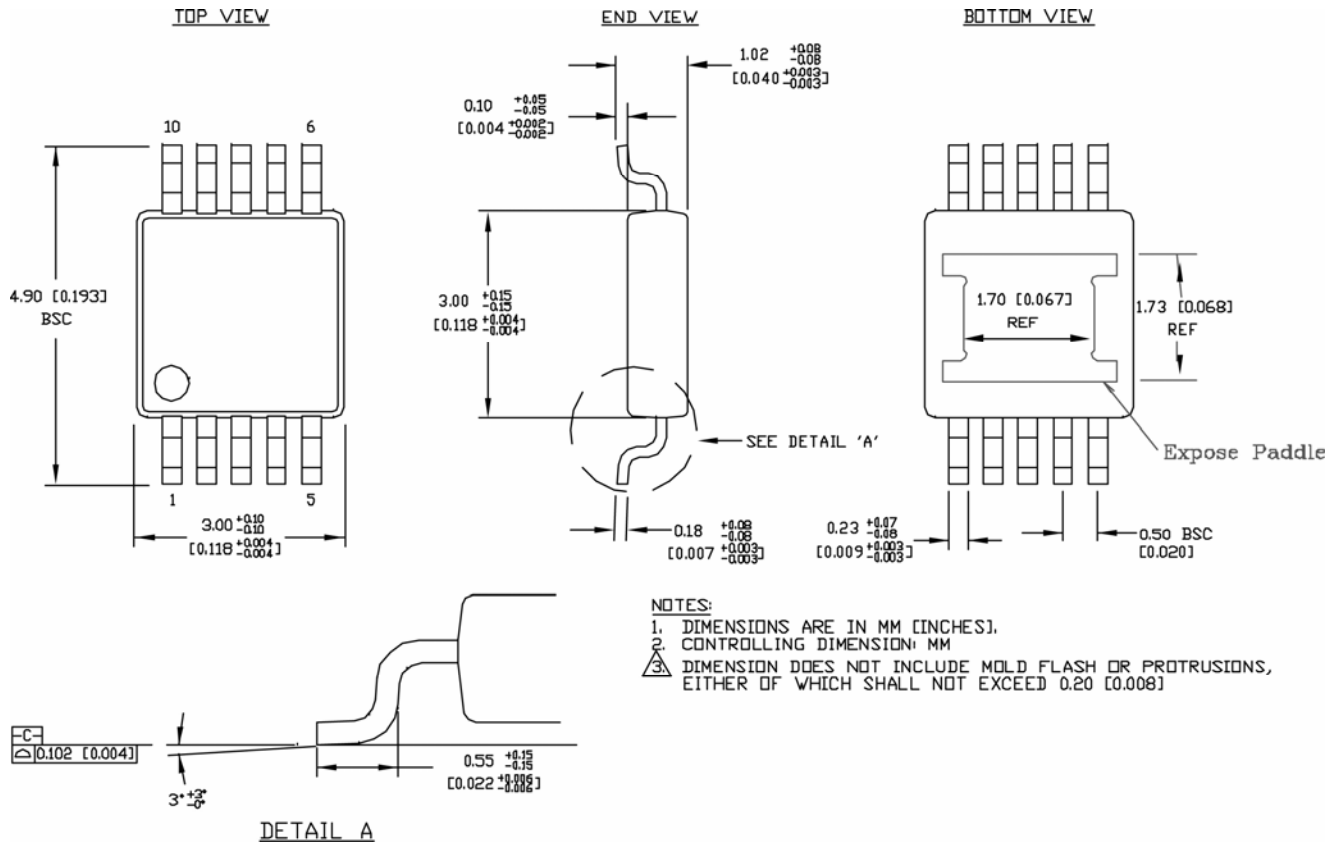


Figure 5. LOSLVL Setting Circuit

**Package Information**



**10-Pin EPAD-MSOP (K10-2)**

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