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# MICREL®

# 3.3V/5V 622Mbps PECL LOW-POWER LIMITING POST AMPLIFIER W/PECL SIGNAL DETECT

## SY88713V

## FEATURES

- **Single 3.3V or 5V power supply**
- **Up to 622Mbps operation**
- **Low noise PECL data outputs**
- **Chatter-free PECL Signal Detect (SD) output**
- **TTL /EN input**
- **Programmable SD level set (SD$_{LVL}$)**
- **Available in a tiny 10-pin MSOP (3mm) package**

## APPLICATIONS

- **622Mbps SONET/SDH**
- **Small form factor transceivers**
- **High-gain line driver and line receiver**

## DESCRIPTION

The SY88713V low-power limiting post amplifier is designed for use in fiber optic receivers. The device connects to typical transimpedance amplifiers (TIAs). The linear signal output from TIAs can contain significant amounts of noise and may vary in amplitude over time. The SY88713V quantizes these signals and outputs PECL level waveforms.
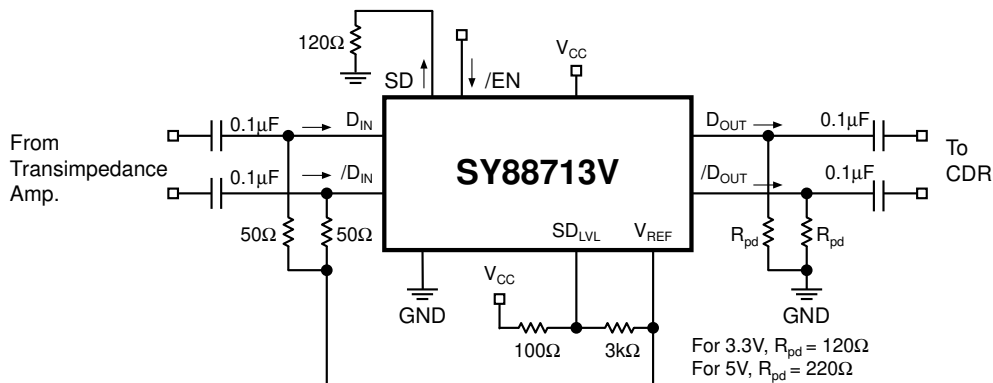
The SY88713V operates from a single +3.3V or +5V power supply, over temperatures ranging from −40°C to +85°C. With its wide bandwidth and high gain, signals with data rates up to 622Mbps and as small as 5mVp-p can be amplified to drive devices with PECL inputs.

The SY88713V generates a PECL SD output. A programmable signal-detect level set pin (SD$_{LVL}$) sets the sensitivity of the input amplitude detection. SD asserts high if the input amplitude rises above the threshold set by SD$_{LVL}$ and deasserts low otherwise. /EN deasserts the true output signal without removing the input signal. Typically 4.6dB SD hysteresis is provided to prevent chattering.
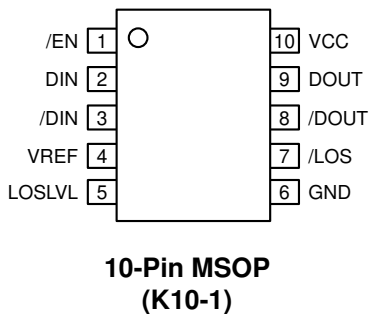
## TYPICAL APPLICATIONS CIRCUIT

# PACKAGE/ORDERING INFORMATION

```
      /EN  1  ○        10  VCC
      DIN  2            9  DOUT
     /DIN  3            8  /DOUT
     VREF  4            7  /LOS
   LOSLVL  5            6  GND
```

**10-Pin MSOP
(K10-1)**

## Ordering Information

| Part Number | Package Type | Operating Range | Package Marking | Lead Finish |
|---|---|---|---|---|
| SY88713VKC | K10-1 | Commercial | 713V | Sn-Pb |
| SY88713VKCTR[1] | K10-1 | Commercial | 713V | Sn-Pb |
| SY88713VKG | K10-1 | Industrial | 713V with Pb-Free bar-line indicator | Pb-Free NiPdAu |
| SY88713VKGTR[1] | K10-1 | Industrial | 713V with Pb-Free bar-line indicator | Pb-Free NiPdAu |

**Note:**

1. Tape and Reel.

# PIN DESCRIPTION

| Pin Number | Pin Name | Type | Pin Function |
|---|---|---|---|
| 1 | /EN | TTL Input: Default is high. | Enable: Deasserts true data output when high. |
| 2 | DIN | Data Input | True data input. |
| 3 | /DIN | Data Input | Complementary data input. |
| 4 | VREF | | Reference voltage. |
| 5 | SDLVL | Input | Signal-Detect Level Set: A voltage between $V_{CC}$ and $V_{REF}$ on this pin sets the threshold for the data input amplitude at which SD will be asserted. |
| 6 | GND | Ground | Device ground. |
| 7 | SD | PECL Output | Signal-Detect: Asserts high when the data input amplitude rises above the threshold set by $SD_{LVL}$. |
| 8 | /DOUT | PECL Output | Complementary data output. |
| 9 | DOUT | PECL Output | True data output. |
| 10 | VCC | Power Supply | Positive power supply. |

# Absolute Maximum Ratings(Note 1)

Supply Voltage ($V_{CC}$) ...................................... 0V to +7.0V

Input Voltage ($D_{IN}$, /$D_{IN}$) ........................................ 0 to $V_{CC}$

Output Current ($I_{OUT}$)

    Continuous ........................................... 50mA

    Surge ................................................. 100mA

/EN Voltage ......................................................... 0 to $V_{CC}$

$V_{REF}$ Current ...................................... –800µA to +500µA

$SD_{LVL}$ Voltage ........................................................ 0 to $V_{CC}$

Lead Temperature (soldering, 20 sec.) .................. +260°C

Storage Temperature ($T_S$) ...................... –55°C to +125°C

# Operating Ratings(Note 2)

Supply Voltage ($V_{CC}$) ............................ +3.0V to +3.6V or

............................................................ +4.5V to +5.5V

Ambient Temperature ($T_A$), **Note 3 ............** –40°C to +85°C

Junction Temperature ($T_J$), **Note 3 ..........** –40°C to +120°C

Package Thermal Resistance

  MSOP

    ($\theta_{JA}$) Still-Air ................................................ 113°C/W

    ($\psi_{JB}$) Still-Air .................................................... 74°C/W

**Note 1.** Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to ABSOLUTE MAXIMUM RATING conditions for extended periods may affect device reliability.

**Note 2.** The data sheet limits are not guaranteed if the device is operated beyond the operating ratings.

**Note 3.** Commercial devices are guaranteed from 0°C to +85°C ambient temperature.

## DC ELECTRICAL CHARACTERISTICS(Note 1)

$V_{CC}$ = 3.0V to 3.6V or 4.5V to 5.5V; $R_{LOAD}$ = 50Ω to $V_{CC}$–2V; $T_A$ = –40°C to +85°C; typical values at $V_{CC}$ = 3.3V, $T_A$ = 25°C

| Symbol | Parameter | Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $I_{CC}$ | Power Supply Current | no output load | | 21 | 40 | mA |
| $SD_{LVL}$ | $SD_{LVL}$ Voltage | | $V_{REF}$ | | $V_{CC}$ | V |
| $V_{IH}$ | /EN Input HIGH Voltage | | 2.0 | | | V |
| $V_{IL}$ | /EN Input LOW Voltage | | | | 0.8 | V |
| $I_{IH}$ | /EN Input HIGH Current | $V_{IN}$ = 2.7V <br> $V_{IN}$ = $V_{CC}$ | | | 20 <br> 100 | µA <br> µA |
| $I_{IL}$ | /EN Input LOW Current | $V_{IN}$ = 0.5V | –0.3 | | | mA |
| $V_{OH}$ | PECL Output HIGH Voltage | 50Ω to $V_{CC}$–2V output load | $V_{CC}$–1.085 | $V_{CC}$–0.955 | $V_{CC}$–0.880 | V |
| $V_{OL}$ | PECL Output LOW Voltage | 50Ω to $V_{CC}$–2V output load | $V_{CC}$–1.830 | $V_{CC}$–1.705 | $V_{CC}$–1.555 | V |
| $V_{OFFSET}$ | Differential Output Offset | | | | ±100 | mV |
| $V_{IHCMR}$ | Common Mode Range | **Note 2** | GND +1.7 | | $V_{CC}$ | V |
| $V_{REF}$ | Reference Voltage | **Note 3** | $V_{CC}$–1.38 | $V_{CC}$–1.32 | $V_{CC}$–1.26 | V |

**Note 1.** Specification for packaged product only.

**Note 2.** The $V_{IHCMR}$ range is referenced to the most positive side of the differential input signal.

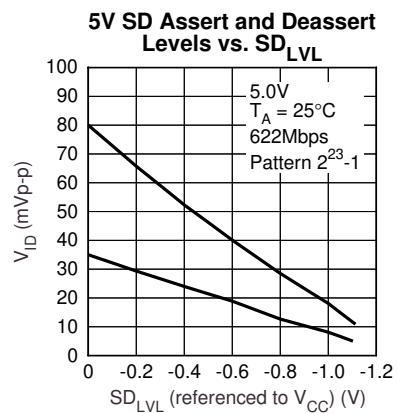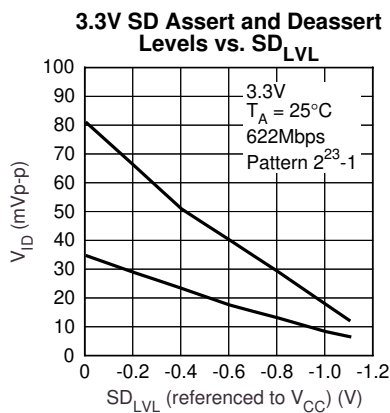**Note 3.** The current provided into or from $V_{REF}$ must be limited to 800µA source and 500µA sink.

## AC ELECTRICAL CHARACTERISTICS(Note 1)

$V_{CC}$ = 3.0V to 3.6V or 4.5V to 5.5V; $R_{LOAD}$ = 50$\Omega$ to $V_{CC}$–2V; $T_A$ = –40°C to +85°C; typical values at $V_{CC}$ = 3.3V, $T_A$ = 25°C

| Symbol | Parameter | Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| HYS | SD Hysteresis | electrical signal | 2 | 4.6 | 8 | dB |
| $t_{OFF}$ | SD Release Time | | | 0.1 | 0.5 | μs |
| $t_{ON}$ | SD Assert Time | | | 0.2 | 0.5 | μs |
| $t_r, t_f$ | Differential Output Rise/Fall Time (20% to 80%) | | | | 400 | ps |
| $V_{ID}$ | Differential Input Voltage Swing | | 5 | | 1800 | mVp-p |
| $V_{OD}$ | Differential Output Voltage Swing | $V_{ID} \geq$ 18mVp-p<br>$V_{ID}$ = 5mVp-p | | 1500<br>400 | | mVp-p<br>mVp-p |
| $V_{SR}$ | SD Sensitivity Range | | 5 | | 50 | mVp-p |
| $A_{V(Diff)}$ | Differential Voltage Gain | | | 38 | | dB |
| $B_{-3dB}$ | 3dB Bandwidth | | 700 | | | MHz |
| $S_{21}$ | Single-Ended Small-Signal Gain | | 26 | 32 | | dB |

**Note 1.** Specification for packaged product only.

## TYPICAL OPERATING CHARACTERISTICS



**3.3V SD Assert and Deassert Levels vs. $SD_{LVL}$**

3.3V
$T_A$ = 25°C
622Mbps
Pattern $2^{23}$-1

$V_{ID}$ (mVp-p)

$SD_{LVL}$ (referenced to $V_{CC}$) (V)



**5V SD Assert and Deassert Levels vs. $SD_{LVL}$**

5.0V
$T_A$ = 25°C
622Mbps
Pattern $2^{23}$-1

$V_{ID}$ (mVp-p)

$SD_{LVL}$ (referenced to $V_{CC}$) (V)

## DETAILED DESCRIPTION

The SY88713V low-power limiting post amplifier operates from a single +3.3V or +5V power supply, over temperatures from –40°C to +85°C. Signals with data rates up to 622Mbps and as small as 5mVp-p can be amplified. Figure 1 shows the allowed input voltage swing. The SY88713V generates an SD output. $SD_{LVL}$ sets the sensitivity of the input amplitude detection.

### Input Amplifier/Buffer

Figure 2 shows a simplified schematic of the SY88713V's input stage. The high sensitivity of the input amplifier allows signals as small as 5mVp-p to be detected and amplified. The input amplifier allows input signals as large as 1800mVp-p. Input signals are linearly amplified with a typically 38dB differential voltage gain. Since it is a limiting amplifier, the SY88713V outputs typically 1500mVp-p voltage-limited waveforms for input signals that are greater than 18mVp-p. Applications requiring the SY88713V to operate with high-gain should have the upstream TIA placed as close as possible to the SY88713V's input pins to ensure the best performance of the device.

### Output Buffer

The SY88713V's PECL output buffer is designed to drive 50Ω lines. The output buffer requires appropriate termination for proper operation. An external 50Ω resistor to $V_{CC}$–2V for each output pin provides this. Figure 3 shows a simplified schematic of the output stage and includes an appropriate termination method.

### Signal-Detect

The SY88813V generates a chatter-free PECL signal-detect (SD) similar to the SY88713V's output buffer. SD is used to determine that the input amplitude is large enough to be considered a valid input. SD asserts high if the input amplitude rises above the threshold set by $SD_{LVL}$ and deasserts low otherwise. /EN deasserts the true output signal without removing the input signals. Typically 4.6dB SD hysteresis is provided to prevent chattering.

### Signal-Detect Level Set

A programmable signal-detect level set pin ($SD_{LVL}$) sets the threshold of the input amplitude detection. Setting a voltage on $SD_{LVL}$ between $V_{CC}$ and $V_{REF}$ sets this threshold. If desired, a resistor divider between $V_{CC}$ and $V_{REF}$, as shown in Figure 4, also creates this threshold. The smaller the voltage difference from $SD_{LVL}$ to $V_{CC}$, the smaller the SD sensitivity. Hence, larger input amplitude is required to assert SD. *"Typical Operating Characteristics"* shows the relationship between the input amplitude detection sensitivity and the $SD_{LVL}$ voltage.

### Hysteresis

The SY88713V provides typically 4.6dB SD electrical hysteresis. By definition, a power ratio measured in dB is 10log(power ratio). Power is calculated as $V^2_{IN}/R$ for an electrical signal. Hence the same ratio can be stated as 20log(voltage ratio). While in linear mode, the electrical voltage input changes linearly with the optical power and hence the ratios change linearly. Therefore, the optical hysteresis in dB is half the electrical hysteresis in dB given in the datasheet. The SY88713V provides typically 2.3dB SD optical hysteresis. As the SY88713V is an electrical device, this datasheet refers to hysteresis in electrical terms. With 6dB SD hysteresis, a voltage factor of two is required to assert or deassert SD.
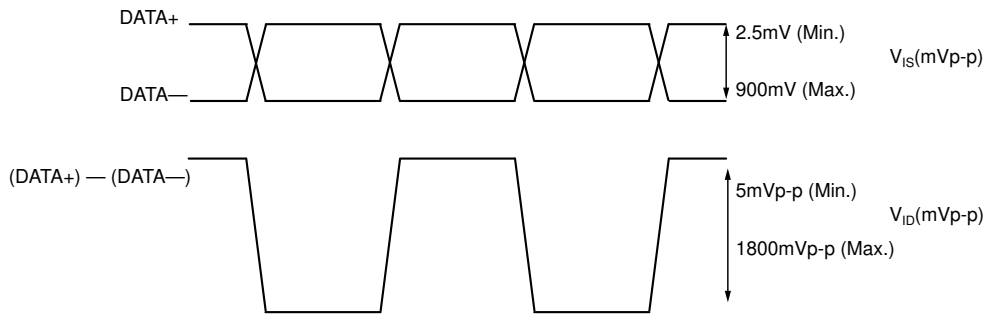
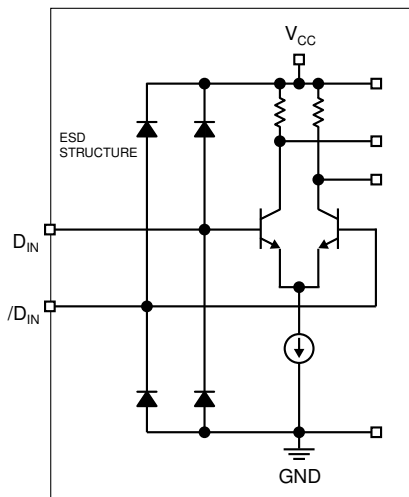**Figure 1.  V$_{IS}$ and V$_{ID}$ Definitions**

DATA+

DATA—

2.5mV (Min.)

900mV (Max.)

V$_{IS}$(mVp-p)

(DATA+) — (DATA—)

5mVp-p (Min.)

1800mVp-p (Max.)

V$_{ID}$(mVp-p)



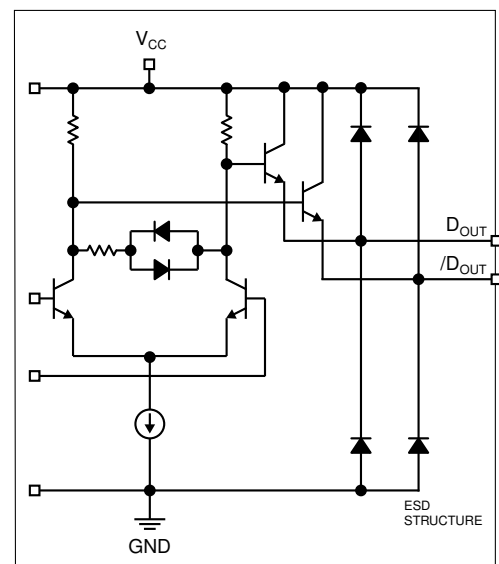**Figure 2.  Input Structure**



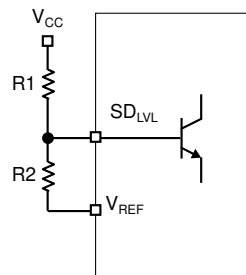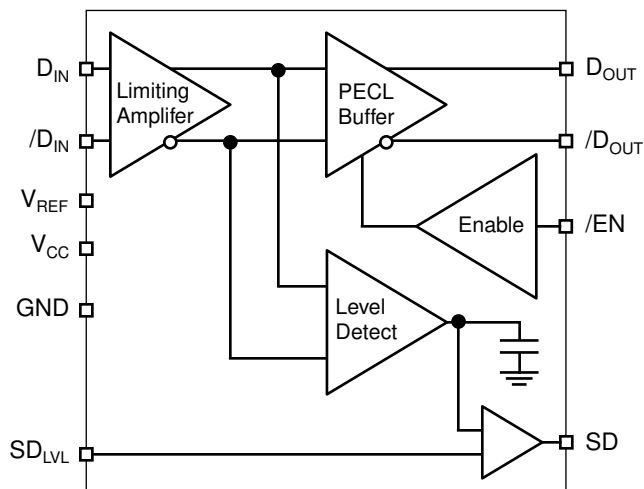**Figure 3.  Output Structure**



**Figure 4.  SD$_{LVL}$ Setting Circuit**

**Notes.**  $SD_{LVL} = V_{CC} - 1.32V + \dfrac{R2}{R1+R2} \times 1.32V$

$R1 + R2 \geq 5k\Omega$

## FUNCTIONAL BLOCK DIAGRAM
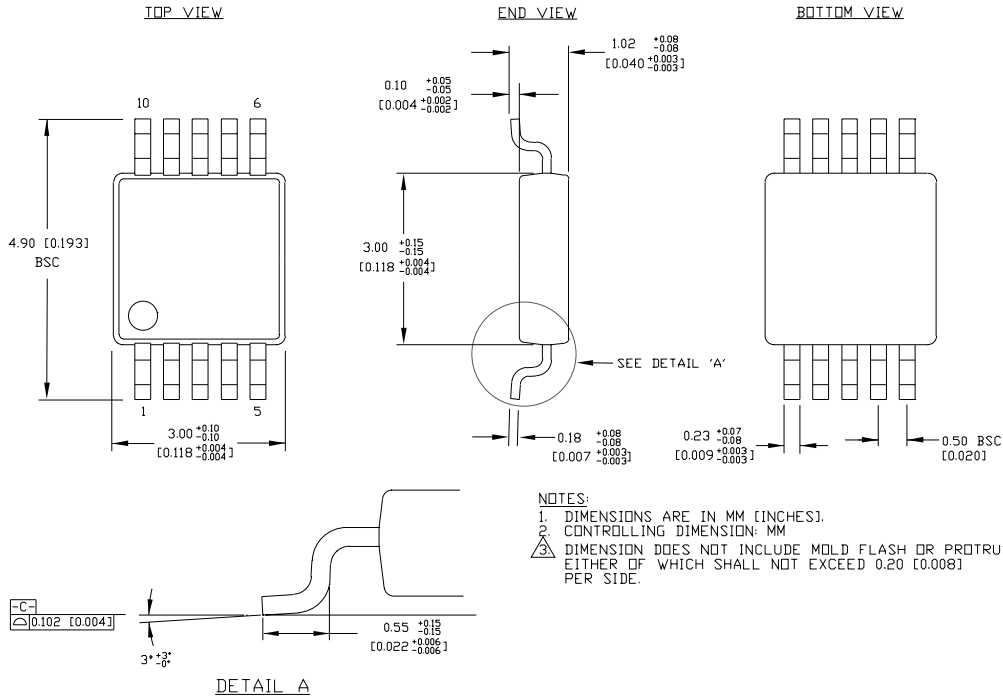


## DESIGN PROCEDURE

**Layout and PCB Design**

Since the SY88713V is a high-frequency component, performance can be largely determined by the board layout and design. A common problem with high-gain amplifiers is the feedback from the large swing outputs to the input via the power supply.

The SY88713V's ground pin should be connected to the circuit board ground. Use multiple PCB vias close to the part to connect to ground. Avoid long, inductive runs which can degrade performance.

## 10 LEAD MSOP (K10-1)

TOP VIEW          END VIEW          BOTTOM VIEW

10          6

4.90 [0.193]
BSC

1          5

3.00 $^{+0.10}_{-0.10}$
[0.118 $^{+0.004}_{-0.004}$]

1.02 $^{+0.08}_{-0.08}$
[0.040 $^{+0.003}_{-0.003}$]

0.10 $^{+0.05}_{-0.05}$
[0.004 $^{+0.002}_{-0.002}$]

3.00 $^{+0.15}_{-0.15}$
[0.118 $^{+0.004}_{-0.004}$]

SEE DETAIL 'A'

0.18 $^{+0.08}_{-0.08}$
[0.007 $^{+0.003}_{-0.003}$]

0.23 $^{+0.07}_{-0.08}$
[0.009 $^{+0.003}_{-0.003}$]

0.50 BSC
[0.020]

NOTES:
1. DIMENSIONS ARE IN MM [INCHES].
2. CONTROLLING DIMENSION: MM
3. DIMENSION DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS, EITHER OF WHICH SHALL NOT EXCEED 0.20 [0.008] PER SIDE.

-C-
0.102 [0.004]

3° $^{+3°}_{-0°}$

0.55 $^{+0.15}_{-0.15}$
[0.022 $^{+0.006}_{-0.006}$]

DETAIL A

Rev. 00

The information furnished by Micrel in this datasheet is believed to be accurate and reliable. However, no responsibility is assumed by Micrel for its use. Micrel reserves the right to change circuitry and specifications at any time without notification to the customer.