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SY88973BL

3.3V 3.2Gbps CML Low Power Limiting Post Amplifier with TTL LOS

General Description

The SY88973BL low-power, limiting post amplifier is designed for use in fiber optic receivers. The device connects to typical transimpedance amplifiers (TIAs). The linear signal output from TIAs can contain significant amounts of noise and may vary in amplitude over time. The SY88973BL quantizes these signals and outputs typically $800mV_{PP}$ voltage-limited waveforms.

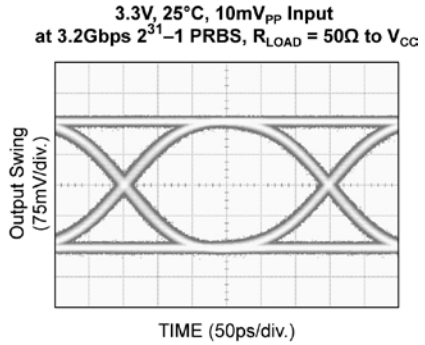
The SY88973BL operates from a single +3.3V ±10% power supply, over an industrial temperature range of –40°C to +85°C. With its wide bandwidth and high gain, signals with data rates up to 3.2Gbps and as small as $10mV_{PP}$ can be amplified to drive devices with CML inputs or AC-coupled PECL inputs.

The SY88973BL incorporates a loss-of-signal (LOS), open-collector TTL output with external 4.75kΩ to 10kΩ pull-up resistor to fully comply with SFP MSA. A programmable, loss-of-signal level-set pin (LOSLVL) sets the sensitivity of the input amplitude detection. LOS asserts high if the input amplitude falls below the threshold sets by LOSLVL and de-asserts low otherwise. LOS can be fed back to the enable (/EN) input to maintain output stability under a loss-of-signal condition. /EN de-asserts the true output signal without removing the input signal. Typically, 4.6dB LOS hysteresis is provided to prevent chattering.

Please see Micrel's website at www.micrel.com for a complete selection of optical module ICs.

All support documentation can be found on Micrel's web site at: www.micrel.com.

Typical Performance



Features

- Multi-rate up to 3.2Gbps operation
- Wide gain-bandwidth product
- 38dB differential gain
- 2GHz 3dB bandwidth
- Low noise 50Ω CML data outputs
  - $800mV_{PP}$ output swing
  - 60ps edge rates
  - $5ps_{RMS}$ typ. random jitter
  - $15ps_{PP}$ typ. deterministic jitter
- Chatter-free, Loss-of-Signal (LOS) output
  - No internal pull-up resistor− fully compliant with SFP MSA
  - 4.6dB electrical hysteresis
  - OC-TTL output
- Programmable LOS sensitivity using single external resistor
- Internal 50Ω data input termination
- TTL /EN input allows feedback from LOS
- Wide operating range:
  - Single 3.3V ±10%
  - –40°C to +85°C industrial temperature range
- Available in a tiny 3mm x 3mm 16-pin QFN package

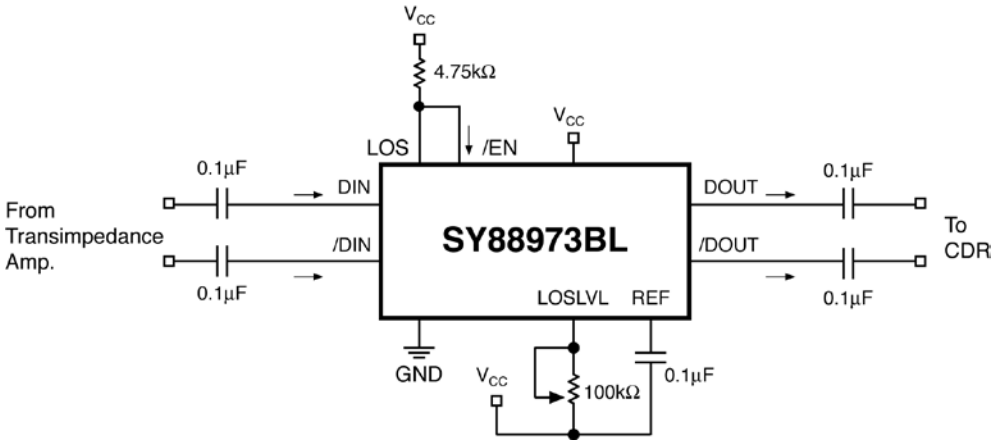
Applications

- 1.25Gbps and 2.5Gbps Gigabit Ethernet
- 1.062Mbps and 2.125Gbps Fibre Channel
- 155Mbps, 622Gbps, 1.25Gbps, and 2.5Gbps SONET/SDH
- Gigabit interface converter (GBIC)
- Small form factor (SFF) and small form factor pluggable (SFP) transceivers
- Parallel 10G Ethernet
- High-gain line driver and line receiver

Markets

- Telecom/datacom
- Optical transceiver

Typical Application Circuit



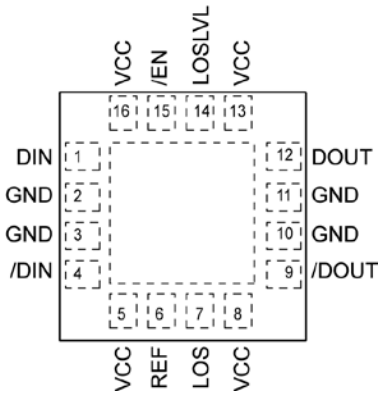
Ordering Information[1]

Part Number	Package Type	Operating Range	Package Marking	Lead Finish
SY88973BLMG[3]	QFN-16	Industrial	973B with Pb-Free bar-line indicator	Pb-Free Matte-Sn
SY88973BLMGTR[2, 3]	QFN-16	Industrial	973B with Pb-Free bar-line indicator	Pb-Free Matte-Sn

Notes:

1. Contact factory for die availability. Dice are guaranteed at TA = 25°C, DC Electricals only.
2. Tape and Reel.
3. Pb-Free package is recommended for new designs.

Pin Configuration

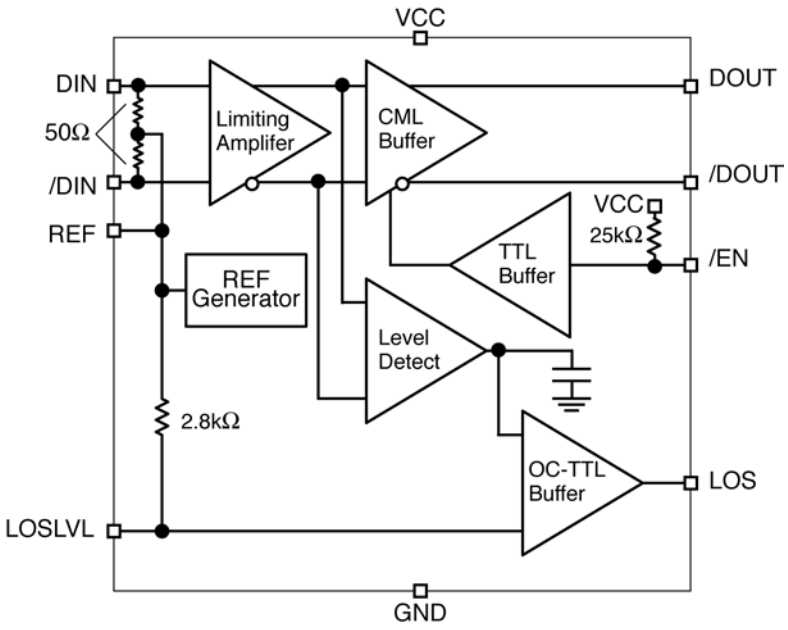


16-pin QFN

Pin Description

Pin Number (QFN)	Pin Name	Type	Pin Function
15	/EN	TTL Input: Default is high.	Enable: De-asserts true data output when high. Incorporates 25kΩ pull-up to VCC.
1, 4	DIN, /DIN	Differential Data Input	Differential data input. Each pin internally terminates to REF through 50Ω.
6	REF		Reference Voltage: Bypass with 0.01µF low ESR capacitor from REF to VCC to stabilize LOSLVL and REF.
14	LOSLVL	Input: Default is maximum sensitivity	Loss-of-Signal Level Set: A resistor from this pin to VCC sets the threshold for the data input amplitude at which the LOS output will be asserted.
2, 3, 10, 11 Exposed Pad	GND	Ground	Device ground. Exposed pad must be soldered (or equivalent) to the same potential as the ground pins.
7	LOS	Open Collector TTL Output	Loss-of-Signal: asserts high when the data input amplitude falls below the threshold set by LOSLVL. For proper operation, connect an external 4.75kΩ to 10kΩ pull-up resistor between this pin and Vcc.
9, 12	DOUT, /DOUT	Differential CML Output	Differential data output.
5, 8, 13, 16	VCC	Power Supply	Positive power supply. Bypass with 0.1µF|| 0.01µF low ESR capacitors. 0.01µF capacitors should be as close as possible to VCC pins.

Functional Block Diagram



Absolute Maximum Ratings[1]

Supply Voltage (V_{CC}) ..... 0V to 4.0V
/EN, LOSLVL Voltage ..... 0V to V_{CC}
REF Current ..... ±1mA
LOS Current ..... ±5mA
DOUT, /DOUT Current ..... ±25mA
DIN, /DIN Current ..... ±10mA
Lead Temperature (soldering, 20sec.) ..... 260°C
Storage Temperature (T_s) ..... –65°C to +150°C

Operating Ratings[2]

Supply Voltage (V_{CC}) ..... +3.0V to +3.6V
Ambient Temperature (T_A) ..... –40°C to +85°C
Junction Temperature (T_J) ..... –40°C to +120°C
Package Thermal Resistance
QFN
θ_{JA} (Still-Air) ..... 61°C/W
ψ_{JB} ..... 38°C/W

DC Electrical Characteristics

V_{CC} = 3.0V to 3.6V; T_A = –40°C to +85°C, typical values at V_{CC} = 3.3V, T_A = 25°C.

Symbol	Parameter	Condition	Min	Typ	Max	Units
I_{CC}	Power Supply Current	Note 4 Note 5		28 45	42 62	mA mA
V_{REF}	REF Voltage			V_{CC}–1.3		V
V_{LOSLVL}	LOSLVL Voltage Range		V_{REF}		V_{CC}	V
V_{OH}	Output HIGH Voltage	Note 6	V_{CC}–0.020	V_{CC}–0.005	V_{CC}	V
V_{OL}	Output LOW Voltage	Note 6	V_{CC}–0.475	V_{CC}–0.400	V_{CC}–0.350	V
V_{OFFSET}	Differential Output Offset	Note 6			±80	mV
Z_O	Single-Ended Output Impedance		40	50	60	Ω
Z_I	Single-Ended Input Impedance		40	50	60	Ω

TTL DC Electrical Characteristics

V_{CC} = 3.0V to 3.6V; T_A = –40°C to +85°C.

Symbol	Parameter	Condition	Min	Typ	Max	Units
I_{OH}	LOS Output Leakage	V_{OH} = 3.6V			100	uA
V_{OL}	LOS Output LOW Level	Sinking 2mA			0.5	V
V_{IH}	/EN Input HIGH Voltage		2.0			V
V_{IL}	/EN Input LOW Voltage				0.8	V
I_{IH}	/EN Input HIGH Current	V_{IN} = 2.7V V_{IN} = V_{CC}			20 100	µA µA
I_{IL}	/EN Input LOW Current	V_{IN} = 0.5V	–300			uA

Notes:

1. Permanent device damage may occur if Absolute Maximum Ratings are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.
2. The data sheet limits are not guaranteed if the device is operated beyond the operating ratings.
3. Thermal performance assumes the use of 4-layer PCB. Exposed pad must be soldered (or equivalent) to the device's most negative potential on the PCB.
4. Excludes current of CML output stage. See “Detailed Description.”
5. Total device current with no output load.
6. Output levels are based on a 50Ω to V_{CC} load impedance. If the load impedance is different, the output level will be changed. Amplifier is in limiting mode.

AC Electrical Characteristics[4]

V_{CC} = 3.0V to 3.6V; T_A = –40°C to +85°C, R_{LOAD} = 50Ω to V_{CC}; typical values at V_{CC} = 3.3V, T_A = 25°C.

Symbol	Parameter	Condition	Min	Typ	Max	Units
PSRR	Power Supply Rejection Ratio			35		dB
t_r, t_f	Output Rise/Fall Times (20% to 80%)	Note 7		60	120	ps
t_{JITTER}	Deterministic Random	Note 8		15 5		ps_{PP} ps_{RMS}
V_{ID}	Differential Input Voltage Swing		10		1800	mV_{PP}
V_{OD}	Differential Output Voltage Swing	Note 7	700	800	950	mV_{PP}
HYS	LOS Hysteresis	Note 9	2	4.6	8	dB
t_{OFF}	LOS Release Time			0.1	0.5	µs
t_{ON}	LOS Assert Time			0.2	0.5	µs
V_{SR}	LOS Sensitivity Range	Note 10	10		35	mV_{PP}
B_{-3dB}	–3dB Bandwidth			2.0		GHz
$A_{V(Diff)}$	Differential Voltage Gain		32	38		dB
S_{21}	Single-Ended Small-Signal Gain		26	32		dB

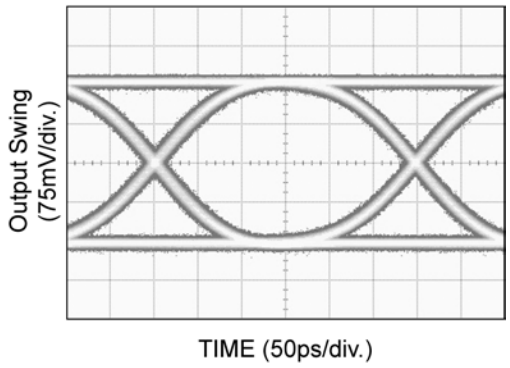
Notes:

7. Amplifier in limiting mode. Input is a 200MHz square wave, t_r < 300ps.
8. Deterministic jitter measured using 2.488Gbps K28.5 pattern, V_{ID} = $10mV_{PP}$. Random jitter measured using 2.488Gbps K28.7 pattern, V_{ID} = $10mV_{PP}$.
9. Electrical signal.
10. This is the detectable range of input amplitudes that can assert LOS. The input amplitude to de-assert LOS is 2–8dB higher than the assert amplitude. See “Typical Operating Characteristics” for graphs showing how to choose a particular V_{LOSLVL} or R_{LOSLVL} for a particular LOS assert, and its associated de-assert amplitude. If increased LOS sensitivity and hysteresis are required, an application note entitled: “Notes on Sensitivity and Hysteresis in Micrel Post Amplifiers” is available at http://www.micrel.com/_PDF/HBW/App-Notes/an-45.pdf.

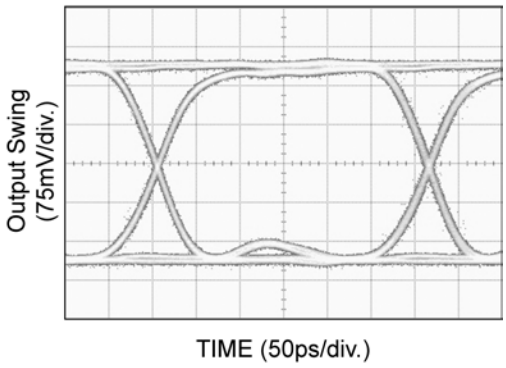
Typical Operating Characteristics

V_{CC} = 3.3V, T_A = 25ºC, R_{LOAD} = 50Ω to V_{CC}, unless otherwise noted.

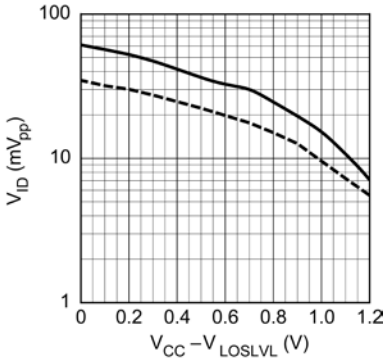
10mV$_{pp}$ Input at 3.2Gbps 2^{31}-1 PRBS



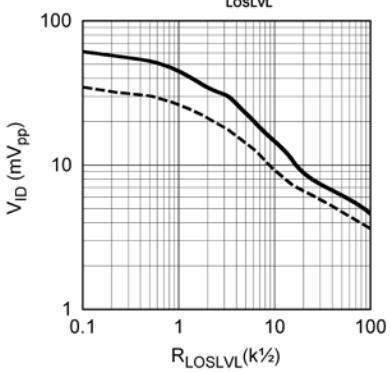
1.8V$_{pp}$ Input at 3.2Gbps 2^{31}-1 PRBS



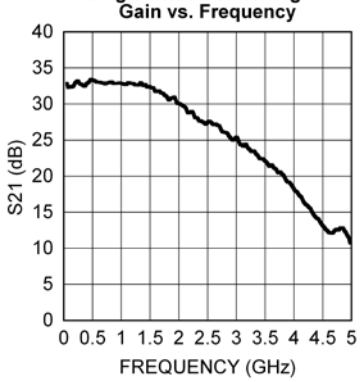
V_{ID} to Assert/De-assert LOS vs. V_{LOSLVL}



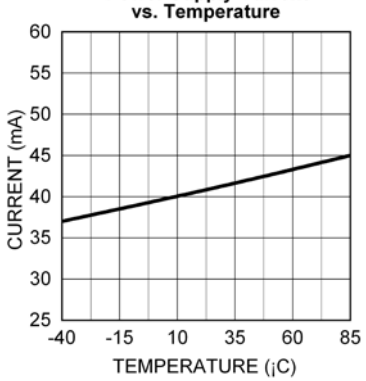
V_{ID} to Assert/De-assert LOS vs. R_{LOSLVL}



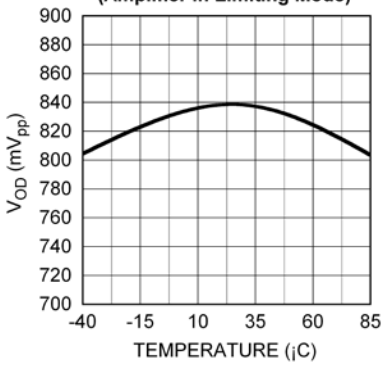
Single-Ended Small-Signal Gain vs. Frequency



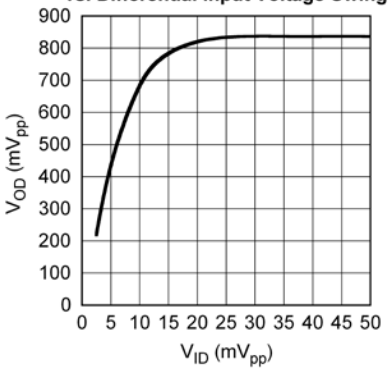
Power Supply Current vs. Temperature



Differential Output Voltage Swing vs. Temperature (Amplifier in Limiting Mode)



Differential Output Voltage Swing vs. Differential Input Voltage Swing



Description

The SY88973BL low-power, limiting post amplifier operates from a single +3.3V ±10% power supply, over an industrial temperature range of –40°C to +85°C. Signals with data rates up to 3.2Gbps and as small as $10mV_{PP}$ can be amplified. Figure 1 shows the allowed input voltage swing. The SY88973BL generates a LOS output, providing feedback to /EN for output stability. LOSLVL sets the sensitivity of the input amplitude detection.

Input Amplifier/Buffer

The SY88973BL's inputs are internally terminated with 50Ω-to-REF. Unless unaffected by this internal termination scheme, upstream devices need to be AC-coupled to the SY88973BL's inputs. Figure 2 shows a simplified schematic of the input structure.

The high sensitivity of the input amplifier detects and amplifies signals as small as $10mV_{PP}$. The input amplifier allows input signals as large as $1800mV_{PP}$. Input signals are linearly amplified with a typical 38dB differential voltage gain. Since it is a limiting amplifier, the SY88973BL outputs, typically $800mV_{PP}$, voltage-limited waveforms for input signals that are greater than $10mV_{PP}$. Applications requiring the SY88973BL to operate with high gain should have the upstream TIA placed as close as possible to the SY88973BL's input pins to ensure the device's best performance.

Output Buffer

The SY88973BL's CML output buffer is designed to drive 50Ω lines. The output buffer requires appropriate termination for proper operation. An external 50Ω resistor -to-VCC or equivalent for each output pin provides this. Figure 3 shows a simplified schematic of the output structure and includes an appropriate termination method. Of course, driving a downstream device with a CML input that is internally terminated with 50Ω -to-V_{CC} eliminates the need for external termination. As noted in the previous section, the amplifier outputs, typically, $800mV_{PP}$, waveforms across 25Ω total loads. The output buffer, thus, switches typically 16mA tail-current. Figure 4 shows the power supply current measurement which excludes the 16mA tail-current.

Loss-of-Signal (LOS)

The SY88973BL incorporates a chatter-free, LOS open-collector TTL output. For proper operation, an external 4.75kΩ to 10kΩ pull-up resistor between LOS and Vcc is required. LOS is used to determine that the input amplitude is too small to be considered a valid input. LOS asserts high if the input amplitude falls below the threshold set by LOSLVL and de-asserts low otherwise. LOS can be fed back to the enable (/EN) input to maintain output stability under a loss of signal condition. /EN de-assert low the true output signal without removing the input signals. Typically, 4.6dB LOS hysteresis is provided to prevent chattering.

Loss-of-Signal Level Set

A programmable, loss-of-signal level set pin sets the threshold of the input amplitude detection. Connecting an external resistor between V_{CC} and LOSLVL sets the voltage at LOSLVL. This voltage ranges from V_{CC} to V_{REF}. The external resistor creates a voltage divider between V_{CC} and REF as shown in Figure 6. If desired, an appropriate external voltage may be applied rather than using a resistor. The relationship between V_{LOSLVL} and R_{LOSLVL} is given by:

$$V_{LOSLVL} = V_{CC} - 1.3\frac{R_{LOSLVL}}{R_{LOSLVL} + 2.8}$$

where voltages are in volts and resistances are in kΩ.

The smaller the external resistor, which implies a smaller voltage difference from L_{OSLVL} to V_{CC}, the lower the LOS sensitivity. Hence, larger input amplitude is required to de-assert LOS. The "Typical Operating Characteristics" section contains graphs showing the relationship between the input amplitude detection sensitivity and V_{LOSLVL} or R_{LOSLVL}.

Hysteresis

The SY88973BL provides typically 4.6dB LOS electrical hysteresis. By definition, a power ratio measured in dB is 10log (power ratio). Power is calculated as V^2_{IN}/R for an electrical signal. Hence, the same ratio can be stated as 20log (voltage ratio). While in linear mode, the electrical voltage input changes linearly with the optical power and the ratios change linearly as well. Therefore, the optical hysteresis in dB is half the electrical hysteresis in dB given in the datasheet. The SY88973BL provides typically 2.3dB LOS optical hysteresis. As the SY88973BL is an electrical device, this datasheet refers to hysteresis in electrical terms. With 4.6dB LOS hysteresis, a voltage factor of 1.7 is required to de-assert LOS.

Hysteresis and Sensitivity Improvement

If increased LOS sensitivity and hysteresis are required, an application note entitled "Notes on Sensitivity and Hysteresis in Micrel Post Amplifiers" is available at: http://www.micrel.com/_PDF/HBW/App-Notes/an-45.pdf.

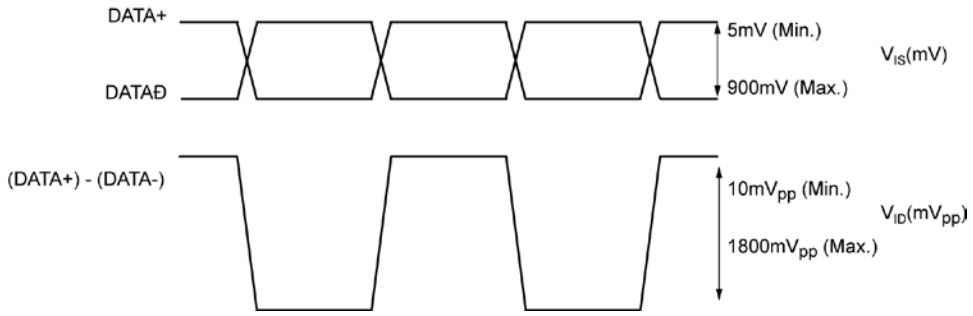


Figure 1. VIS and VID Definition

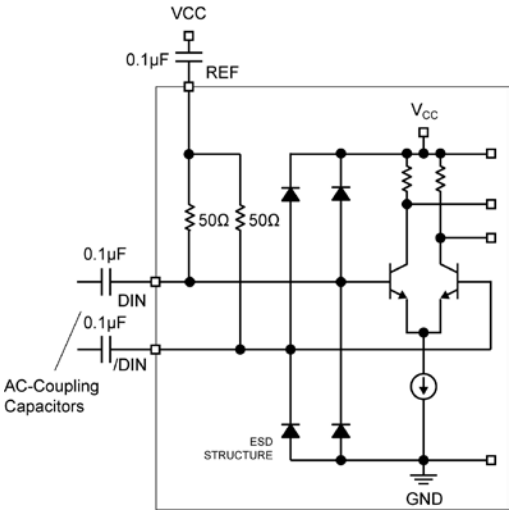


Figure 2. Input Structure

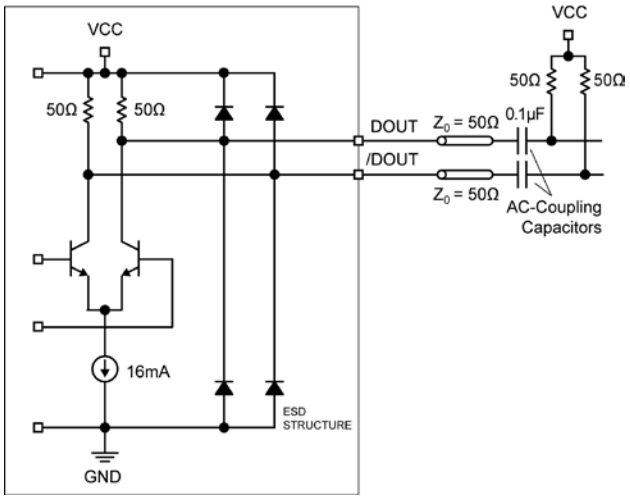


Figure 3. Output Structure

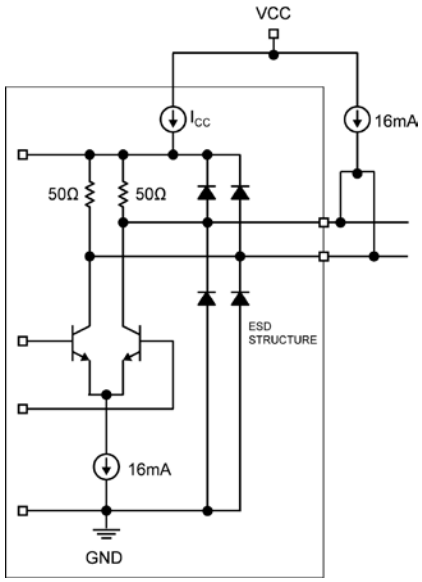


Figure 4. Power Supply Current Measurement

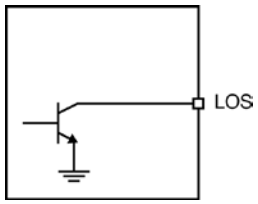


Figure 5. LOS Output Structure

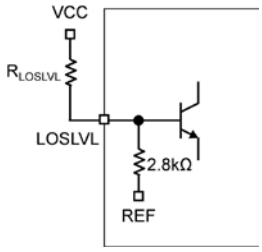
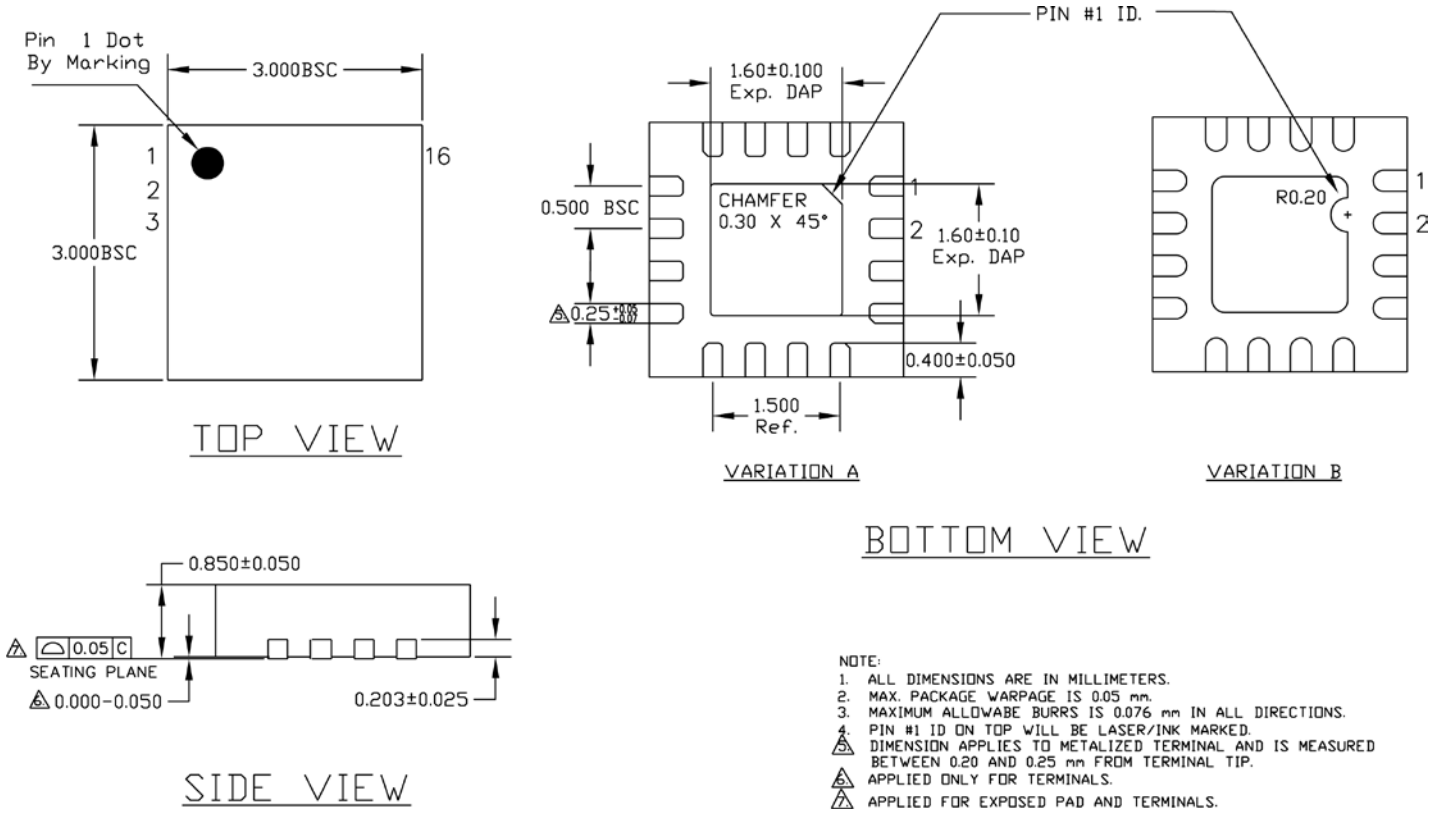
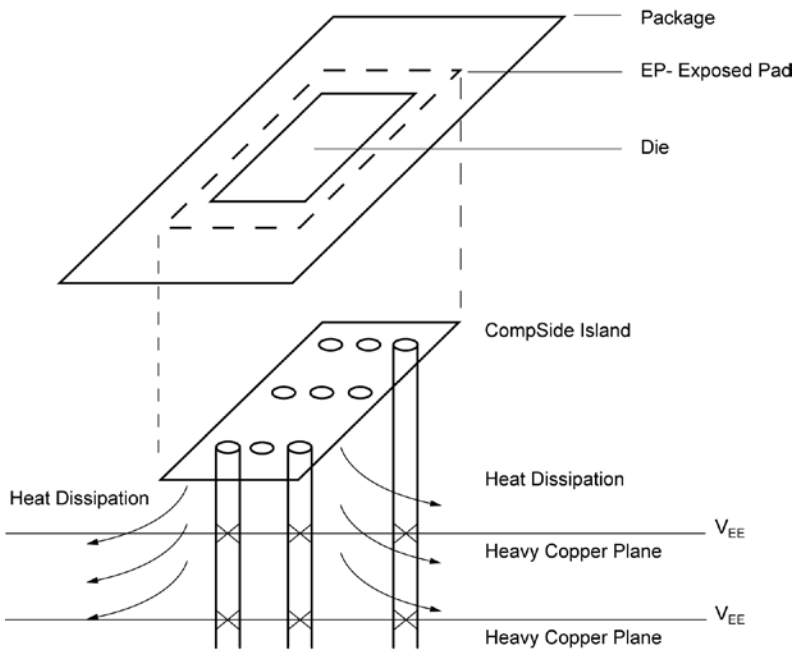


Figure 6. LOSLVL Setting Circuit

Package Information



16-Pin QFN



PCB Thermal Consideration for 16-Pin QFN Package
(Always solder, or equivalent, the exposed pad to the PCB)

Package Notes:

1. Package meets Level 2 qualification.
2. All parts are dry-packaged before shipment.
3. Exposed pad must be soldered to a ground for proper thermal management; solder void has to be less than 50% of the epad area.

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