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3.3V/5V 3.2Gbps CML LOW-POWER LIMITING POST AMPLIFIER w/TTL SD

SY88983V

FEATURES

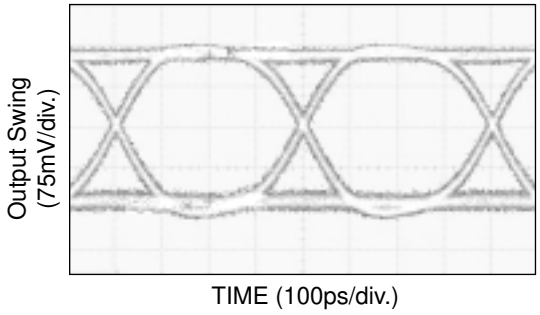
- **Multi-Rate up to 3.2Gbps operation**
- **Wide gain-bandwidth product**
  - **38dB differential gain**
  - **2.2GHz 3dB bandwidth**
- **Low noise 50Ω CML data outputs**
  - **800mV$_{pp}$ output swing**
  - **60ps edge rates**
  - **5ps$_{rms}$ typ. random jitter**
  - **15ps$_{pp}$ typ. deterministic jitter**
- **Chatter-free Signal Detect (SD) output**
  - **4.6dB electrical hysteresis**
  - **OC-TTL output with internal 5kΩ pull-up resistor**
- **Programmable SD sensitivity using single external resistor**
- **Internal 50Ω data input termination**
- **TTL EN input allows feedback from SD**
- **Wide operating range**
  - **Single 3.3V ±10% or 5V ±10% power supply**
  - **–40°C to +85°C industrial temperature range**
- **Available in tiny 10-pin MSOP (3mm) and 16-pin MLF™ (3mm × 3mm) packages**
- **NOT RECOMMENDED for New Designs!**

APPLICATIONS

- **1.25Gbps and 2.5Gbps Gigabit Ethernet**
- **1.062Gbps and 2.125Gbps Fibre Channel**
- **155Mbps, 622Mbps, 1.25Gbps and 2.5Gbps SONET/SDH**
- **Gigabit interface converter (GBIC)**
- **Small form factor (SFF) and small form factor pluggable (SFP) transceivers**
- **Parallel 10G Ethernet**
- **High-gain line driver and line receiver**

TYPICAL PERFORMANCE

3.3V, 25°C, 10mV$_{PP}$ Input
@2.5Gbps 2^{23}-1 PRBS, R_{LOAD} = 50Ω to V_{CC}



DESCRIPTION

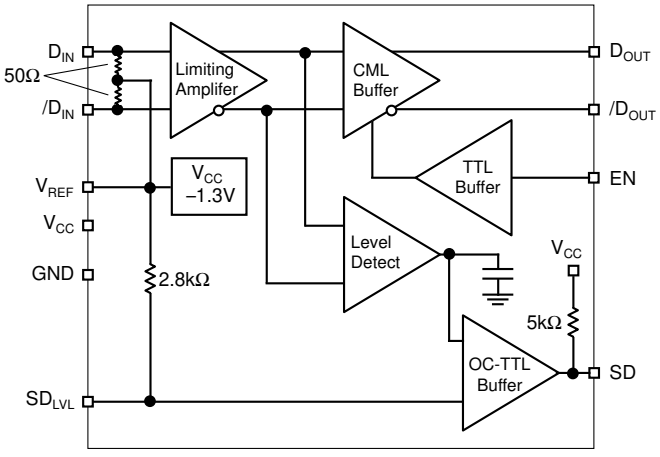
The SY88983V low-power limiting post amplifier is designed for use in fiber optic receivers. The device connects to typical transimpedance amplifiers (TIAs). The linear signal output from TIAs can contain significant amounts of noise and may vary in amplitude over time. The SY88983V quantizes these signals and outputs typically 800mV$_{pp}$ voltage-limited waveforms.

The SY88983V operates from a single +3.3V ±10% or +5V ±10% power supply, over the industrial temperature of –40°C to +85°C. With its wide bandwidth and high gain, signals with data rates up to 3.2Gbps and as small as 10mV$_{pp}$ can be amplified to drive devices with CML inputs or AC-coupled PECL inputs.

The SY88983V generates a signal detect (SD) open-collector TTL output with internal 5kΩ pull-up resistor. A programmable signal detect level set pin (SD_{LVL}) sets the sensitivity of the input amplitude detection. SD asserts high if the input amplitude rises above the threshold set by SD_{LVL} and de-asserts low otherwise. SD can be fed back to the enable (EN) input to maintain output stability under a loss-of-signal condition. EN de-asserts the true output signal without removing the input signal. Typically, 4.6dB SD hysteresis is provided to prevent chattering.

All support documentation can be found on Micrel's web site at www.micrel.com.

FUNCTIONAL BLOCK DIAGRAM



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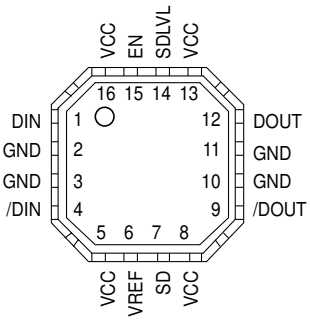
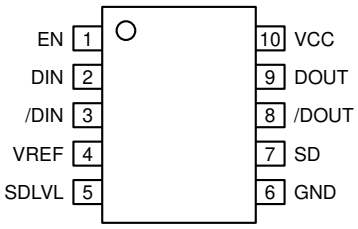
PACKAGE/ORDERING INFORMATION



16-Pin MLF™ (MLF-16)



10-Pin MSOP (K10-1)

Ordering Information

Part Number	Package Type	Operating Range	Package Marking
SY88983VKI	K10-1	Industrial	983V
SY88983VKITR[1]	K10-1	Industrial	983V
SY88983VMI	MLF-16	Industrial	983V
SY88983VMITR[1]	MLF-16	Industrial	983V

Note:

1. Tape and Reel.

PIN DESCRIPTION

Pin Number (MSOP)	Pin Number (MLF™)	Pin Name	Type	Pin Function
1	15	EN	TTL Input: Default is high.	Enable: De-asserts true data output when low.
2, 3	1, 4	DIN, /DIN	Differential Data Input	Differential data input. Each pin internally terminates to V_{REF} through 50Ω.
4	6	VREF		Reference Voltage: Bypass with 0.01µF low ESR capacitor from V_{REF} to V_{CC} to stabilize SD_{LVL} and V_{REF}.
5	14	SDLVL	Input: Default is maximum sensitivity.	Signal Detect Level Set: A resistor from this pin to V_{CC} sets the threshold for the data input amplitude at which the SD output will be asserted.
6	2, 3, 10, 11, Exposed Pad	GND	Ground	Device ground. Exposed pad must be connected to same potential as ground pins for MLF-16.
7	7	SD	Open-Collector: TTL Output with internal 5kΩ pull-up resistor.	Signal Detect: Asserts high when the data input amplitude rises above the threshold set by SD_{LVL}.
8, 9	9, 12	DOUT, /DOUT	Differential CML Output	Differential data output.
10	5, 8, 13, 16	VCC	Power Supply	Positive power supply. Bypass with 0.1µF||0.01µF low ESR capacitors. 0.01µF capacitors should be as close to V_{CC} pins as possible.

Absolute Maximum Ratings[1]

Supply Voltage (V_{CC}) ..... 0V to +7.0V
EN, SD_{LVL} Voltage ..... 0 to V_{CC}
D_{IN}, $/D_{IN}$ Current ..... ±10mA
D_{OUT}, $/D_{OUT}$ Current ..... ±25mA
SD Current ..... ±5mA
V_{REF} Current ..... ±1mA
Storage Temperature (T_S) ..... –65°C to +150°C
Lead Temperature (soldering, 10 sec.) ..... 220°C

Operating Ratings[2]

Supply Voltage (V_{CC}) ..... +3.0V to +3.6V or
..... +4.5V to +5.5V
Ambient Temperature (T_A) ..... –40°C to +85°C
Junction Temperature (T_J) ..... –40°C to +120°C
Package Thermal Resistance[3]
MLF™
(θ_{JA}) Still-Air ..... 61°C/W
(ψ_{JB}) ..... 38°C/W
MSOP
(θ_{JA}) Still-Air ..... 113°C/W
(ψ_{JB}) ..... 74°C/W

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 3.0V to 3.6V or 4.5V to 5.5V; R_{LOAD} = 50Ω to V_{CC}; T_A = –40°C to +85°C; typical values at V_{CC} = 3.3V, T_A = 25°C.

Symbol	Parameter	Condition	Min	Typ	Max	Units
I_{CC}	Power Supply Current[4]	3.3V 5V		19 21	28 31	mA mA
I_{CC}	Power Supply Current[5]	3.3V 5V		32 38	53 58	mA mA
V_{REF}	V_{REF} Voltage			V_{CC} –1.3		V
SD_{LVL}	SD_{LVL} Level		V_{REF}		V_{CC}	V
V_{OH}	Output HIGH Voltage	**Note 6**	V_{CC}–0.020	V_{CC}–0.005	V_{CC}	V
V_{OL}	Output LOW Voltage	**Note 6**		V_{CC}–0.400	V_{CC}–0.275	V
V_{OFFSET}	Differential Output Offset				±80	mV
Z_O	Single-Ended Output Impedance		40	50	60	Ω
Z_I	Single-Ended Input Impedance		40	50	60	Ω

TTL DC ELECTRICAL CHARACTERISTICS

V_{CC} = 3.0V to 3.6V or 4.5V to 5.5V; R_{LOAD} = 50Ω to V_{CC}; T_A = –40°C to +85°C; typical values at V_{CC} = 3.3V, T_A = 25°C.

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{OH}	SD Output HIGH Level	Sourcing 100µA	2.4		V_{CC}	V
V_{OL}	SD Output LOW Level	Sinking 2mA			0.5	V
V_{IH}	EN Input HIGH Voltage		2.0			V
V_{IL}	EN Input LOW Voltage				0.8	V
I_{IH}	EN Input HIGH Current	V_{IN} = 2.7V V_{IN} = V_{CC}			20 100	µA µA
I_{IL}	EN Input LOW Current	V_{IN} = 0.5V	–0.3			mA

Notes:

1. Permanent device damage may occur if *"Absolute Maximum Ratings"* are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to *"Absolute Maximum Ratings"* conditions for extended periods may affect device reliability.
2. The data sheet limits are not guaranteed if the device is operated beyond the operating ratings.
3. Thermal performance assumes use of 4-layer PCB. If applicable, exposed pad must be soldered (or equivalent) to the device's most negative potential on the PCB.
4. Excludes current of CML output stage. See *"Detailed Description."*
5. Total device current with no output load.
6. Output levels are based on a 50Ω to V_{CC} load impedance. If the load impedance is different, the output level will be changed.

AC ELECTRICAL CHARACTERISTICS

V_{CC} = 3.0V to 3.6V or 4.5V to 5.5V; R_{LOAD} = 50Ω to V_{CC}; T_A = –40°C to +85°C; typical values at V_{CC} = 3.3V, T_A = 25°C.

Symbol	Parameter	Condition	Min	Typ	Max	Units
HYS	SD Hysteresis	**Note 7**	2	4.6	8	dB
PSRR	Power Supply Rejection Ratio			35		dB
t_{OFF}	SD Release Time			0.1	0.5	µs
t_{ON}	SD Assert Time			0.2	0.5	µs
t_r, t_f	Differential Output Rise/Fall Time (20% to 80%)	**Note 8**		60	120	ps
t_{JITTER}	Deterministic Random	**Note 9**		15 5		ps_{p-p} ps_{rms}
V_{ID}	Differential Input Voltage Swing		10		1800	mV_{p-p}
V_{OD}	Differential Output Voltage Swing	**Note 10**	550	800		mV_{p-p}
V_{SR}	SD Sensitivity Range	**Note 11**	10		50	mV_{p-p}
$A_{V(Diff)}$	Differential Voltage Gain		32	38		dB
$B_{–3dB}$	3dB Bandwidth			2.2		GHz
S_{21}	Single-Ended Small Signal-Gain		26	32		dB

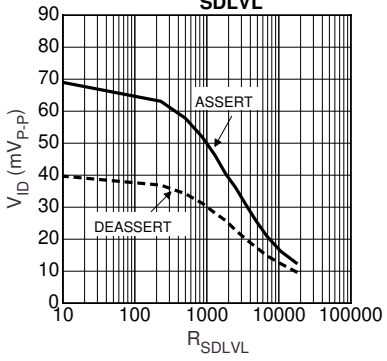
Notes:

7. Electrical signal.
8. With input signal V_{ID} > 50mV_{p-p} and 50Ω load.
9. Deterministic jitter measured using K28.5 pattern at 2.488Gbps, V_{ID} = 10mV_{p-p}. Random jitter measured using K28.7 pattern at 2.488Gbps, V_{ID} = 10mV_{p-p}.
10. Input is a 200MHz square wave, t_r < 300ps, 50Ω load. V_{ID} ≥ 14mV_{p-p}.
11. This is the detectable range of input amplitudes that can de-assert SD. The input amplitude to assert SD is 2–8dB higher than the de-assert amplitude. See *"Typical Operating Characteristics"* for a graph showing how to choose a particular R_{SDLVL} for a particular SD de-assert, and its associated assert, amplitude.

TYPICAL OPERATING CHARACTERISTICS

V_{CC} = 3.3V, GND = 0V, T_A = 25°C unless otherwise stated.

SD Assert/Deassert Level vs. R_{SDLVL}



DETAILED DESCRIPTION

The SY88983V low power limiting post amplifier operates from a single +3.3V or +5V power supply, over temperatures from –40°C to +85°C. Signals with data rates up to 3.2Gbps and as small as $10mV_{p-p}$ can be amplified. Figure 1 shows the allowed input voltage swing. The SY88983V generates an SD output, allowing feedback to EN for output stability. SD_{LVL} sets the sensitivity of the input amplitude detection.

Input Amplifier/Buffer

The SY88983V's inputs are internally terminated with 50Ω to V_{REF}. Unless they are not affected by this internal termination scheme, upstream devices need to be AC-coupled to the SY88983V's inputs. Figure 2 shows a simplified schematic of the input stage.

The high sensitivity of the input amplifier allows signals as small as $10mV_{p-p}$ to be detected and amplified. The input amplifier allows input signals as large as $1800mV_{p-p}$. Input signals are linearly amplified with a typically 38dB differential voltage gain. Since it is a limiting amplifier, the SY88983V outputs typically $800mV_{p-p}$ voltage-limited waveforms for input signals that are greater than $10mV_{p-p}$. Applications requiring the SY88983V to operate with high-gain should have the upstream TIA placed as close as possible to the SY88983V's input pins to ensure the best performance of the device.

Output Buffer

The SY88983V's CML output buffer is designed to drive 50Ω lines. The output buffer requires appropriate termination for proper operation. An external 50Ω resistor to V_{CC} or equivalent for each output pin provides this. Figure 3 shows a simplified schematic of the output stage and includes an appropriate termination method. Of course, driving a downstream device with a CML input that is internally terminated with 50Ω to V_{CC} eliminates the need for external termination. As noted in the previous section, the amplifier outputs typically $800mV_{p-p}$ waveforms across 25Ω total loads. The output buffer, thus, switches typically 16mA tail-current. Figure 4 shows the power supply current measurement, which excludes the 16mA tail-current.

Signal Detect

The SY88983V generates a chatter-free signal detect (SD) open-collector TTL output with internal 5kΩ pull-up resistor as shown in Figure 5. SD is used to determine that the input amplitude is large enough to be considered a valid input. SD asserts high if the input amplitude rises above the threshold set by SD_{LVL} and de-asserts low otherwise. SD can be fed back to the enable (EN) input to maintain output stability under a loss-of-signal condition. EN de-asserts low the true output signal without removing the input signals. Typically, 4.6dB SD hysteresis is provided to prevent chattering.

Signal Detect-Level Set

A programmable signal detect-level set pin (SD_{LVL}) sets the threshold of the input amplitude detection. Connecting an external resistor between V_{CC} and SD_{LVL} sets the voltage at SD_{LVL}. This voltage ranges from V_{CC} to V_{REF}. The external resistor creates a voltage divider between V_{CC} and V_{REF} as shown in Figure 6. If desired, an appropriate external voltage may be applied rather than using a resistor. The smaller the external resistor, implying a smaller voltage difference from SD_{LVL} to V_{CC}, lowers the SD sensitivity. Hence, larger input amplitude is required to assert SD. *"Typical Operating Characteristics"* shows the relationship between the input amplitude detection sensitivity and the SD_{LVL} setting resistor.

Hysteresis

The SY88983V provides typically 4.6dB SD electrical hysteresis. By definition, a power ratio measured in dB is 10log(power ratio). Power is calculated as V^2_{IN}/R for an electrical signal. Hence, the same ratio can be stated as 20log(voltage ratio). While in linear mode, the electrical voltage input changes linearly with the optical power and hence, the ratios also change linearly. Therefore, the optical hysteresis in dB is half the electrical hysteresis in dB given in the data sheet. The SY88983V provides typically 2.3dB SD optical hysteresis. As the SY88983V is an electrical device, this data sheet refers to hysteresis in electrical terms. With 4.6dB SD hysteresis, a voltage factor of 1.7 is required to assert SD from its de-assert value.

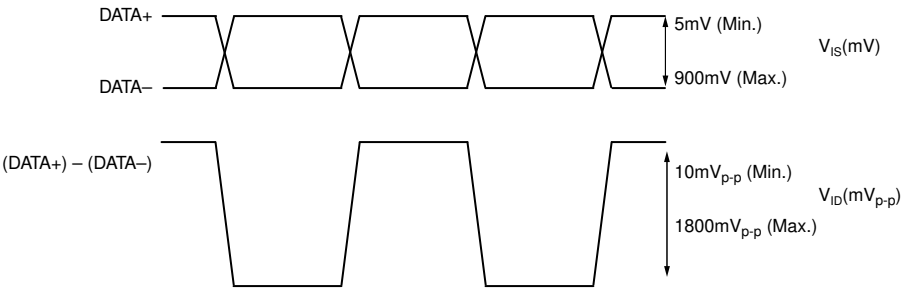


Figure 1. V_{IS} and V_{ID} Definition

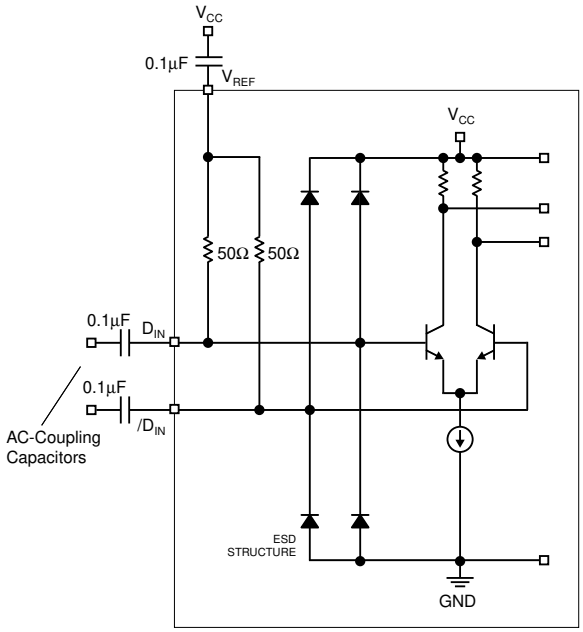


Figure 2. Input Structure

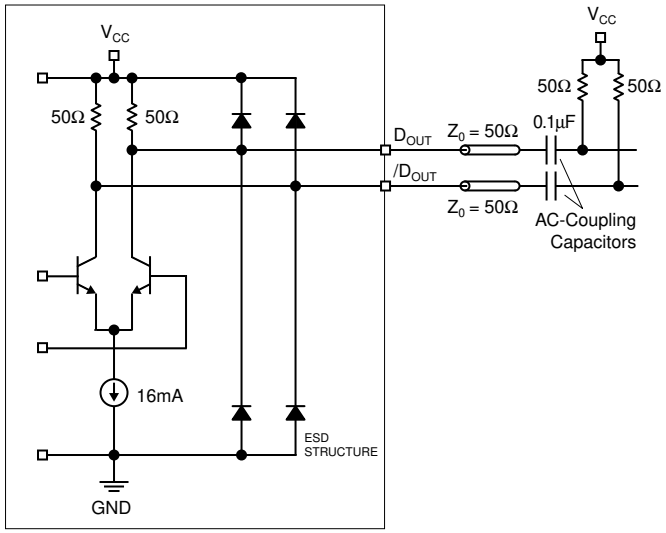


Figure 3. Output Structure

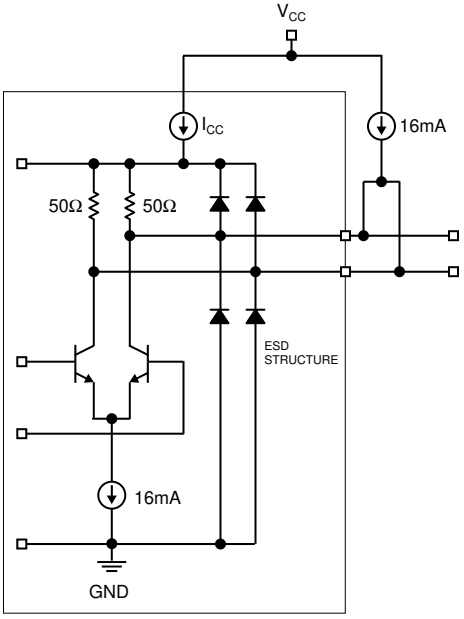


Figure 4. Power Supply Current Measurement

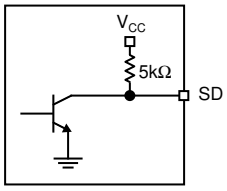


Figure 5. SD Output Structure

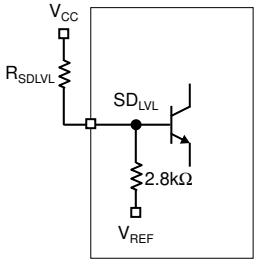
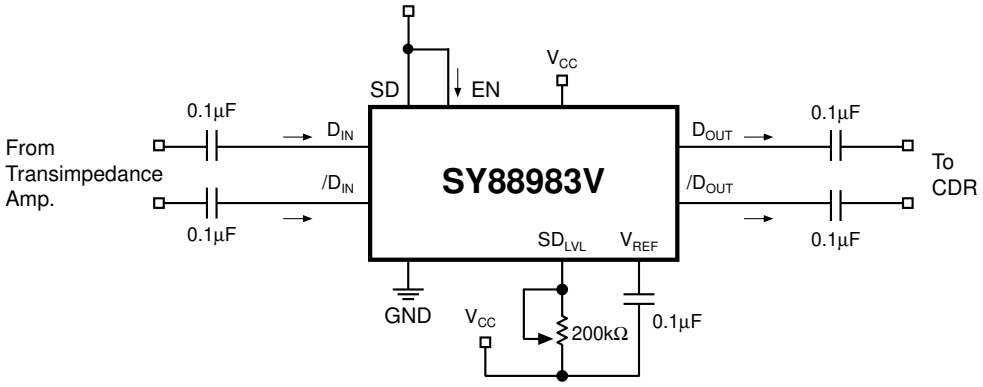
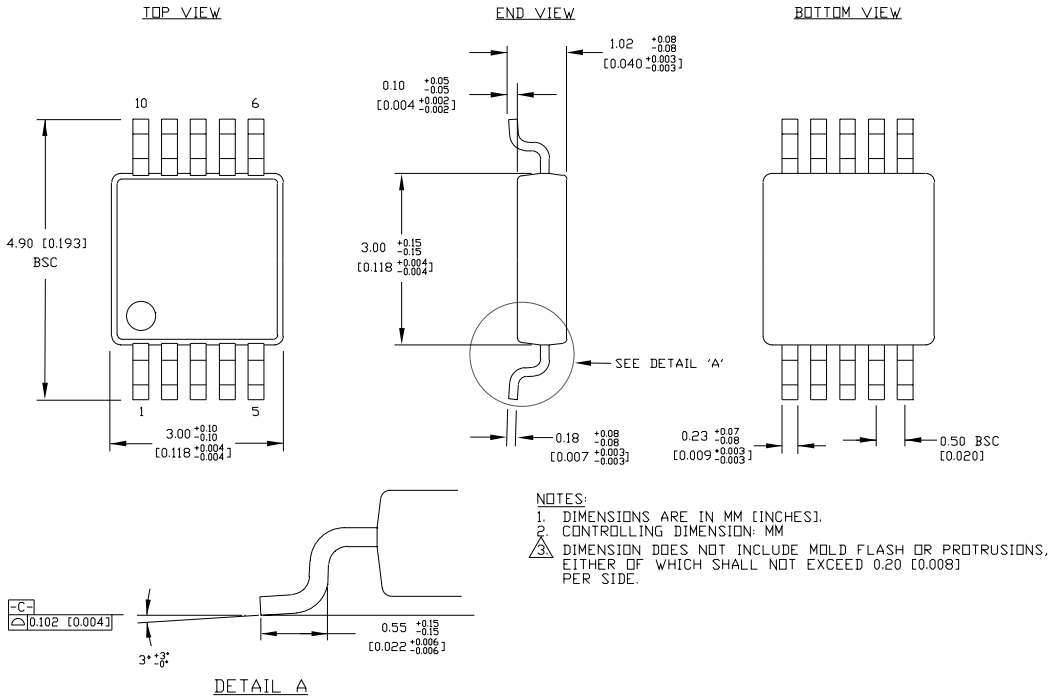


Figure 6. SD_{LVL} Setting Circuit

TYPICAL APPLICATIONS CIRCUIT

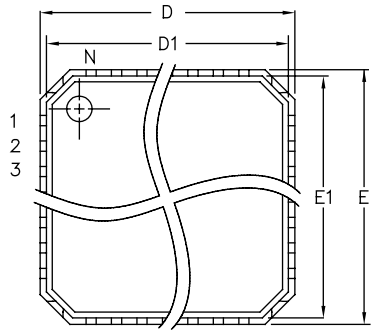


10 LEAD MSOP (K10-1)

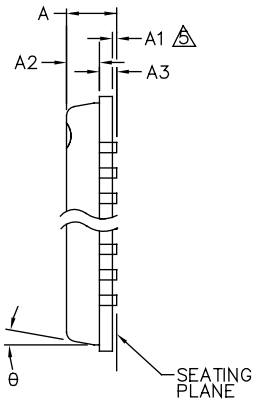


Rev. 00

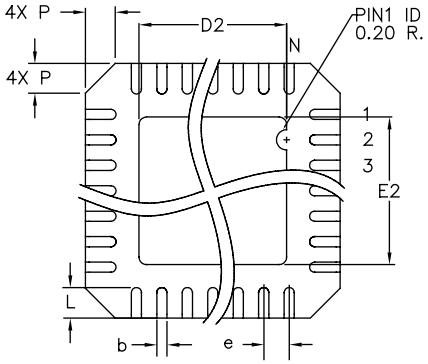
16 LEAD *Micro*LeadFrame™ (MLF-16)



TOP VIEW



	DIMENSION (mm)		
	MIN.	NOM.	MAX.
A	–	0.85	1.00
A1	0.00	0.01	0.05
A2	–	0.65	0.80
A3		0.20 REF.	
D		3.00 BSC	
D1		2.75 BSC	
D2	1.35	1.50	1.65
E		3.00 BSC	
E1		2.75 BSC	
E2	1.35	1.50	1.65
θ			12°
P	0.24	0.42	0.60
e		0.50 BSC	
N		16	
L	0.30	0.40	0.50
b	0.18	0.23	0.30



BOTTOM VIEW

NOTE:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. N IS THE NUMBER OF TERMINALS.
   THE NUMBER OF TERMINALS PER SIDE IS N/4.
3. THE PIN#1 IDENTIFIER MUST BE EXISTED ON THE TOP SURFACE OF PACKAGE BY USING IDENTIFICATION MARK OR OTHER FEATURE OF PACKAGE BODY.
4. PACKAGE WARPAGE MAX 0.05mm.

5 APPLIED FOR EXPOSED PAD AND TERMINALS.

Rev.03

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