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# 3.3V DUAL TTL-to-DIFFERENTIAL PECL TRANSLATOR

Precision Edge®  
SY89222L

## FEATURES

- 3.3V power supply
- 300ps typical propagation delay
- <100ps output-to-output skew
- Differential LVPECL outputs
- PNP TTL inputs for minimal loading
- Flow-through pinouts
- Available in ultra-small 8-pin MLF™ (2mm x 2mm) package



Precision Edge®

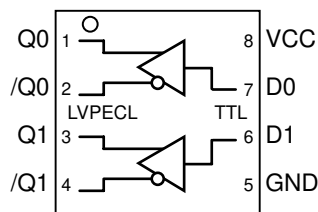
## DESCRIPTION

The SY89222L is a dual TTL-to-differential LVPECL translator with a +3.3V power supply. Because LVPECL (Positive ECL) levels are used, only +3.3V and ground are required. The SY89222L is functionally equivalent to the SY100ELT22L but in an ultra-small 8-lead MLF™ package that features a 70% smaller footprint. The low skew, dual gate design of the SY89222L makes it ideal for applications that require the translation of a clock and a data signal.

## FUNCTIONAL CROSS REFERENCE

Micrel Part Number		Functional Cross
2x2 MLF™	PECL	8-SOIC
SY89222L	100K	SY100ELT22

**PACKAGE/ORDERING INFORMATION**



**TOP VIEW**  
**8-Pin MLF™**  
**Ultra-Small Outline (2mm x 2mm)**

**Ordering Information<sup>(1)</sup>**

Part Number	Package Type	Operating Range	Package Marking	Lead Finish
SY89222LMITR <sup>(2)</sup>	MLF-8	Industrial	222	Sn-Pb
SY89222LMGTR <sup>(2)</sup>	MLF-8	Industrial	222 with Pb-Free bar-line indicator	Pb-Free NiPdAu

**Notes:**

1. Contact factory for die availability. Dice are guaranteed at T<sub>A</sub> = 25°C, DC electricals only.
2. Tape and Reel.

**PIN DESCRIPTION**

Pin Number	Pin Name	Type	Pin Function
7, 6	D0, D1	TTL Input	Single-ended TTL inputs. If left open, defaults to HIGH.
1, 2, 3, 4	Q0, /Q0, Q1, /Q1	100k LVPECL Output	Differential LVPECL Outputs: See “Output Interface Applications” section for recommendations on terminations. Q defaults to HIGH (/Q defaults to LOW) when D input is left open.
8	VCC	Power	Positive Power Supply: Bypass with 0.1µF//0.01µF low ESR capacitors.
5	GND, Exposed Pad	Ground	GND and Exposed pad must be tied to ground plane.

**Absolute Maximum Ratings**(Note 1)

Supply Voltage ( $V_{CC}$ ) ..... -0.5V to +4.0V  
 Input Voltage ( $V_{IN}$ ) ..... -0.5V to  $V_{CC}$   
 LVPECL Output Current ( $I_{OUT}$ )  
     Continuous ..... 50mA  
     Surge ..... 100mA  
 Input Current  
     Source or sink current on D0, D1 ..... ±50mA  
 Lead Temperature (soldering, 10 sec.) ..... +220°C  
 Storage Temperature ( $T_S$ ) ..... -65°C to +150°C

**Operating Ratings**(Note 2)

Supply Voltage ( $V_{CC}$ ) ..... 3.0V to 3.8V  
 Ambient Temperature ( $T_A$ ) ..... -40°C to +85°C  
 Package Thermal Resistance, (Note 3)  
 MLF™ ( $\theta_{JA}$ )  
     Still-Air ..... 93°C/W  
     500lfpm ..... 87°C/W  
 MLF™ ( $\Psi_{JB}$ )  
     Junction-to-Board ..... 56°C/W

**DC ELECTRICAL CHARACTERISTICS**

Symbol	Parameter	Condition	Min	Typ	Max	Units
$I_{CC}$	Power Supply Current	Max $V_{CC}$ , no load	—	—	25	mA

**TTL DC ELECTRICAL CHARACTERISTICS**(Note 4)

$V_{CC} = +3.0V$  to  $+3.8V$ ;  $T_A = -40^\circ C$  to  $+85^\circ C$ , unless otherwise stated.

Symbol	Parameter	Condition	Min	Typ	Max	Units
$V_{IH}$	Input HIGH Voltage		2.0	—	—	V
$V_{IL}$	Input LOW Voltage		—	—	0.8	V
$I_{IH}$	Input HIGH Current	$V_{IN} = 2.7V$ $V_{IN} = V_{CC}$	—	—	20 100	$\mu A$ $\mu A$
$I_{IL}$	Input LOW Current	$V_{IN} = 0.5V$	—	—	-0.2	mA
$V_{IK}$	Input Clamp Voltage	$I_{IN} = -18mA$	—	—	-1.2	V

**PECL DC ELECTRICAL CHARACTERISTICS**(Note 5)

$V_{CC} = +3.0V$  to  $+3.8V$  and  $V_{EE} = 0V$ ;  $T_A = -40^\circ C$  to  $+85^\circ C$  unless otherwise noted.

Symbol	Parameter	Condition	Min	Typ	Max	Units
$V_{OH}$	Output HIGH Voltage	Note 1	$V_{CC}-1.080$	—	$V_{CC}-0.880$	V
$V_{OL}$	Output LOW Voltage	Note 1	$V_{CC}-1.830$	—	$V_{CC}-1.620$	V

**Note 1.** Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to ABSOLUTE MAXIMUM RATING conditions for extended periods may affect device reliability.

**Note 2.** The data sheet limits are not guaranteed if the device is operated beyond the operating ratings.

**Note 3.** Package thermal resistance assumes exposed pad is soldered (or equivalent) to the devices most negative potential on the PCB.

**Note 4.** Parametric values specified at: 3 volt power supply range +3.0V to +3.8V.

**Note 5.** Output loaded with 50Ω to  $V_{CC}-2V$ .

**AC ELECTRICAL CHARACTERISTICS (Note 6)**

$V_{CC} = +3.0V$  to  $+3.8V$ ;  $T_A = -40^{\circ}C$  to  $+85^{\circ}C$ ,  $R_L = 50\Omega$  to  $V_{CC}-2V$ , unless otherwise stated.

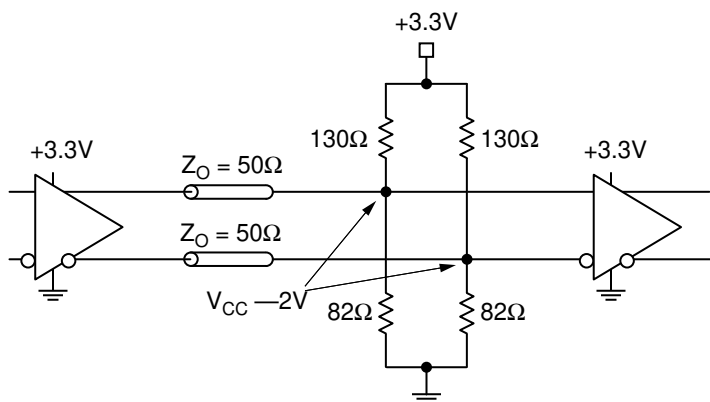
Symbol	Parameter	Condition	Min	Typ	Max	Units
$t_{pd}$	Propagation Delay		100	—	600	ps
$t_r / t_f$	Output Rise/Fall Time 20% to 80%		200	—	500	ps
$t_{skew}$	Within-Device Skew	<b>Notes 6, 7</b>	—	—	100	ps
$t_{skpp}$	Part-to-Part Skew	<b>Note 6</b>	—	—	500	ps
$T_{jitter}$	Cycle-to-cycle	<b>Note 8</b>			1	ps <sub>RMS</sub>

**Note 6.** AC parameters are guaranteed by design and characterization.

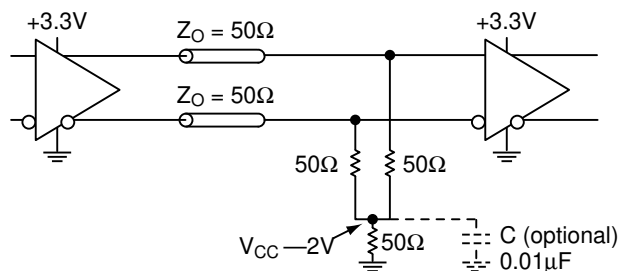
**Note 7.** Same transition, common  $V_{CC}$  levels.

**Note 8.** Cycle-to-cycle jitter definition: the variation in the period between adjacent cycles over a random sample of adjacent cycle pairs:  
 $T_{jitter-CC} = T_n - T_{nt}$ , where T is the time between the rising edges of the output cycle.

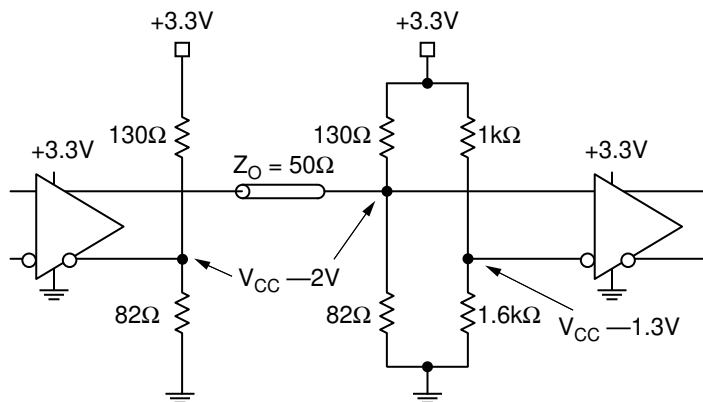
**LVPECL OUTPUT INTERFACE APPLICATIONS**



**Figure 1a. Parallel Thevenin-Equivalent Termination**

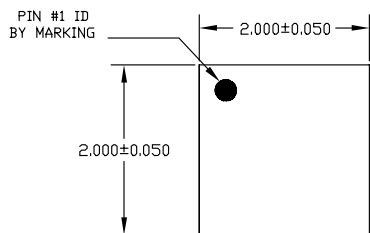


**Figure 1b. Three Resistor "Y Termination"**

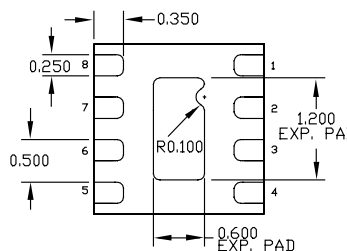


**Figure 1c. Terminating Unused I/O**

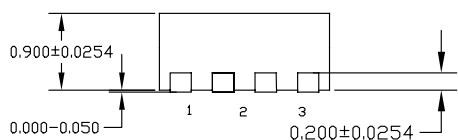
**8 LEAD ULTRA-SMALL EPAD-MicroLeadFrame™ (MLF-8)**



TOP VIEW

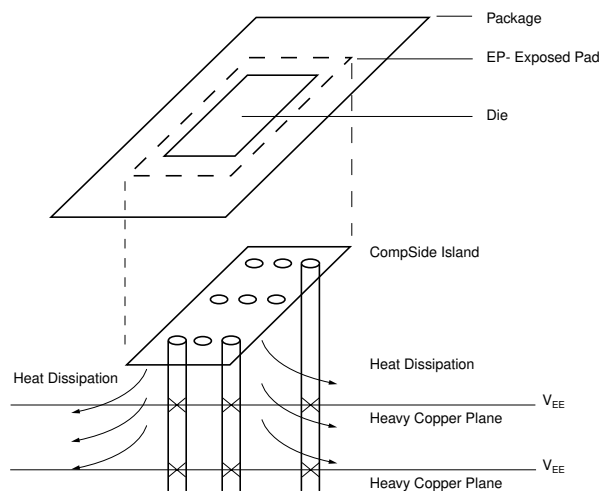


BOTTOM VIEW



SIDE VIEW

- NOTE:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
  2. MAX. PACKAGE WARPAGE IS 0.05 mm.
  3. MAXIMUM ALLOWABLE BURRS IS 0.076 mm IN ALL DIRECTIONS.
  4. PIN #1 ID ON TOP WILL BE LASER/INK MARKED.



PCB Thermal Consideration for 8-Pin MLF™ Package

**Package Notes:**

- Note 1.** Package meets Level 2 qualification.
- Note 2.** All parts are dry-packaged before shipment.
- Note 3.** Exposed pads must be soldered to a ground plane, of the same potential as the GND plane for proper thermal management.

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