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5V/3.3V HIGH-PERFORMANCE PHASE LOCKED LOOP

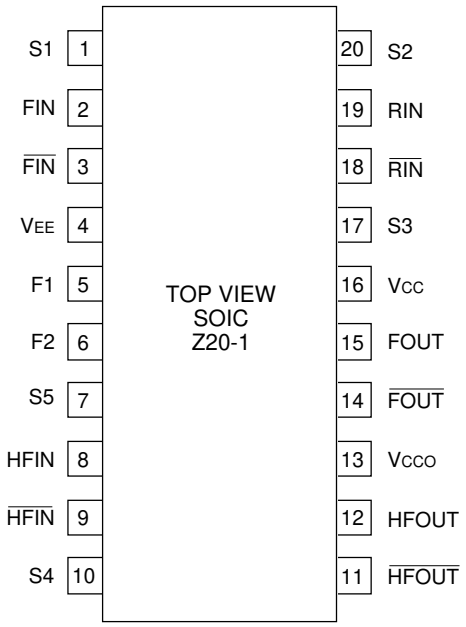
FEATURES

- 3.3V and 5V power supply options
- 1.12GHz maximum VCO frequency
- 30MHz to 560MHz reference input operating frequency
- External 2.0GHz VCO capability
- Low jitter differential design
- Frequency doubler mode
- PECL Differential output
- External loop filter optimizes performance/cost
- Available in 20-pin SOIC package

APPLICATIONS

- Workstations
- Advanced communications
- High-performance computing

PIN CONFIGURATION



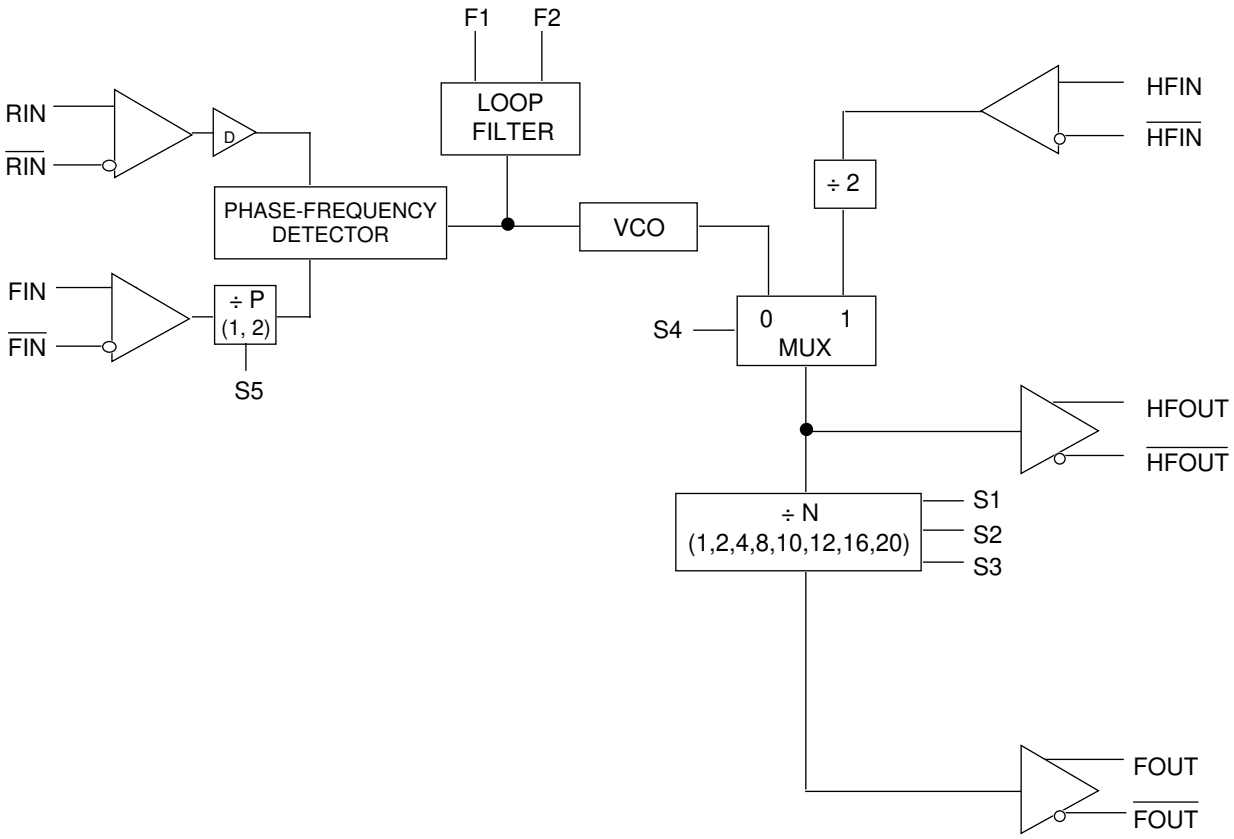
DESCRIPTION

The SY89421V is a digital Phase Locked Loop based on Micrel-Synergy's differential PLL technology. It is capable of operating in the 30MHz to 560MHz reference input frequency range, and up to 2000MHz with the HFIN input and an external VCO. Use of a phase-frequency detector results in excellent PLL locking and tracking characteristics. Error correction voltages are generated by the detector if either phase or frequency deviations occur. The VCO has a frequency range covering more than a 2:1 ratio from 480MHz to 1120MHz.

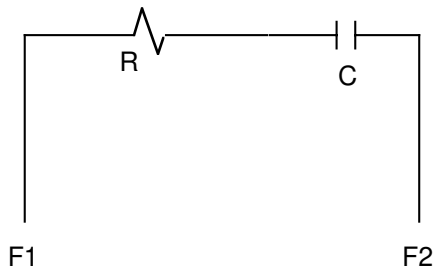
Feedback for the loop is realized by connecting FOUT, $\overline{\text{FOUT}}$ to FIN, $\overline{\text{FIN}}$ by means of external circuitry. This allows the flexibility of inserting additional circuitry off-chip in the feedback paths, such as an additional divider and/or buffer. Pulldown resistors are required for the FOUT and $\overline{\text{FOUT}}$ pins. High frequency inputs HFIN, $\overline{\text{HFIN}}$ and corresponding outputs HFOUT, $\overline{\text{HFOUT}}$ are featured for use with external components such as an active loop filter and a high frequency VCO.

Select pins S1 and S2 are used to program the N divider for optimum VCO operation, in other words with the VCO in the center of its range. Select pin S3 allows bypassing the N divider enabling the PLL to output the VCO directly. Select pin S4 is used to select off-chip or on-chip VCO. Select pin S5 enables the divide-by-two prescaler, which is useful in frequency doubling applications. All Select pins are TTL compatible.

BLOCK DIAGRAM



LOOP FILTER COMPONENT SELECTION



C = 1.0µF ±10% (X7R dielectric)

R = 560Ω ±10%

PIN NAMES

Pin	Function	I/O
F1	Filter Pin 1	I/O
F2	Filter Pin 2	I/O
RIN	Reference Input	I
$\overline{\text{RIN}}$	Inverted Reference Input	I
FIN	Feedback Input	I
$\overline{\text{FIN}}$	Inverted Feeback Input	I
HFIN	High Frequency Input	I
$\overline{\text{HFIN}}$	Inverted High Frequency Input	I
HFOUT	High Frequency Output	O
$\overline{\text{HFOUT}}$	Inverted High Frequency Output	O
FOUT	Frequency Output	O
$\overline{\text{FOUT}}$	Inverted Frequency Output	O
V_{CC}	V_{CC}	—
V_{CCO}	Output V_{CC}	—
V_{EE}	V_{EE} (0V)	—
S1	Select Input 1 (TTL)	I
S2	Select Input 2 (TTL)	I
S3	Select Input 3 (TTL)	I
S4	Select Input 4 (TTL)	I
S5	Select Input 5 (TTL)	I

PIN DESCRIPTION

RIN, $\overline{\text{RIN}}$

Reference frequency inputs. These are differential signal pairs and may be driven differentially or single-ended.

FIN, $\overline{\text{FIN}}$

Feedback frequency inputs. These are a differential signal pair and may be driven differentially or single-ended.

HFIN, $\overline{\text{HFIN}}$

High frequency feedback inputs. These are a differential signal pair. Differential drive is recommended.

F1, F2

These pins are connection points for the loop filter, which is to be provided off-chip. F1 is the high impedance side, F2 is the reference side. The loop filter should be a first order, low pass with a DC block. The difference voltage on these pins will be a dc level, which is controlled by the loop feedback and determined by the required VCO frequency.

FOUT, $\overline{\text{FOUT}}$

Frequency outputs for the loops. These are differential, positive referenced, emitter-follower signals and must be terminated off chip. Termination in 50 ohms is recommended.

HFOUT, $\overline{\text{HFOUT}}$

High frequency output. These are a differential signal pair. Termination in 50 ohms is recommended.

S1, S2, S3, S4, S5

These are the frequency select inputs, and are used to configure the PLL. They are compatible with standard TTL signal levels. See the Frequency Selection Table for details of the logic.

V_{CC}

This is the positive supply for the chip. It should be decoupled and should present a very low impedance in order to assure low-jitter operation.

V_{CCO}

This is the positive supply for the output buffer. It is constrained to be equal to or less than the value of V_{CC}. It should be decoupled and should present a very low impedance for low-jitter.

V_{EE}

This pin is the negative supply for the chip and is normally connected to ground (0V).

FREQUENCY SELECTION TABLE

S4	S3	S2	S1	N	FOUT Freq. Range MHz	HFOUT Freq. Range MHz
0	0	0	0	2	240 – 560	480 – 1120
0	0	0	1	4	120 – 280	480 – 1120
0	0	1	0	8	60 – 140	480 – 1120
0	0	1	1	16	30 – 70	480 – 1120
0	1	0	0	1	480 – 1120	480 – 1120
0	1	0	1	10	48 – 112	480 – 1120
0	1	1	0	12	40 – 93.3	480 – 1120
0	1	1	1	20	20 – 56	480 – 1120
1	0	0	0	2	HFIN divide by 4	HFIN divide by 2
1	0	0	1	4	HFIN divide by 8	HFIN divide by 2
1	0	1	0	8	HFIN divide by 16	HFIN divide by 2
1	0	1	1	16	HFIN divide by 32	HFIN divide by 2
1	1	0	0	1	HFIN divide by 2	HFIN divide by 2
1	1	0	1	10	HFIN divide by 20	HFIN divide by 2
1	1	1	0	12	HFIN divide by 24	HFIN divide by 2
1	1	1	1	20	HFIN divide by 40	HFIN divide by 2

S5	Divide-by-P	Maximum Feedback Frequency (MHz)
0	P = 1	560
1	P = 2	1120

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Parameter	Value	Unit
V_{CC}	Power Supply Voltage	–0.5 to +7.0	V
V_I	TTL Input Voltage[2]	–0.5 to 6.0	V
I_I	TTL Input Current[2]	–30 to +5.0	mA
I_{OUT}	ECL Output Current — Continuous — Surge	 50 100	mA
T_{store}	Storage Temperature	–65 to +150	°C
T_A	Operating Temperature Range[3]	0 to +85	°C

NOTES:

1. Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to ABSOLUTE MAXIMUM RATING conditions for extended periods may affect device reliability.
2. Either voltage limit or current limit is sufficient to protect input.
3. All DC and AC electrical characteristics are specified over the operating termperature range.

5V DC ELECTRICAL CHARACTERISTICS

$V_{CC} = V_{CCO} = 5.0V \pm 5\%$

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
V_{CC}	Power Supply Voltage	4.75	—	5.25	V	$V_{CC} = V_{CCO}$
I_{CC}	Power Supply Current (V_{CC})	—	—	100	mA	
I_{CCO}	Power Supply Current (V_{CCO})	—	—	28	mA	PECL outputs are open

3.3V DC ELECTRICAL CHARACTERISTICS

$V_{CC} = V_{CCO} = 3.3V \pm 5\%$

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
V_{CC}	Power Supply Voltage	3.135	—	3.465	V	$V_{CC} = V_{CCO}$
I_{CC}	Power Supply Current (V_{CC})	—	—	100	mA	
I_{CCO}	Power Supply Current (V_{CCO})	—	—	28	mA	PECL outputs are open

PECL DC ELECTRICAL CHARACTERISTICS

$V_{CC} = V_{CCO} = 3.3V$ or $5.0V \pm 5\%$

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
V_{OH}	Output HIGH Voltage	$V_{CC} – 1.025$	—	$V_{CC} – 0.780$	V	
V_{OL}	Output LOW Voltage	$V_{CC} – 1.810$	—	$V_{CC} – 1.520$	V	
V_{IH}	Input HIGH Voltage	$V_{CC} – 1.165$	—	$V_{CC} – 0.780$	V	
V_{IL}	Input LOW Voltage	$V_{CC} – 1.810$	—	$V_{CC} – 1.475$	V	

TTL DC ELECTRICAL CHARACTERISTICS

$V_{CC} = V_{CCO} = 3.3V$ or $5.0V \pm 5\%$

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
V_{IH}	Input HIGH Voltage	2.0	—	—	V	
V_{IL}	Input LOW Voltage	—	—	0.8	V	
I_{IH}	Input HIGH Current	—	—	20 100	µA	$V_{IN} = 2.7V$ $V_{IN} = V_{CC}$
I_{IL}	Input LOW Current	—	—	–0.3	mA	$V_{IN} = 0.5V$
V_{IK}	Input Clamp Voltage	—	—	– 1.2	V	$I_{IN} = –12mA$

AC ELECTRICAL CHARACTERISTICS

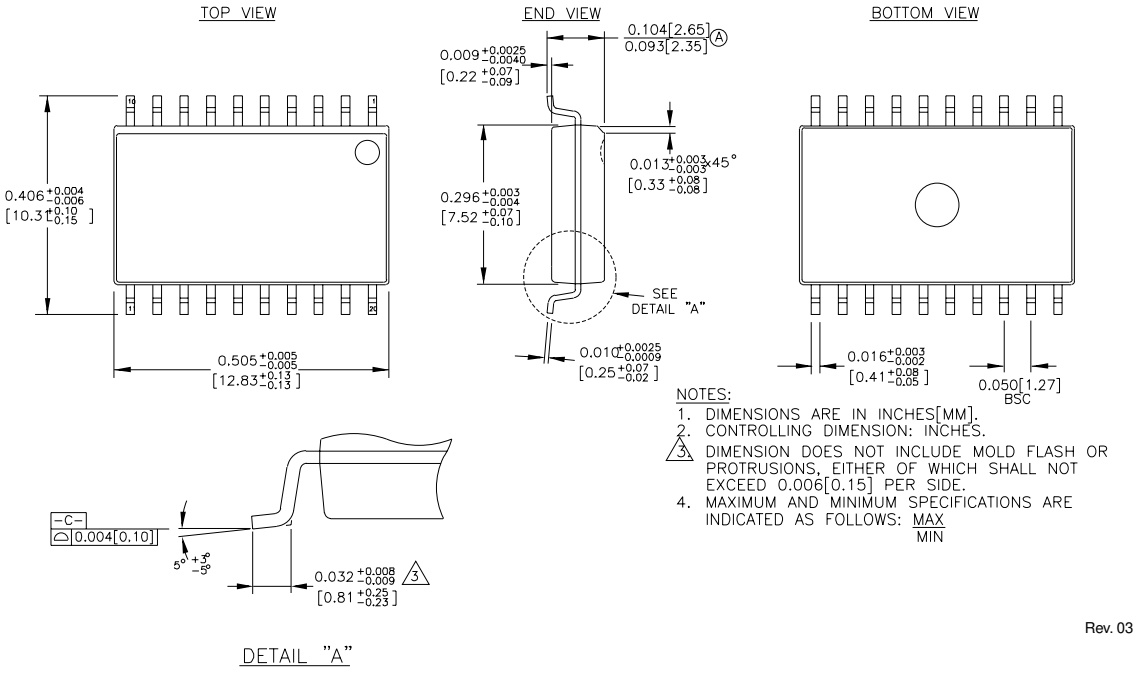
V_{CC} = V_{CCO} = 3.3V or 5.0V ±5%

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
ΔT	Output Period Jitter	—	10	15	ps rms	
P_{PW}	Output Duty Cycle	45	50	55	%	
tr tf	Output Rise/Fall Time (20% to 80%)	— —	300 300	550 550	ps	—
RIN	Reference Frequency Input	—	—	560	MHz	
FIN	Feedback Frequency Input	— —	— —	560 1120	MHz MHz	S5 = 0 S5 = 1
HFIN	High Frequency Input	—	—	2000	MHz	
HFOUT	High Frequency Output	—	—	1120	MHz	
FOUT	Frequency Output	—	—	1120	MHz	

PRODUCT ORDERING CODE

Odering Code	Package Type	Operating Range
SY89421VZC	Z20-1	Commercial
SY89421VZCTR	Z20-1	Commercial

20 LEAD SOIC .300" WIDE (Z20-1)



NOTES:
1. DIMENSIONS ARE IN INCHES[MM].
2. CONTROLLING DIMENSION: INCHES.
3. DIMENSION DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS, EITHER OF WHICH SHALL NOT EXCEED 0.006[0.15] PER SIDE.
4. MAXIMUM AND MINIMUM SPECIFICATIONS ARE INDICATED AS FOLLOWS: MAX / MIN

Rev. 03

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