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3.3V, 3.2Gbps DIFFERENTIAL 4:1 LVDS MULTIPLEXER with 1:2 FANOUT and INTERNAL TERMINATION

Precision Edge®
SY89547L

FEATURES

- Selects among four differential inputs
- Provides two copies of the selected input
- Guaranteed AC performance over temp and voltage:
  - DC-to > 3.2Gbps data rate throughput
  - < 620ps In-to-Out t_{pd}
  - < 150ps t_r/t_f
- Unique input isolation design minimizes crosstalk
- Ultra-low jitter design:
  - < $1ps_{RMS}$ random jitter
  - < $10ps_{PP}$ deterministic jitter
  - < $10ps_{PP}$ total jitter (clock)
  - < $0.7ps_{RMS}$ crosstalk-induced jitter
- Internal input termination
- Unique input termination and V_T pin accepts DC-coupled and AC-coupled inputs (LVDS, LVPECL, CML)
- 350mV LVDS output swing
- Power supply 3.3V ±10%
- –40°C to +85°C temperature range
- Available in 32-pin (5mm x 5mm) MLF® package

Precision Edge®

DESCRIPTION

The SY89547L is a precision, high-speed 4:1 differential multiplexer that provides two copies of the selected input. The high speed LVDS (350mV) compatible outputs with a guaranteed throughput of up to 3.2Gbps over temperature and voltage.

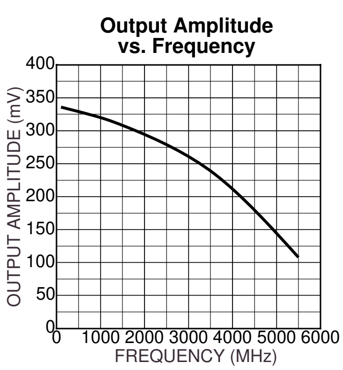
The SY89547L differential inputs include Micrel's unique, 3-pin internal termination design that allows access to the termination network through a V_T pin. This feature allows the device to easily interface to different logic standards, both AC- and DC-coupled without external resistor-bias and termination networks. The result is a clean, stub-free, low jitter interface solution.

The SY89547L operates from a single 3.3V supply, and is guaranteed over the full industrial temperature range (–40°C to +85°C). For applications that require a 2.5V supply, consider the SY89546U. For applications that only require one differential output, consider the SY89544U or SY89545L. The SY89547L is part of a Micrel's Precision Edge® product family. All support documentation can be found on Micrel's web site at: www.micrel.com.

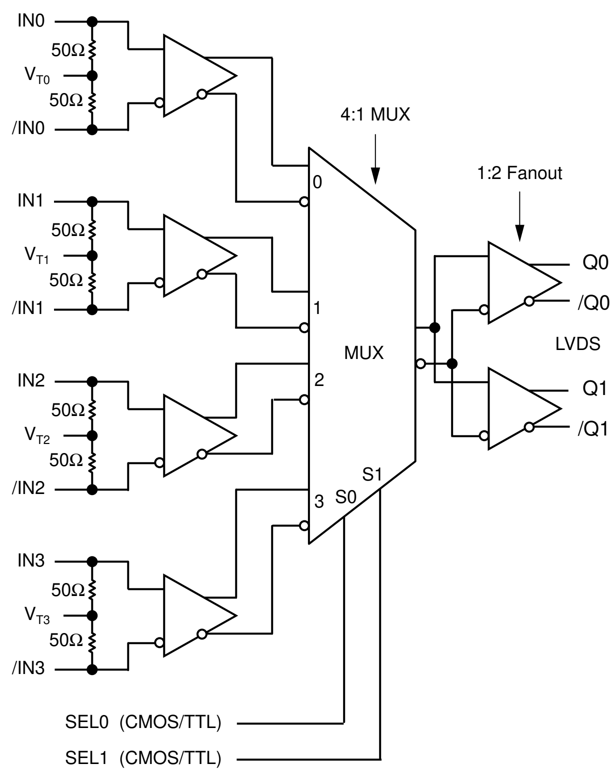
APPLICATIONS

- SONET/SDH multi-channel select applications
- Fibre Channel applications
- GigE applications

TYPICAL PERFORMANCE



FUNCTIONAL BLOCK DIAGRAM



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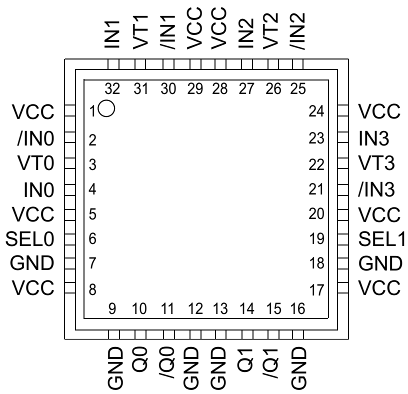
*Micro*LeadFrame and MLF are registered trademarks of Amkor Technology, Inc.

PACKAGE/ORDERING INFORMATION



32-Pin MLF®

Ordering Information(1)

Part Number	Package Type	Operating Range	Package Marking	Lead Finish
SY89547LMI	MLF-32	Industrial	SY89547L	Sn-Pb
SY89547LMITR(2)	MLF-32	Industrial	SY89547L	Sn-Pb
SY89547LMG(3)	MLF-32	Industrial	SY89547L with Pb-Free bar-line indicator	Pb-Free NiPdAu
SY89547LMGTR(2, 3)	MLF-32	Industrial	SY89547L with Pb-Free bar-line indicator	Pb-Free NiPdAu

Notes:

1. Contact factory for die availability. Dice are guaranteed at T_A = 25°C, DC electricals only.
2. Tape and Reel.
3. Recommended for new designs.

PIN DESCRIPTION

Pin Number	Pin Name	Pin Function
4, 2, 32, 30, 27, 25, 23, 21	IN0, /IN0, IN1, /IN1, IN2, /IN2, IN3, /IN3	Differential Inputs: These input pairs are the differential signal inputs to the device. Inputs accept AC- or DC-coupled signals as small as 100mV. Each pin of a pair internally terminates to a V_T pin through 50Ω. Note that these inputs will default to an indeterminate state if left open. Unused differential input pairs can be terminated by connecting one input to V_{CC} and the complementary input to GND through a 1kΩ resistor. The V_T pin is to be left open in this configuration. Please refer to the “Input Interface Applications” section for more details.
3, 31, 26, 22	VT0, VT1, VT2, VT3	Input Termination Center-Tap: Each side of the differential input pair, terminates to a V_T pin. The V_{TA0}, V_{TA1}, V_{TB0}, V_{TB1} pins provide a center-tap to a termination network for maximum interface flexibility. See “Input Interface Applications” section for more details.
6, 19	SEL0, SEL1	These single-ended TTL/CMOS-compatible inputs select the inputs to the multiplexers. Note that these inputs are internally connected to a 25kΩ pull-up resistor and will default to a logic HIGH state if left open. Input switching threshold is $V_{CC}/2$.
1, 5, 8, 17, 20, 24, 28, 29	VCC	Positive Power Supply: Bypass with 0.1µF‖0.01µF low ESR capacitors.
10, 11, 14, 15	Q0, /Q0, Q1, /Q1	Differential Outputs: These LVDS output pairs are the outputs of the device. They are a logic function of the INA0, INA1, INB0, INB1 and SELA and SELB inputs. Please refer to the “Truth Table’” for details. If an output is not used, it must be terminated with 100Ω across the differential pair.
7, 9, 12, 13, 16, 18	GND, Exposed pad	Ground: Ground pin and exposed pad must be connected to the same ground plane.

Absolute Maximum Ratings(1)

Supply Voltage (V_{CC}) .... – 0.5V to + 4.0V
Input Voltage (V_{IN}) .... –0.5V to V_{CC}
Termination Current(3)
Source or sink current on V_T .... ±100mA
Input Current
Source or sink current on IN, /IN .... ±50mA
Lead Temperature (soldering, 20 sec.) .... +260°C
Storage Temperature (T_S) .... –65°C to +150°C

Operating Ratings(2)

Supply Voltage (V_{CC}) .... 3.0V to 3.6V
Ambient Temperature (T_A) .... –40°C to +85°C
Package Thermal Resistance(4)
MLF® (θ_{JA})
Still-Air .... 35°C/W
500lfpm .... 28°C/W
MLF® (Ψ_{JB})
Junction-to-Board .... 20°C/W

DC ELECTRICAL CHARACTERISTICS(5)

T_A = –40°C to +85°C; Unless otherwise stated.

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{CC}	Power Supply		3.0	3.3	3.6	V
I_{CC}	Power Supply Current	No Load, Max. V_{CC}(6)		68	90	mA
R_{DIFF_IN}	Differential Input Resistance (IN-to-/IN)		80	100	120	Ω
R_{IN}	Input Resistance (IN-to-V_T, /IN-to-V_T)		40	50	60	Ω
V_{IH}	Input High Voltage (IN, /IN)		1.2		V_{CC}	V
V_{IL}	Input Low Voltage (IN, /IN)		0		V_{IH}–0.1	V
V_{IN}	Input Voltage Swing (IN, /IN)	**Note 7**	0.1		V_{CC}	V
V_{DIFF_IN}	Differential Input Voltage Swing | IN - /IN |	**Note 7**	0.2			V
IN-to-V_T		**Note 7**			1.8	V

Notes:

1. Permanent device damage may occur if "Absolute Maximum Ratings" are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to "Absolute Maximum Ratings" conditions for extended periods may affect device reliability.
2. The data sheet limits are not guaranteed if the device is operated beyond the operating ratings.
3. Due to the limited drive capability use for input of the same package only.
4. Package thermal resistance assumes exposed pad is soldered (or equivalent) to the device's most negative potential (GND) on the PCB. Ψ_{JB} uses 4-layer θ_{JA} in still-air unless otherwise stated.
5. The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.
6. Includes current through internal 50Ω pull-ups.
7. See "Operating Characteristics" section for V_{IN} and V_{DIFF_IN} definition.

LVDS OUTPUTS DC ELECTRICAL CHARACTERISTICS(9)

V_{CC} = 3.3V ±10%; T_A = –40°C to +85°C; R_L = 100Ω across Q and /Q, unless otherwise stated.

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{OH}	Output HIGH Voltage (Q, /Q)	See Figure 5a			1.475	V
V_{OL}	Output LOW Voltage (Q, /Q)	See Figure 5a	0.925			V
V_{OUT}	Output Voltage Swing (Q, /Q)	See Figures 1a, 5a	250	350		mV
$V_{DIFF-OUT}$	Differential Output Voltage Swing | Q - /Q|	See Figure 1b	500	700		mV
V_{OCM}	Output Common Mode Voltage (Q, /Q)	See Figure 5b	1.125		1.275	V
ΔV_{OCM}	Change in Common Mode Voltage (Q, /Q)	See Figure 5b	–50		+50	mV

LVTTL/CMOS DC ELECTRICAL CHARACTERISTICS(9)

V_{CC} = 3.3V ±10%; T_A = –40°C to +85°C; unless otherwise stated.

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{IH}	Input HIGH Voltage		2.0		V_{CC}	V
V_{IL}	Input LOW Voltage				0.8	V
I_{IH}	Input HIGH Current				40	µA
I_{IL}	Input LOW Current				–300	µA

Note:

9. The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.

AC ELECTRICAL CHARACTERISTICS(10)

V_{CC} = 3.3V ±10%; T_A = –40°C to +85°C; R_L = 100Ω across Q and /Q, unless otherwise stated.

Symbol	Parameter	Condition	Min	Typ	Max	Units
f_{MAX}	Maximum Operating Frequency	NRZ Data	3.2			Gbps
		$V_{OUT} \geq$ 200mV Clock		4		GHz
t_{pd}	Differential Propagation Delay	IN-to-Q	340	440	540	ps
		SEL-to-Q	200	420	700	ps
t_{SKEW}	Input-to-Input Skew	**Note 11**		5	20	ps
	Output-to-Output Skew	**Note 12**		8	20	ps
	Part-to-Part Skew	**Note 13**			200	ps
t_{JITTER}	Data Random Jitter (RJ)	**Note 14**			1	ps_{RMS}
	Deterministic Jitter (DJ)	**Note 15**			10	ps_{PP}
	Clock Total Jitter (TJ)	**Note 16**			10	ps_{PP}
	Cycle-to-Cycle Jitter	**Note 17**			1	ps_{RMS}
Crosstalk	Crosstalk-Induced Jitter	**Note 18**			0.7	ps_{RMS}
t_R, t_F	Output Rise / Fall Time (20% to 80%)	At full output swing	40	80	150	ps

Notes:

10. Measured with 100mV input swing. See "Timing Diagrams" section for definition of parameters. High frequency AC parameters are guaranteed by design and characterization.
11. Input-to-input skew is the difference in time from an input-to-output in comparison to any other input-to-output. In addition, the input-to-input skew does not include the output skew.
12. Output-to-output skew is measured between two different outputs under identical input transitions.
13. Part-to-part skew is defined for two parts with identical power supply voltages at the same temperature and with no skew of the edges at the respective inputs. Total skew is calculated as the RMS (Root Mean Square) of the input skew and output skew.
14. RJ is measured with a K28.7 comma detect character pattern, measured at 1.25Gbps and 3.2Gbps.
15. DJ is measured at 1.25Gbps and 3.2Gbps, with both K28.5 and 2^{23}–1 PRBS pattern.
16. Total jitter definition: with an ideal clock input of frequency $\leq f_{MAX}$, no more than one output edge in 10^{12} output edges will deviate by more than the specified peak-to-peak jitter value.
17. Cycle-to-cycle jitter definition: the variation of periods between adjacent cycles, Tn-Tn-1 where T is the time between rising edges of the output signal.
18. Crosstalk is measured at the output while applying two similar clock frequencies to adjacent inputs that are asynchronous with respect to each other at the inputs.

SINGLE-ENDED AND DIFFERENTIAL SWINGS

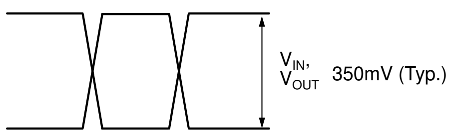


Figure 1a. Single-Ended Voltage Swing

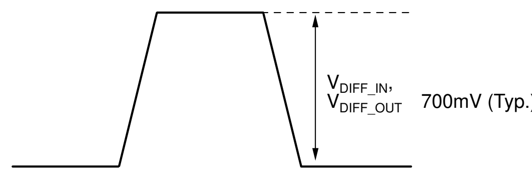


Figure 1b. Differential Voltage Swing

TIMING DIAGRAM

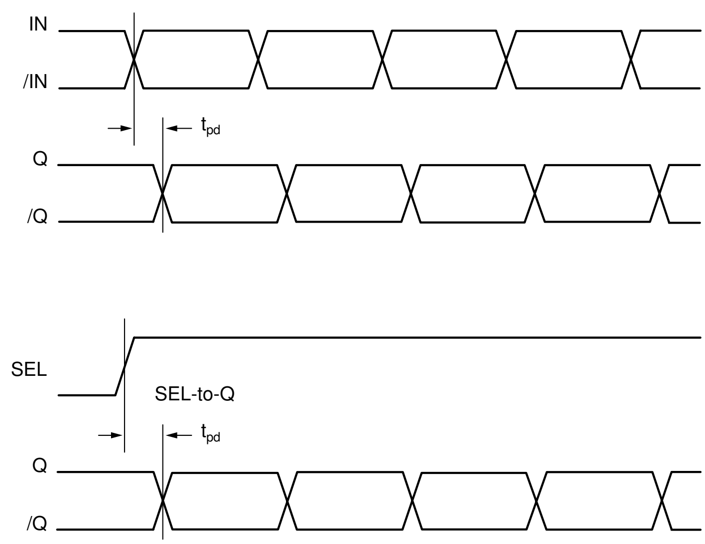


Figure 2. Timing Diagram

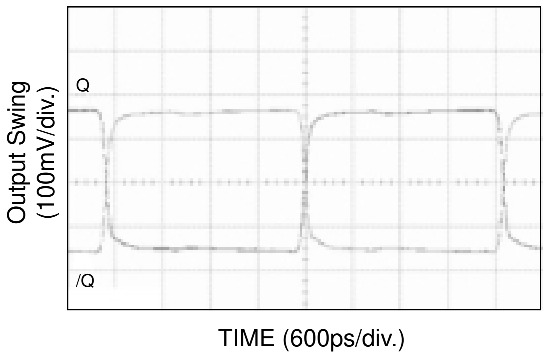
TRUTH TABLE

IN0	IN1	IN2	IN3	SEL0	SEL1	Q	/Q
0	X	X	X	0	0	0	1
1	X	X	X	0	0	1	0
X	0	X	X	1	0	0	1
X	1	X	X	1	0	1	0
X	X	0	X	0	1	0	1
X	X	1	X	0	1	1	0
X	X	X	0	1	1	0	1
X	X	X	1	1	1	1	0

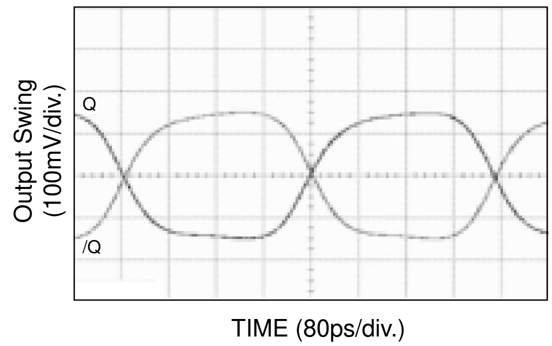
FUNCTIONAL CHARACTERISTICS

V_{CC} = 3.3V, GND = 0V, V_{IN} = 100mV, T_A = 25°C.

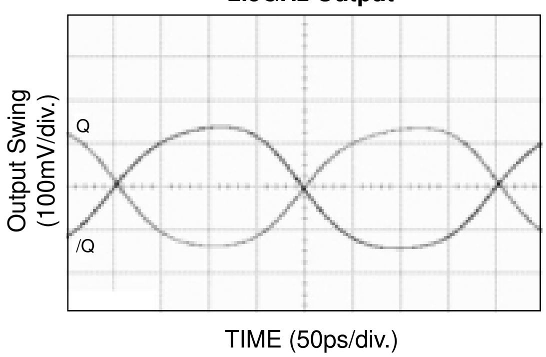
200MHz Output



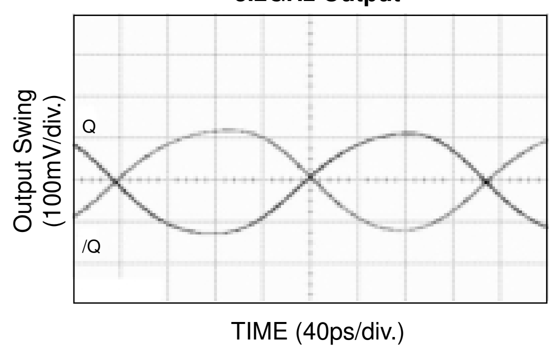
1.6GHz Output



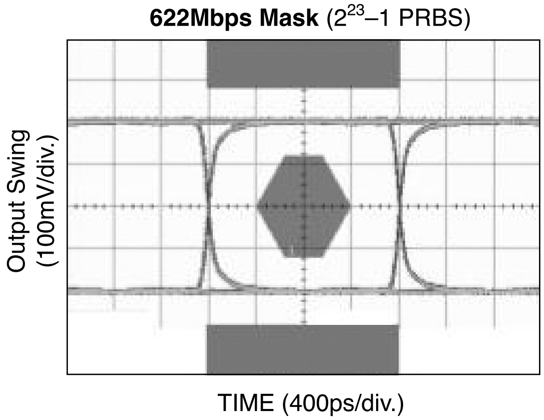
2.5GHz Output



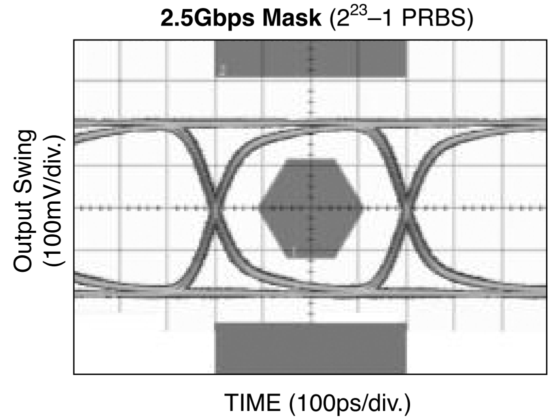
3.2GHz Output



622Mbps Mask (2^{23}–1 PRBS)



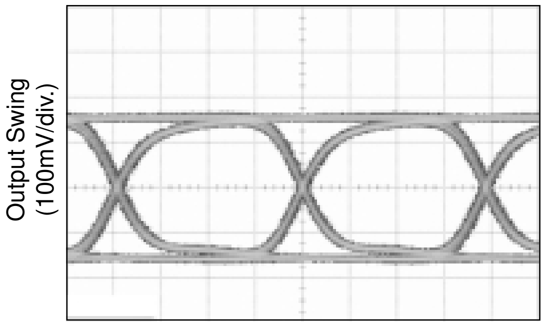
2.5Gbps Mask (2^{23}–1 PRBS)



FUNCTIONAL CHARACTERISTICS

V_{CC} = 3.3V, GND = 0V, V_{IN} = 100mV, T_A = 25°C.

3.2Gbps Data Output (2^{23}—1 PRBS)



INPUT AND OUTPUT STAGE INTERNAL TERMINATION

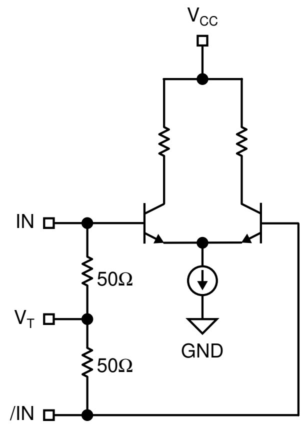


Figure 3. Simplified Differential Input Stage

INPUT INTERFACE APPLICATIONS

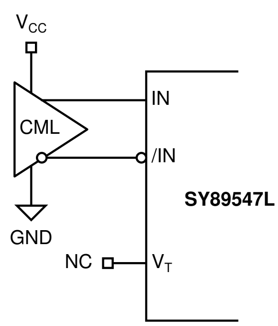


Figure 4a. CML Interface (DC-Coupled)

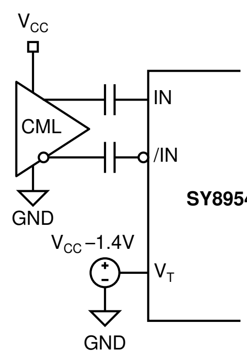


Figure 4b. CML Interface (AC-Coupled)

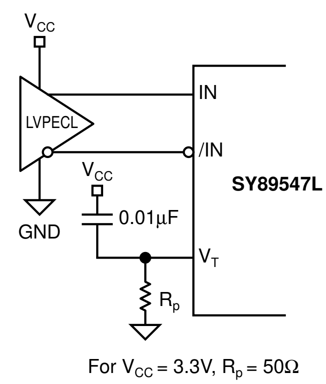


Figure 4c. LVPECL Interface (DC-Coupled)

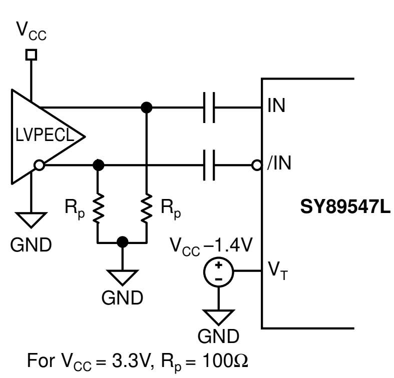


Figure 4d. LVPECL Interface (AC-Coupled)

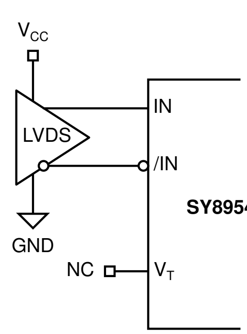


Figure 4e. LVDS Interface

OUTPUT INTERFACE APPLICATIONS

LVDS specifies a small swing of 350mV typical, on a nominal 1.25V common mode above ground. The common mode voltage has tight limits to permit large variations in ground between an LVDS driver and receiver. Also, change in common mode voltage, as a function of data input, is kept to a minimum, to keep EMI low.

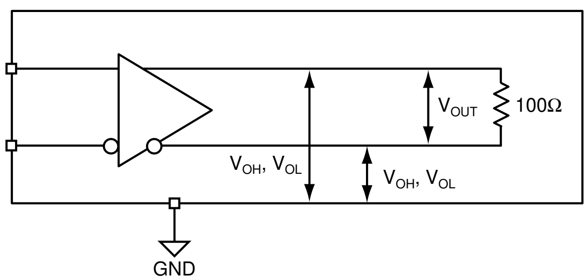


Figure 5a. LVDS Differential Measurement

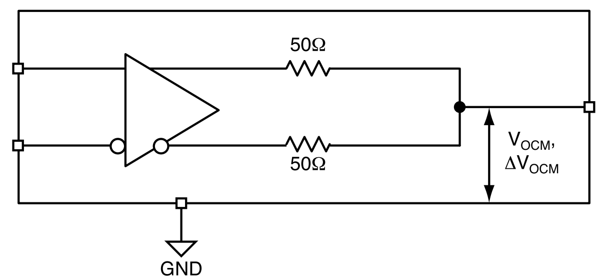
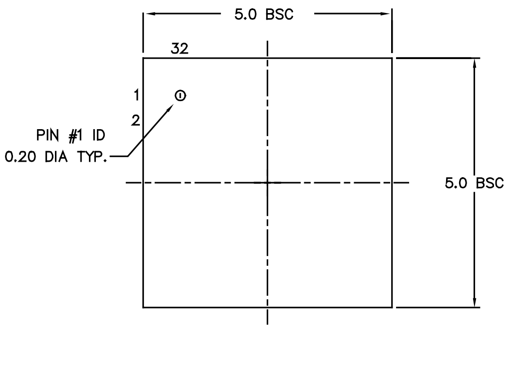


Figure 5b. LVDS Common Mode Measurement

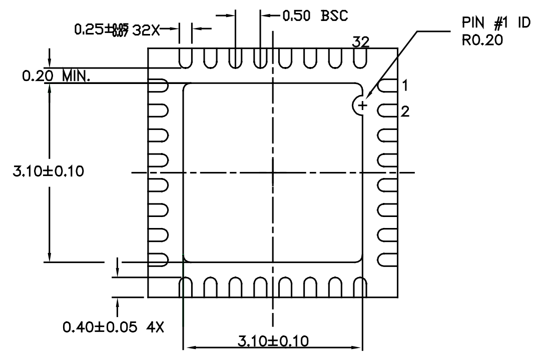
RELATED MICREL PRODUCTS AND SUPPORT DOCUMENTATION

Part Number	Function	Data Sheet Link
SY89542U	2.5 V, 3.2Gbps Dual, Differential 2:1 LVDS Multiplexer with Internal Input Termination	http://www.micrel.com/_PDF/HBW/sy89542u.pdf
SY89543L	3.3V, 3.2Gbps Dual, Differential 2:1 LVDS Multiplexer with Internal Input Termination	http://www.micrel.com/_PDF/HBW/sy89543l.pdf
SY89544U	2.5V, 3.2Gbps, Differential 4:1 LVDS Multiplexer with Internal Input Termination	http://www.micrel.com/_PDF/HBW/sy89544u.pdf
SY89545L	3.3V, 3.2Gbps 4:1 LVDS Multiplexer with Internal Input Termination	http://www.micrel.com/_PDF/HBW/sy89545l.pdf
SY89546U	2.5V, 3.2Gbps, Differential 4:1 LVDS Multiplexer with 1:2 Fanout and Internal Termination	http://www.micrel.com/_PDF/HBW/SY89546u.pdf
	MLF® Application Note	www.amkor.com/products/notes_papers/MLF_AppNote_0902.pdf
HBW Solutions	New Products and Applications	www.micrel.com/product-info/products/solutions.shtml

32-PIN *Micro*LeadFrame® (MLF-32)

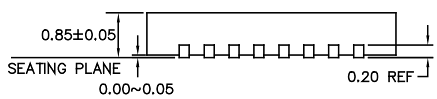


TOP VIEW

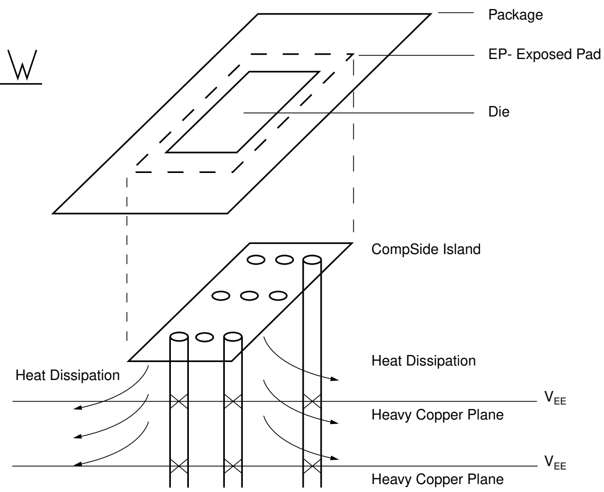


BOTTOM VIEW

NOTE:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. MAX. PACKAGE WARPAGE IS 0.05 mm.
3. MAXIMUM ALLOWABE BURRS IS 0.076 mm IN ALL DIRECTIONS.
4. PIN #1 ID ON TOP WILL BE LASER/INK MARKED.



SIDE VIEW



PCB Thermal Consideration for 32-Pin MLF® Package
(Always solder, or equivalent, the exposed pad to the PCB)

Package Notes:

1. Package meets Level 2 qualification.
2. All parts are dry-packaged before shipment.
3. Exposed pads must be soldered to a ground for proper thermal management.

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