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Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
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Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

SY89850U

Precision Low-Power LVPECL Line Driver/Receiver with Internal Termination

General Description

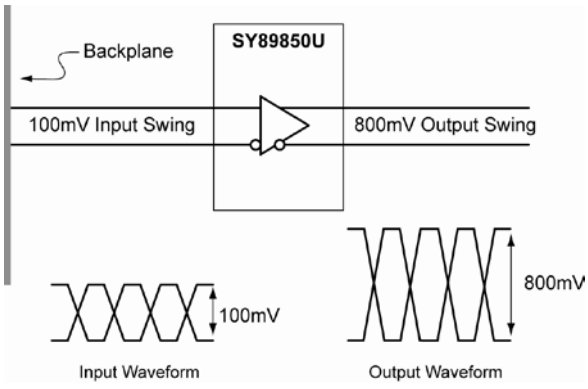
The SY89850U is a 2.5V/3.3V precision, high-speed, differential receiver capable of handling clocks up to 4GHz and data streams up to 3.2Gbps.

The differential input includes Micrel's unique, 3-pin input termination architecture that allows users to interface to any differential signal (AC or DC-coupled) as small as 100mV ($200mV_{PP}$) without any level shifting or termination resistor networks in the signal path. The outputs are 800mV LVPECL, with extremely fast rise/fall times guaranteed to be less than 160ps.

The SY89850U operates from a 2.5V ±5% supply or a 3.3V ±10% supply and is guaranteed over the full industrial temperature range of –40°C to +85°C. The SY89850U is part of Micrel's high-speed, Precision Edge® product line.

All support documentation can be found on Micrel's web site at www.micrel.com.

Typical Application



Precision Edge®

Features

- Guaranteed AC performance over temperature and supply voltage:
  - DC- to > 3.2Gbps data rate throughput
  - 4GHz clock f_{MAX} (typ.)
  - <280ps In-to-Out t_{pd}
  - <160ps t_r/t_f
- Low power: 50mW (2.5V typ.)
- Ultra-low jitter design:
  - $<1ps_{RMS}$ random jitter
  - $<10ps_{PP}$ deterministic jitter
  - $<10ps_{PP}$ total jitter (clock)
- Unique input termination and VT pin accepts DC- and AC-coupled inputs (CML, PECL, LVDS)
- Typical 800mV (100k) LVPECL Output Swing
- Power supply 2.5V ±5% or 3.3V ±10%
- Industrial temperature range –40°C to +85°C
- Available in ultra-small (2mm x 2mm) 8-pin DFN package

Applications

- Backplane buffering
- OC-12 to OC-192 SONET/SDN clock/data distribution
- All Gigabit Ethernet clock or data distribution
- Fibre Channel distribution

Markets

- LAN/WAN
- Enterprise servers
- ATE
- Test and measurement

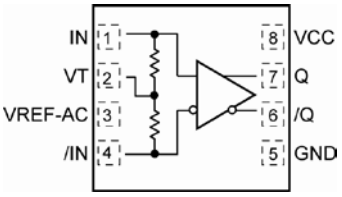
Ordering Information[1]

Part Number	Package Type	Operating Range	Package Marking	Lead Finish
SY89850UMG	DFN-8	Industrial	850U with Pb-Free bar-line indicator	NiPdAu Pb-Free
SY89850UMGTR[2]	DFN-8	Industrial	850U with Pb-Free bar-line indicator	NiPdAu Pb-Free

Notes:

1. Contact factory for dice availability. Dice are guaranteed at T_A = 25°C, DC Electrical Only.
2. Tape and Reel.

Pin Configuration



8-Pin DFN

Pin Description

Pin Number	Pin Name	Pin Function
1, 4	IN, /IN	Differential Input: This input pair is the signal to be buffered. These inputs accept AC- or DC-coupled signals as small as 100mV. Each pin of this pair internally terminates to a VT pin through 50Ω. Note that this input will default to an indeterminate state if left open. Please refer to the "Input Interface Applications" section for more details.
2	VT	Input Termination Center-Tap: Each side of the differential input pair terminates to this pin. The VT pin provides a center-tap to a termination network for maximum interface flexibility. See "Input Interface Applications" section for more details.
3	VREF-AC	Reference Output Voltage: This output biases to V_{CC} –1.2V. Connect to VT pin when AC-coupling the input. Bypass with 0.01µF low ESR capacitor to V_{CC}. Maximum sink/source current is ±1.5mA. Due to the limited drive capability, the VREF-AC pin is only intended to drive its respective VT pin. See "Input Interface Applications" section.
5	GND, Exposed Pad	Ground: Ground pin and exposed pad must be connected to the same ground plane.
7, 6	Q, /Q	Differential 100K LVPECL Output: This LVPECL output is the output of the device. Terminate through 50Ω to V_{CC}–2V. See "Output Interface Applications" section.
8	VCC	Positive Power Supply: Bypass with 0.1µF//0.01µF low ESR capacitors as close to the VCC pin as possible.

Absolute Maximum Ratings[1]

Supply Voltage (V_{CC}) ..... –0.5V to +4.0V
Input Voltage (V_{IN}) ..... –0.5V to V_{CC}
LVPECL Output Current (I_{OUT}) .....
  Continuous 50mA
  Surge 100mA
Input Current .....
  Source or sink current on IN, /IN ..... ±50mA
Termination Current .....
  Source or sink current on VT ..... ±100mA
Source or sink current on V_{REF-AC} ..... ±2mA
Lead Temperature (soldering, 20sec.) ..... 260°C
Storage Temperature (T_s) ..... –65°C to +150°C

Operating Ratings[2]

Supply Voltage (V_{CC}) ..... +2.375V to +2.625V
  ..... +3.0V to +3.6V
Ambient Temperature (T_A) ..... –40°C to +85°C
Package Thermal Resistance[3]
DFN (θ_{JA})
  Still-Air ..... 93°C/W
DFN (ψ_{JB})
  Junction-to-Board ..... 60°C/W

DC Electrical Characteristics[4]

T_A = –40°C to +85°C, unless noted.

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{CC}	Power Supply		2.375 3.0	2.5 3.3	2.625 3.6	V V
I_{CC}	Power Supply Current	No load, max. V_{CC}		20	30	mA
R_{DIFF_IN}	Differential Input Resistance (IN-to-/IN)		90	100	110	Ω
R_{IN}	Input Resistance (IN-to-V_T), (/IN-to-V_T)		45	50	55	Ω
V_{IH}	Input High Voltage (IN, /IN)	Note 5	V_{CC}–1.6		V_{CC}	V
V_{IL}	Input Low Voltage (IN, /IN)		0		V_{IH}–0.1	V
V_{IN}	Input Voltage Swing (IN, /IN)	See Figure 1a.	0.1		1.7	V
V_{DIFF_IN}	Differential Input Voltage Swing |IN–/IN|	See Figure 1b.	0.2			V
V_{T_IN}	In-to-V_T (IN, /IN)				1.28	V
V_{REF-AC}	Output Reference Voltage		V_{CC}–1.3	V_{CC}–1.2	V_{CC}–1.1	V

Notes:

1. Permanent device damage may occur if Absolute Maximum Ratings are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. The data sheet limits are not guaranteed if the device is operated beyond the operating ratings.
3. Package Thermal Resistance assumes exposed pad is soldered (or equivalent) to the devices most negative potential on the PCB.
4. The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.
5. V_{IH} (min) not lower than 1.2V.

LVPECL Output DC Electrical Characteristics[6]

V_{CC} = +2.5V ±5% or +3.3V ±10%; T_A = –40°C to +85°C; R_L = 50Ω to V_{CC} –2V, unless otherwise stated.

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{CC}	Output High Voltage Q, /Q		V_{CC} –1.145		V_{CC} –0.895	V
V_{OL}	Output Low Voltage Q, /Q		V_{CC} –1.945		V_{CC} –1.695	V
V_{OUT}	Output Voltage Swing Q, /Q	See Figure 1a.	550	800		mV
V_{DIFF_OUT}	Differential Output Voltage Swing Q, /Q	See Figure 1b.	1100	1600		mV

Note:

6. The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.

AC Electrical Characteristics[7]

V_{CC} = +2.5V ±5% or +3.3V ±10%; T_A = –40°C to +85°C; R_L = 50Ω to V_{CC} –2V, unless otherwise stated.

Symbol	Parameter	Condition	Min	Typ	Max	Units
f_{MAX}	Maximum Operating Frequency	NRZ Data	3.2			Gbps
		V_{OUT} ≥ 400mV Clock		4		GHz
t_{pd}	Propagation Delay IN-to-Q	V_{IN} ≥ 100mV	180	260	360	ps
t_{pd} Tempco	Differential Propagation Delay Temperature Coefficient			115		fs/°C
t_{JITTER}	Data Random Jitter (RJ)	Note 8			1	ps_{RMS}
	Deterministic Jitter (DJ)	Note 9			10	ps_{PP}
	Clock Cycle-to-Cycle Jitter	Note 10			1	ps_{RMS}
	Total Jitter (TJ)	Note 11			10	ps_{PP}
t_r, t_f	Rise/Fall Time (20% to 80%) Q, /Q	At full output swing.	50	100	160	ps

Notes:

7. The circuit is designed to meet the AC specifications shown in the above table after thermal equilibrium has been established.
8. Random jitter is measured with a K28.7 comma detect character pattern, measured at 2.5Gbps and 3.2Gbps.
9. Deterministic jitter is measured at 2.5Gbps and 3.2Gbps, with both K28.5 and 2^{23}–1 PRBS pattern.
10. Cycle-to-cycle jitter definition: the variation of periods between adjacent cycles, $T_n - T_{n-1}$ where T is the time between rising edges of the output signal.
11. Total jitter definition: with an ideal clock input of frequency < f_{MAX}, no more than one output edge in 10^{12} output edges will deviate by more than the specified peak-to-peak jitter value.

Single-Ended and Differential Swings

Figure 1a. Singled-Ended Voltage Swing

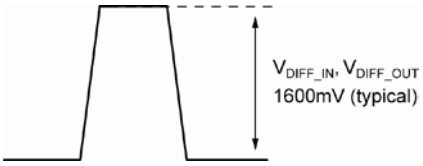
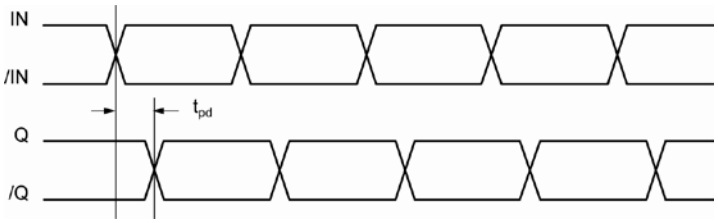


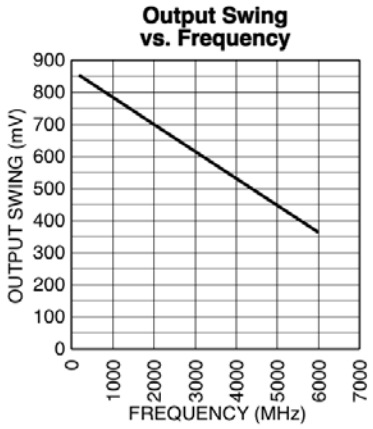
Figure 1b. Differential Voltage Swing

Timing Diagram



Typical Operating Characteristics

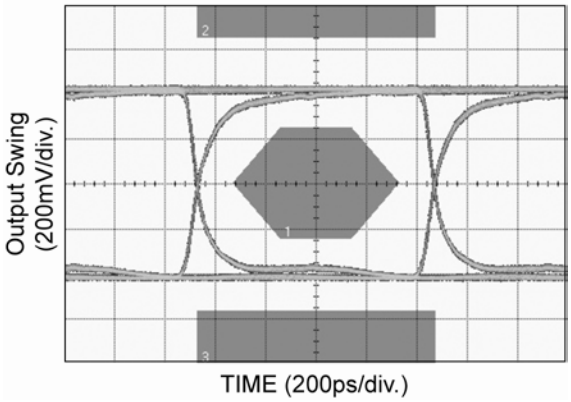
V_{CC} = 3.3V, GND = 0V, V_{IN} = ≥ 400mV$_{pp}$, t_r/t_f ≤ 300ps, T_A = 25°C, unless otherwise stated.



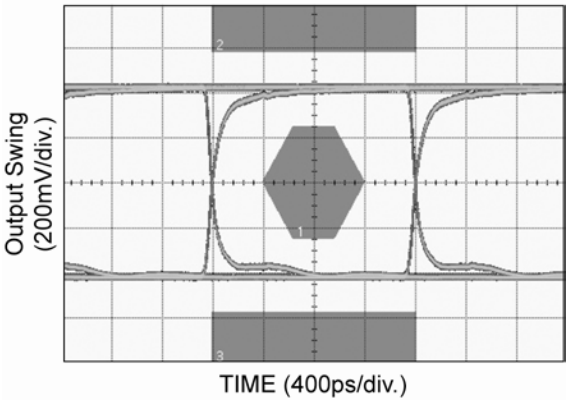
Functional Characteristics

V_{CC} = 3.3V, GND = 0V, V_{IN} = ≥ 400mV$_{pp}$, t_r/t_f ≤ 300ps, T_A = 25°C, unless otherwise stated.

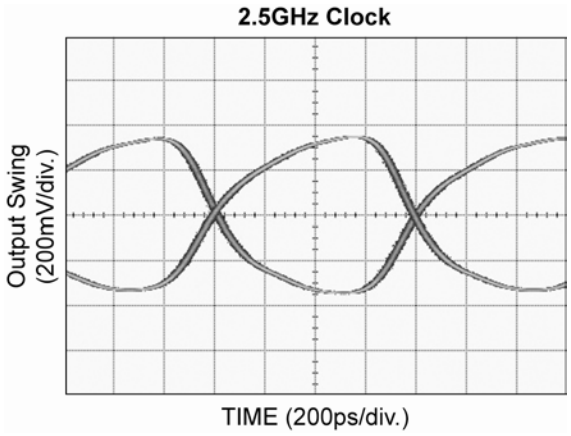
1xFC Mask 2^{23}-1 PRBS



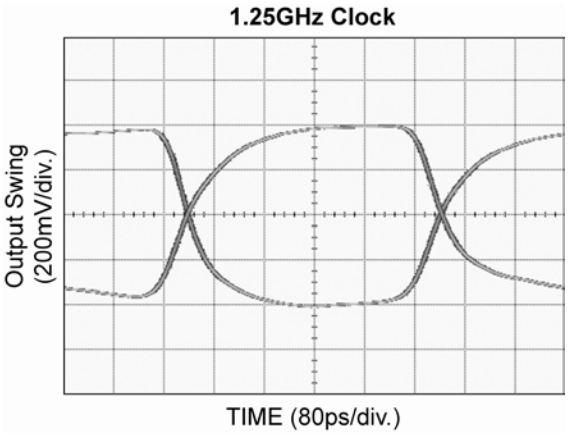
OC-12 Mask 2^{23}-1 PRBS



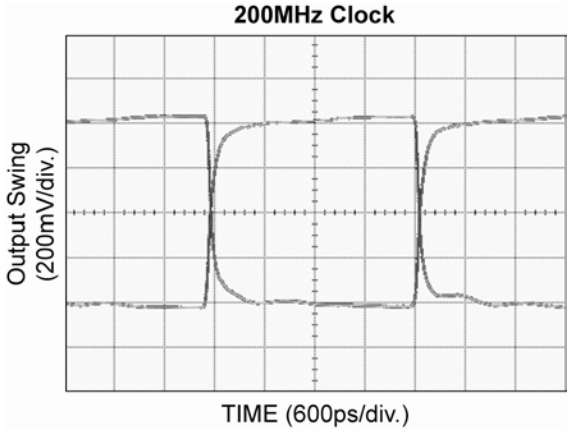
2.5GHz Clock



1.25GHz Clock



200MHz Clock



Input and Output Stages

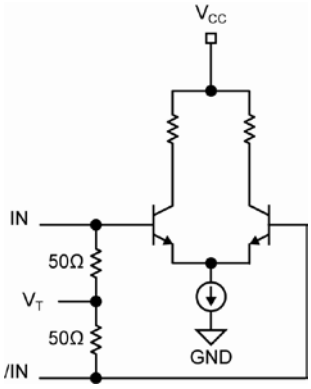


Figure 2a. Simplified Differential Input Stage

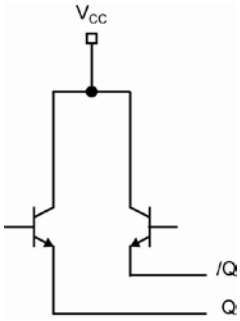


Figure 2b. Simplified LVPECL Output Stage

Input Interface Applications

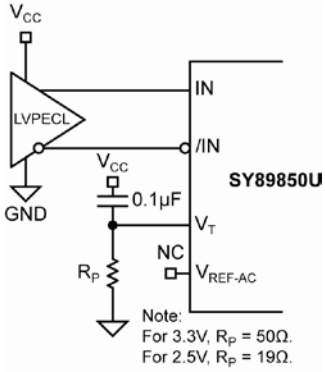


Figure 3a. LVPECL Interface (DC-Coupled)

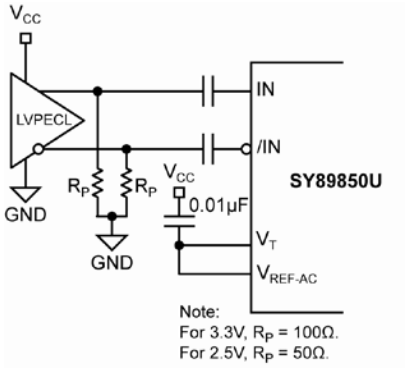
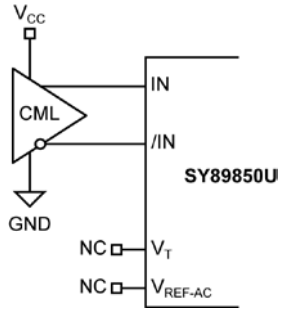


Figure 3b. LVPECL Interface (AC-Coupled)



Option: may connect V_T to V_{CC}

Figure 3c. CML Interface (DC-Coupled)

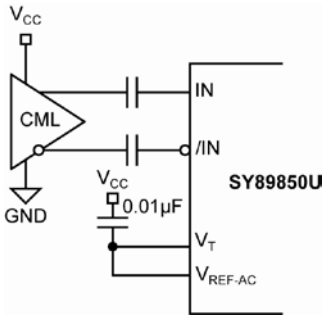


Figure 3d. CML Interface (AC-Coupled)

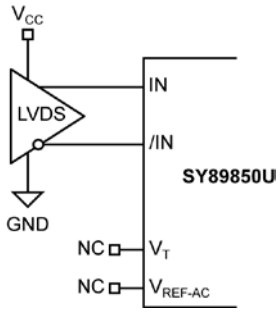
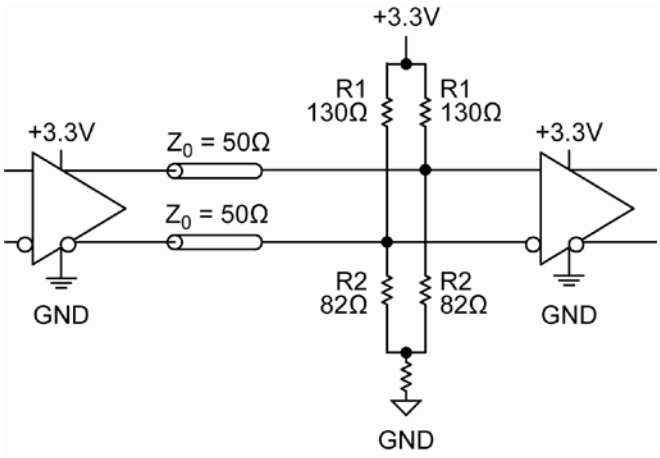


Figure 3e. LVDS Interface (DC-Coupled)

Output Interface Applications

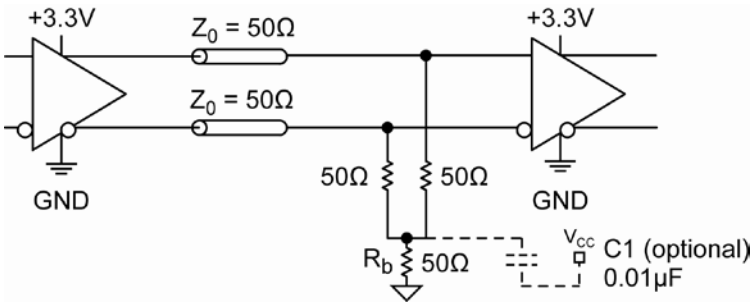
LVPECL has a high input impedance, a very low output impedance (open emitter), and a small signal swing which results in low EMI. LVPECL is ideal for driving 50Ω and 100Ω controlled impedance transmission lines. There are several techniques for terminating the LVPECL output: Parallel Termination-Thevenin Equivalent, Parallel Termination (3-resistor), and AC-coupled Termination. Unused output pairs may be left floating. However, single-ended outputs must be terminated, or balanced.



Note:

1. For +2.5V systems, R1 = 250Ω, R2 = 62.5Ω.

Figure 4a. Parallel Termination-Thevenin Equivalent



Notes:

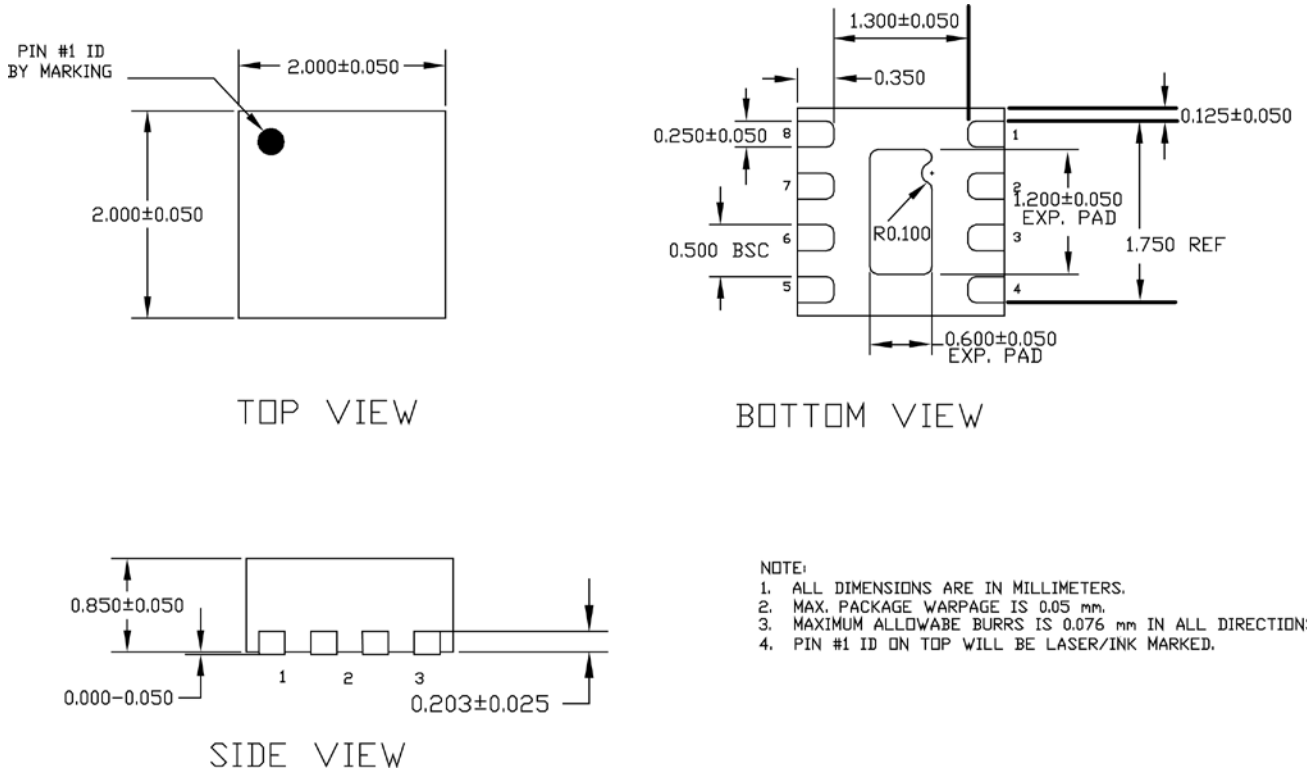
1. Power-saving alternative to Thevenin termination.
2. Place termination resistors as close to destination inputs as possible.
3. R_b resistor sets the DC bias voltage, equal to V_T.
4. For 2.5V systems, R_b = 19Ω.

Figure 4b. Parallel Termination (3-Resistor)

Related Product and Support Documentation

Part Number	Function	Data Sheet Link
SY58601U	Ultra-Precision Differential 800mV LVPECL Line Driver/Receiver with Internal Termination	www.micrel.com/product-info/products/sy58601u.shtml
HBW Solutions	New Products and Applications	www.micrel.com/product-info/products/solutions.shtml

Package Information



8-Pin Ultra-Small EPAD DFN

MICREL, INC. 2180 FORTUNE DRIVE SAN JOSE, CA 95131 USA
TEL +1 (408) 944-0800 FAX +1 (408) 474-1000 WEB http:/www.micrel.com