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# User's Manual

## SYG-70CP



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# 1 SYG-70CP Overview

## 1.1 Introduction

The Future Designs, Inc.  $\Sigma$ yG™ (pronounced “sig”) Family provides a complete and qualified Graphical User Interface (GUI) / Human Machine Interface (HMI) platform for the rapid release of customer products. The core of  $\Sigma$ yG is Renesas Synergy™ – a comprehensive and integrated software-based microcontroller platform. FDI adds the Synergy platform to its GUI hardware, systems, and production expertise. The result is a sum of high-quality products that provide a robust and proven source for GUI and HMI solutions:

$$\Sigma\text{yG} = \text{Renesas Synergy} + \text{GUI}$$

## 1.2 ESD Warning

The SYG-70CP is shipped in a protective anti-static package. Do not subject the module to high electrostatic potentials. Exposure to high electrostatic potentials may cause damage to the boards that will not be covered under warranty. General practice for working with static sensitive devices should be followed when working with the kit.



### 1.3 SYG-70CP Block Diagram

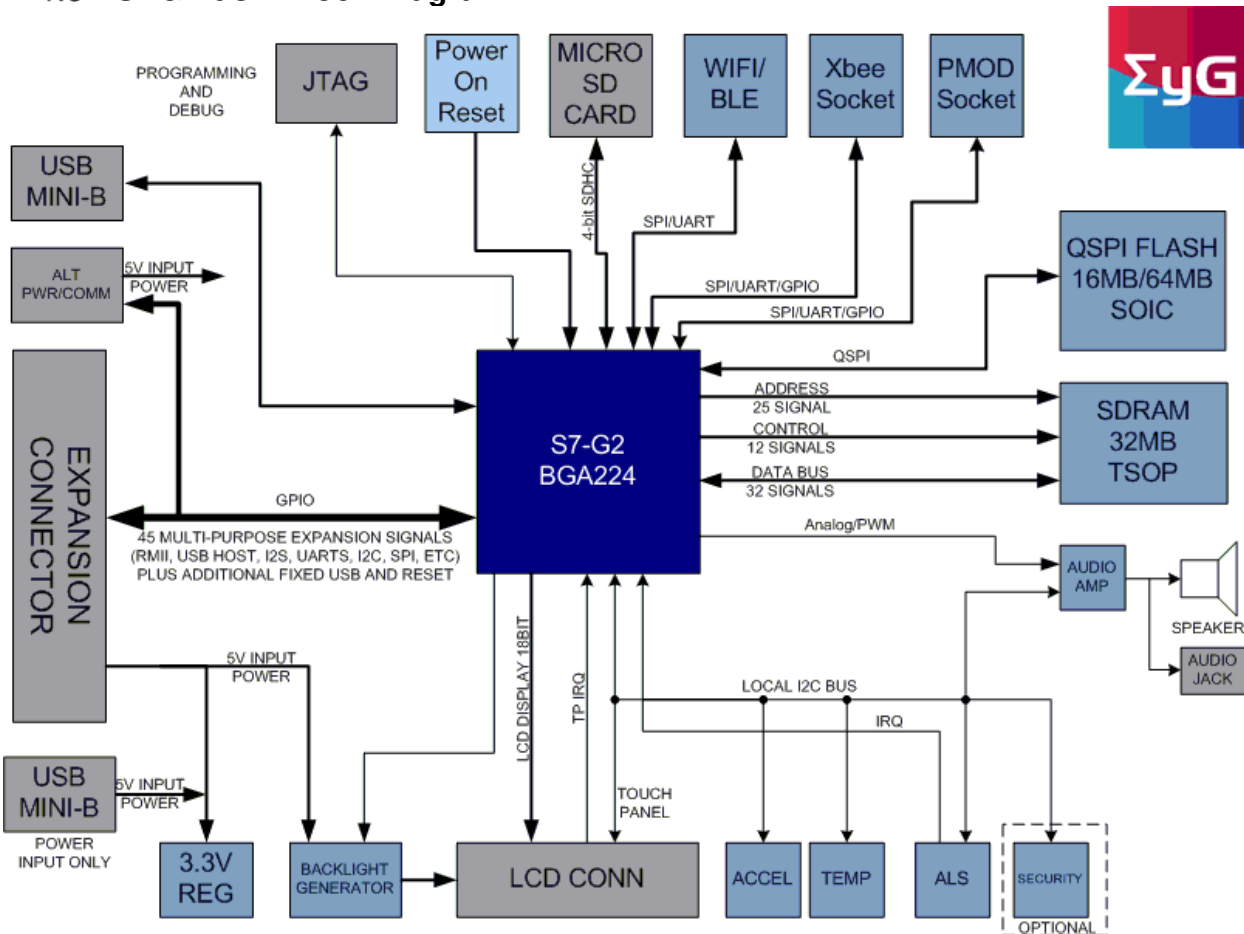


Figure 1 - SYG-70CP Block Diagram





Board Layout

1.4 Component Layout

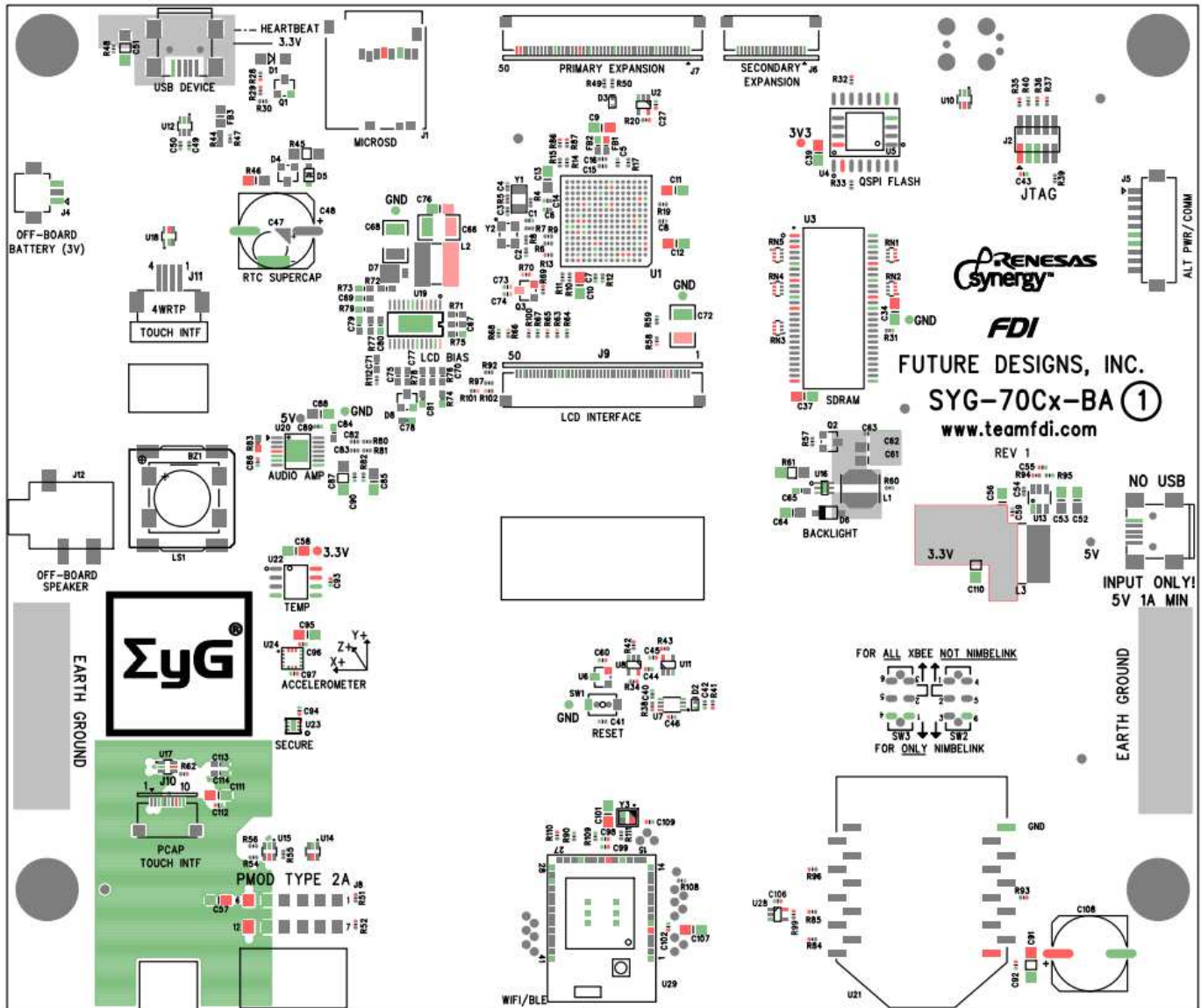


Figure 2 - Component Layer (Top)



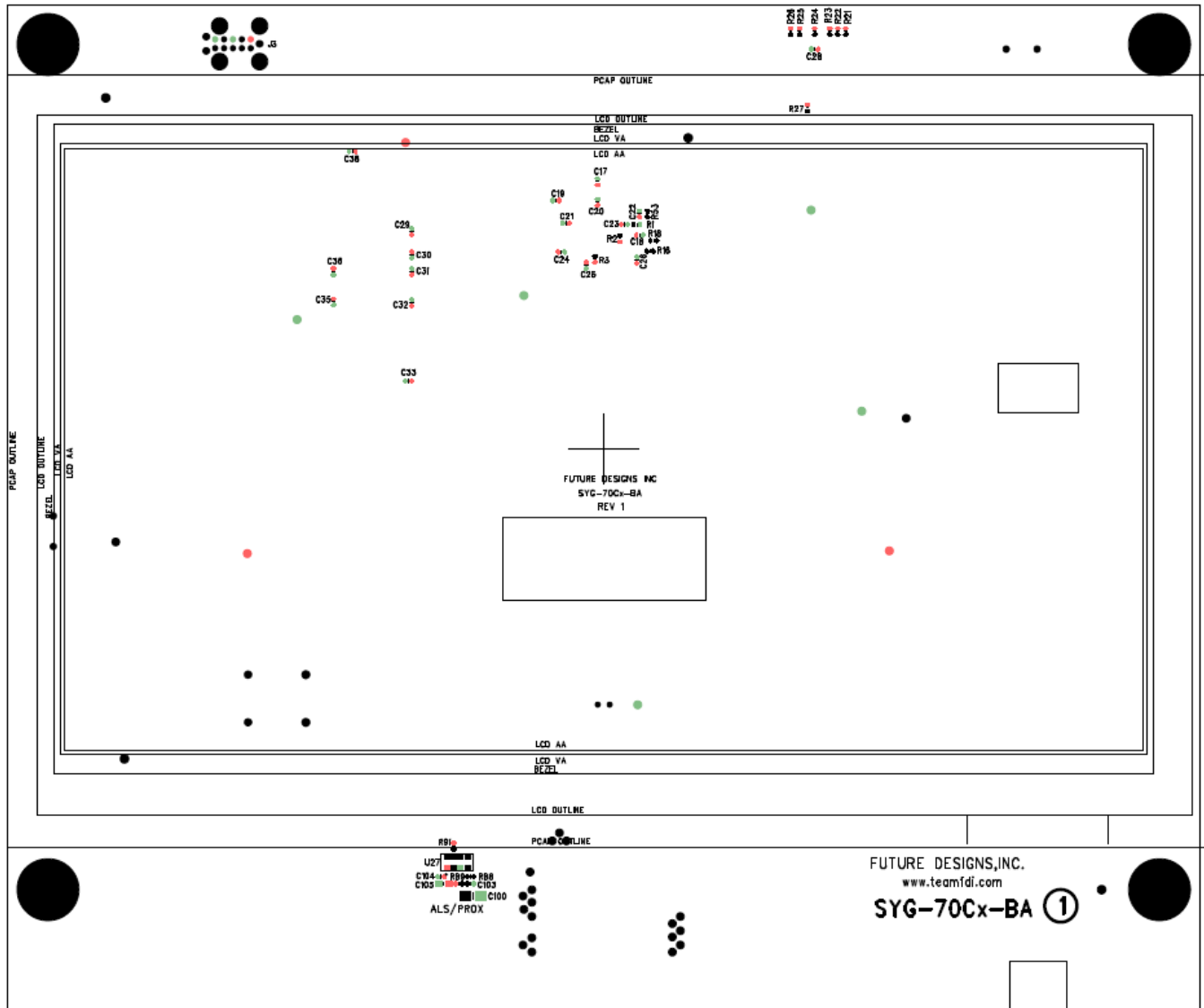


Figure 3 – Component Layer (Bottom)



### 1.5 Board Dimensions

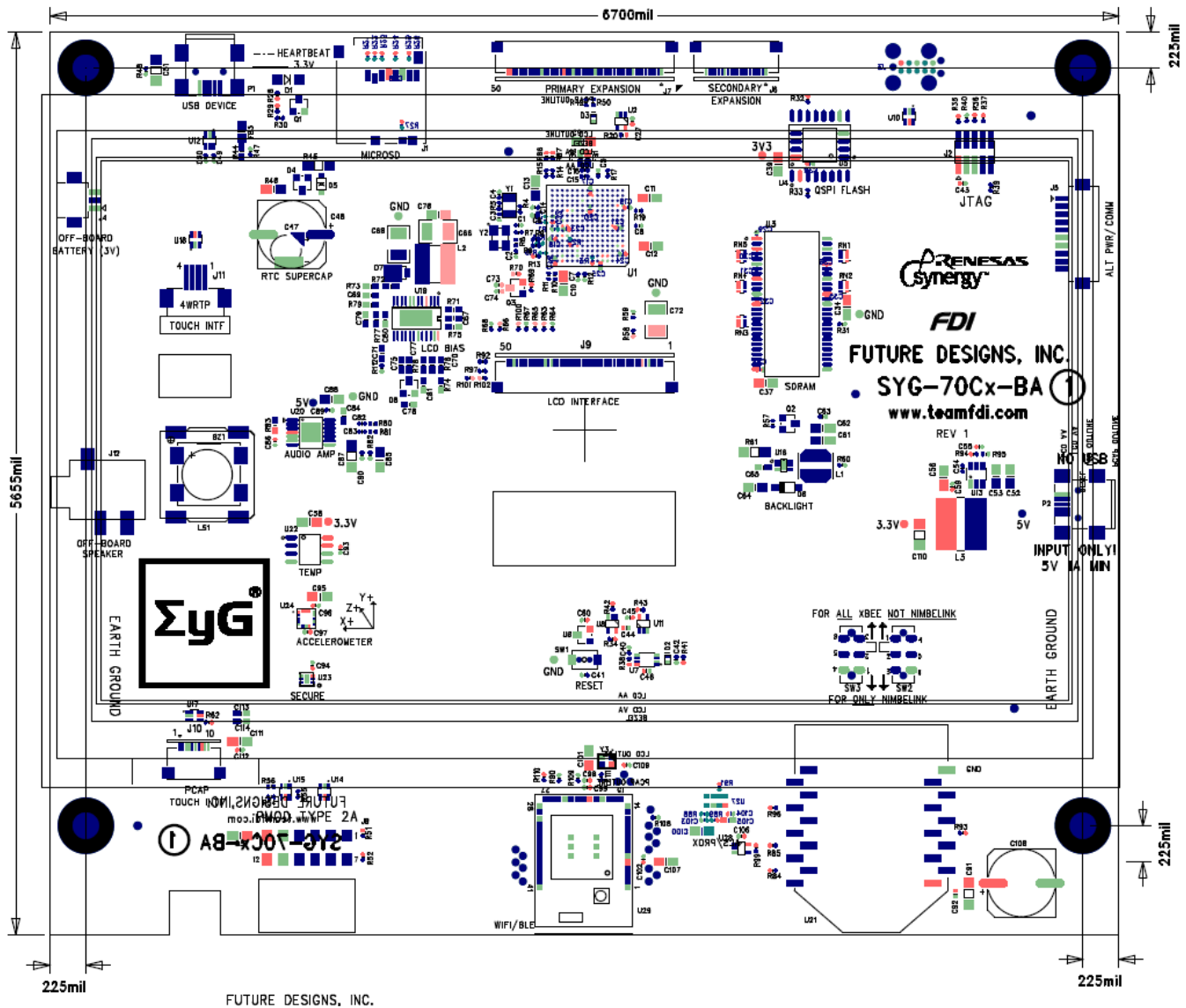


Figure 4- Board Dimensions

**Note: Mounting holes are .167" in diameter and are not threaded, but do provide Earth Ground**

Not Pictured: SYG-70CP Total Height – 822 mil, Height off PCB – 319 mil



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## 2 Input Power Sources

The SYG-70CP can be powered multiple ways depending on your requirements. The various power input methods are described below.

**Input power requirements are 5V  $\pm$ 5%, 1 A minimum.**

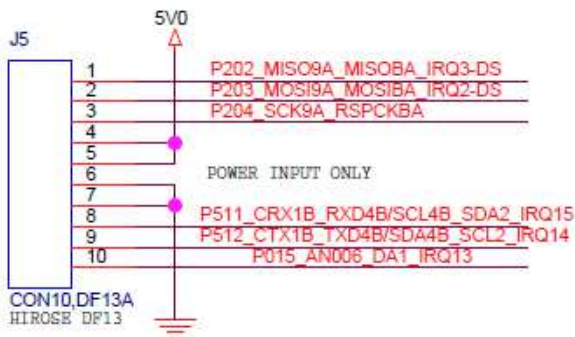
### 2.1 5V input via USB Mini-B (P2)

The most convenient power source available to the SYG-70CP is the USB Mini-B connector. This connector is labeled "NO USB" "INPUT ONLY! 5V 1A MIN" so that it cannot be confused with the USB Mini-B Device port. No data is sent over this cable, it is strictly for powering the SYG-70CP.



### 2.2 Alternate Power Connection (J5)

The alternate power connector comes in the form of the DF13A-10P-1.25H connector. This connector accepts the DF13-10S-1.25C socket connector. Pins 4 and 5 accept 5V and pins 6 and 7 accept Ground. The remaining lines are for use with COMMs and will be described in the peripheral section of this manual.



### ALTERNATE POWER & COMM INTERFACE

### 2.3 Power Requirements

## 2.4 USB Power (P2)

---

**Rating: +5VDC  $\pm$ 5%, 1A Minimum Input**

---

+5VDC  $\pm$ 5% is the input power range specification. The +5VDC output level to either the Expansion Board connector or the 5V devices may be affected if the +5VDC input power is not within specifications.

For reference on the USB output port from the  $\mu$ EZ GUI, the following are the specifications:

- USB High Power Specifications are 500mA maximum, and 4.75V to 5.25V standard.
- USB Low Power Specifications are 100mA maximum, and 4.4V to 5.25V standard.

## 2.5 70-pin Expansion Connectors (J6 & J7)

---

**Rating: +5VDC  $\pm$ 5%, 300mA Maximum Output (1A Minimum if Input)**

---

The SYG-70CP can provide a maximum of 300mA of 3.3V power for “external use” over the expansion connectors J7 (50 pin) and J6 (20 pin).

If more than 300mA of 3.3V is needed for an expansion board:

- Then the primary power input (i.e. 5V) should be located on the expansion board rather than on the SYG-70CP
- The expansion board should include its own 3.3V voltage regulator
- Ensure the 3.3V voltage rails of the SYG-70CP & Expansion Board are not connected.
- The SYG-70CP should be powered using 5V from the expansion board over the 70-pin breakout, instead of powering the expansion board from the SYG-70CP USB connector.

More information on this connector can be found in the [Expansion Connectors](#) section of this document.



## 2.6 Alternate Power & Communication Interface Connector (J5)

---

**Rating: +5VDC ±5%, 1A Minimum Input, 2A Maximum Input**

---

Alternate Power/Communication Interface Connector, J7, is a great alternative to bringing external power onto the SYG-70CP in cases where the onboard power regulator isn't sufficient.

More information on this connector can be found in the [10 Pin Alternate Power & Comm Interface](#) section of this document.

**Note: This is a Power Input only connector. Do not use this connector to power an external device.**





### 3 Renesas Synergy S7G2 Microcontroller

The microcontroller unit (MCU) on the SYG-70CP is a 32-bit, 240 MHz, Cortex® M4 processor with 4 MB of internal flash and 640 KB of SRAM. MCUs from the Synergy family include qualified commercial-grade software to enable rapid development of applications which require a real-time operating system. The Synergy Software Package (SSP) integrates the full suite of Express Logic® software including the ThreadX RTOS and suite of X-Ware stacks. For more information on Express Logic software, see [www.rtos.com](http://www.rtos.com).



## 4 Development Tools

To develop applications for the SYG-70CP, it is highly recommended to use one of the two development environments provided with purchase of the SYG-70CP. All the available development software is available on the Renesas Synergy Gallery website and includes:

### 4.1 e2 studio

- The Renesas Synergy™ Platform's Eclipse-based e2 studio Integrated Solution Development Environment (ISDE) is your workbench, providing you all the tools you need to create differentiated applications for Synergy MCU devices.
- An open tool platform, the Eclipse CDT (C/C++ Development Tooling) standard allows plug-ins for many innovative tool functions. Renesas engineers created solution-based plug-ins for Synergy that guide the design process in three intuitive phases covering Synergy MCUs and software – the Preparation Phase, the Build Phase, and the Debug Phase.

### 4.2 IAR Embedded Workbench® for Synergy

- IAR Embedded Workbench, the world's most widely used embedded development environment, is now completely integrated with the Renesas Synergy™ Platform. The new product IAR EW for Synergy provides add-on functionality to simplify and accelerate software development, and provide the best performance and smallest code size. Renesas created the Synergy Standalone Configurator (SSC) which is available to IAR EW for Synergy users as a separate download. The SSC includes the Synergy Project Generator as well as the Synergy Project Editor, including configurators like the Clock Configurator, Pin Configurator, RTOS Configurator, and SSP Module Selector/Configurator.

### 4.3 Synergy Software Package (SSP)

- Part of the Renesas Synergy™ Platform, the Synergy Software Package (SSP) features software that has been integrated, optimized, tested, and qualified by Renesas for Synergy users – and is also maintained and warranted by Renesas on an ongoing basis.
- The SSP includes the ThreadX® real-time operating system (RTOS), the X-Ware™ suite of stacks and middleware (NetX™, NetX Duo™, USBX™, GUIX™, FileX®) plus other quality stacks, libraries, and drivers all connected by a rich Application Framework for ease of use. A common robust API resides over these components enabling you to focus on your own product application code without delays

### 4.4 TraceX®

- TraceX® is Express Logic's host-based analysis tool that provides developers with a graphical view of real-time system events and enables them to visualize and better understand the behavior of their real-time systems. With TraceX, developers can see clearly the occurrence of system events like interrupts and context switches that occur out of view of standard debugging tools. The ability to identify and study these events, and to pinpoint the timing of their occurrence in the context of the overall system's operation enables developers to resolve programming problems by finding unexpected behavior and letting them investigate specific areas further.



#### 4.5 GUIX Studio™

- GUIX Studio™ provides a complete WYSIWYG screen design environment which allows the user to drag-and-drop graphical elements used to build the UI screens. GUIX Studio automatically generates C code compatible with the GUIX™ library, ready to be compiled and run on the target. Developers can produce pre-rendered fonts for use within an application using the integrated GUIX Studio font generation tool. Fonts can be generated in monochrome or anti-aliased formats, and are optimized to save space on the target. Fonts can include any set of characters, including Unicode characters for multi-lingual applications.

#### 4.6 Renesas Verified Software Add-Ons

- A selection of specialty software components developed, licensed, and serviced by Renesas VSA partner companies
- Tested and verified by Renesas to be compatible with the SSP per Renesas SSP interoperability requirements
- Continuously tested for SSP interoperability with each new SSP maintenance release
- Free evaluation version available, full licensing required from the VSA partner company for end-product production

#### 4.7 Renesas Qualified Software Add-Ons

- A selection of specialty software components, licensed and serviced directly by Renesas
- Developed under the same quality standards and guidelines as the SSP
- Tightly integrated and optimized for use with SSP and API structure
- Free evaluation version available, full licensing required from Renesas for end-product production



## 5 Board Support Package (BSP)

To allow users to begin application development quickly, a Board Support Package has been developed to pre-configure the S7G2 MCU's pins to support the various peripherals on board the SYG-70CP. This allows you to focus on application development instead of spending hours tracing signals through schematics. To install the BSP, download the ".pack" file from the TeamFDI website using the link below. This file can also be found by navigating to the SYG-70CP product page under the software tab:

[http://www.teamfdi.com/wp-content/uploads/SYG-70CP\\_Pack.zip](http://www.teamfdi.com/wp-content/uploads/SYG-70CP_Pack.zip)

**Note: Clicking this link on a PC will start a download**

Once you have the file, ensure e2studio or IAR is closed and copy the file into the **Packs** directory of your e2studio or SSC directory.

If you installed e2studio into its default directory, this folder will be located at:

**C:\Renesas\e2\_studio\internal\projectgen\arm\Packs**

If you use IAR Embedded Workbench with SSC, and installed it into its default directory, it will be located at:

**C:\Renesas\Synergy\SSC\internal\projectgen\arm\Packs**

**Note: If you use both IAR and e2studio, you must install the pack in BOTH locations.**

Once the \*.pack file has been placed into the directory, open e2studio or IAR and either development environment's **New Synergy C Project** wizard will be updated to include the SYG-70CP as a new board option to select.



## 6 Memory

### 6.1 32 MB External SDRAM

The 32MB 16Mbx16 SDRAM is a high-speed CMOS, dynamic random-access memory in an industry standard 54 ball VFBGA package. It is internally configured as a quad-bank DRAM with a synchronous interface (all signals are registered on the positive edge of the clock signal, CLK). Each of the x16's 67,108,864-bit banks are organized as 8192 rows by 512 columns by 16 bits. The 256Mb SDRAM uses an internal pipelined architecture to achieve high-speed operation. This architecture is compatible with the 2n rule of prefetch architectures, but it also allows the column address to be changed on every clock cycle to achieve a highspeed, fully random access. The 256Mb SDRAM is designed to operate in 3.3V memory systems. An auto refresh mode is provided, along with a power-saving, power-down mode. All inputs and outputs are LVTTTL-compatible.

SDRAMs offer substantial advances in DRAM operating performance, including the ability to synchronously burst data at a high data rate with automatic column-address generation, the ability to interleave between internal banks to hide pre-charge time, and the capability to randomly change column addresses on each clock cycle during a burst access.

Micron is a longtime leader in the SDRAM space, offering solutions from 64Mb to 256Mb, as well as a full suite of simulation models and technical support. The MT48LC16M16A2P-6AIT:G is supported on a cost effective 50nm process technology, with assured lifecycle support for years to come.

For more technical information visit <http://www.micron.com/>

This memory is accessed through the S7G2 microcontroller (MCU) External Memory Interface peripheral which is pre-configured on projects created using the provided Board Support Package (BSP).



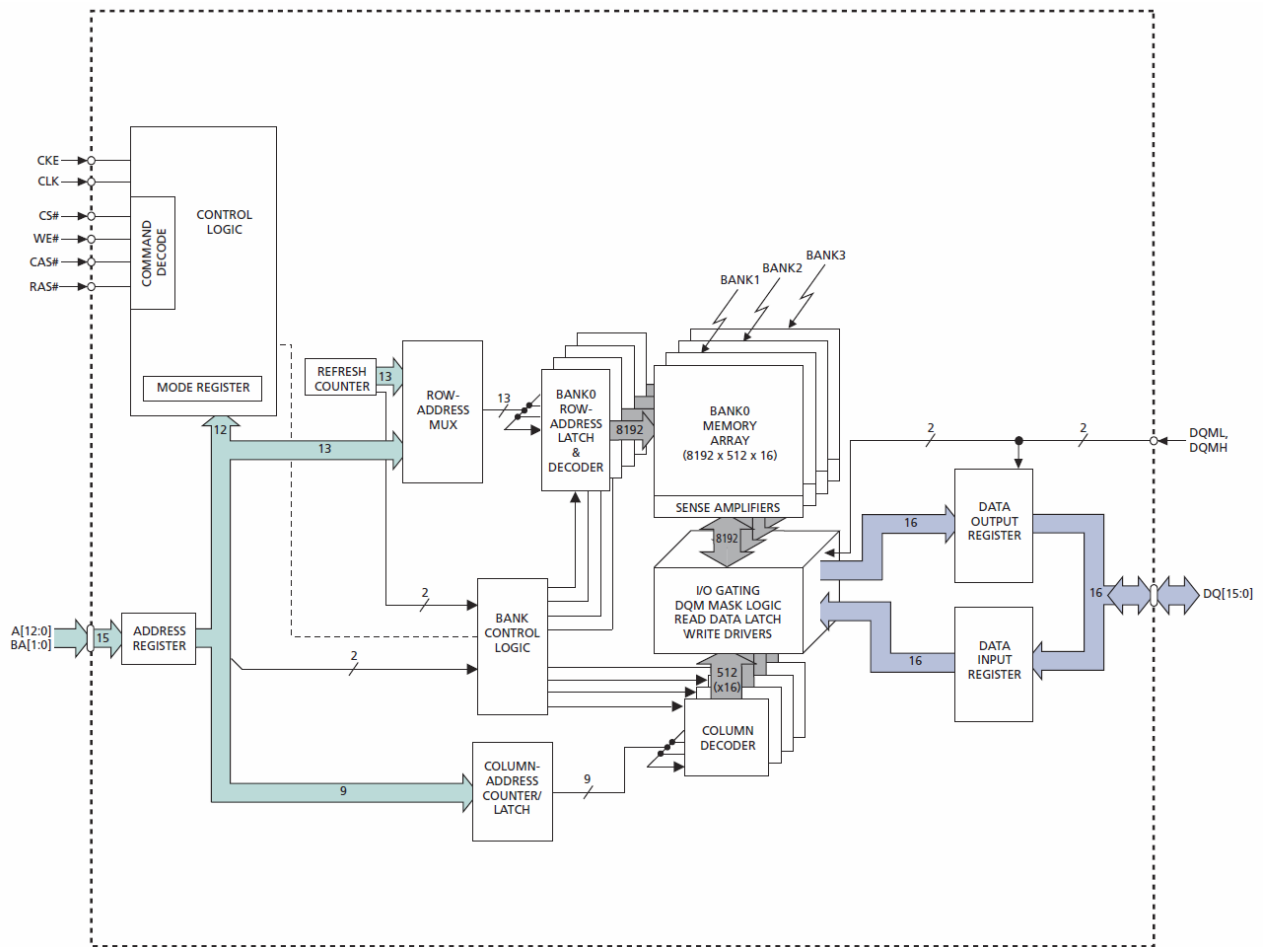


Figure 5 - SDRAM Block Diagram





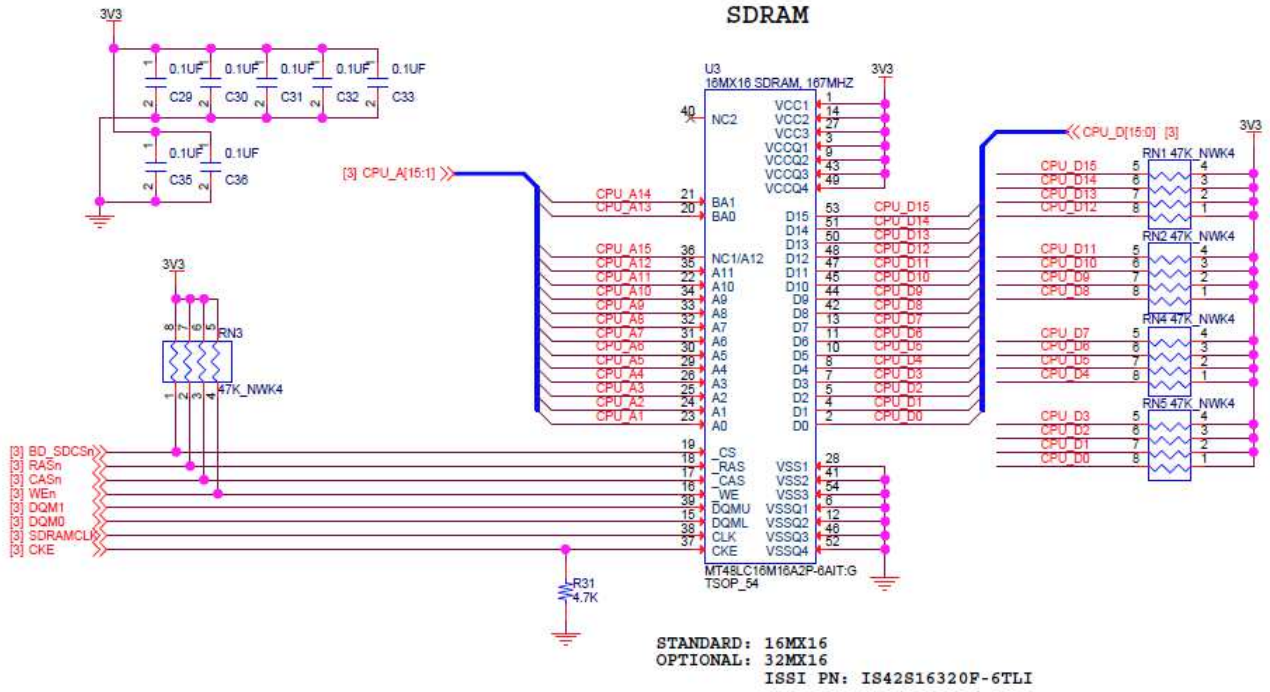


Figure 6 - SDRAM Schematic



Pin Configuration		Pin Configuration	
Module name:	BUS0	A03:	✓ P113
Operation Mode:	SDRAM 16bit	A04:	✓ P112
<b>Input/Output</b>		A05:	✓ P111
BCLK_SDCLK:	✓ P602	A06:	✓ P301
RD:	None	A07:	✓ P302
WR_WR0_DQM0:	✓ P601	A08:	✓ P303
WR1_BC1:	None	A09:	✓ P304
SDCS:	✓ P611	A10:	✓ P305
CS0_WE:	✓ P610	A11:	✓ P306
CS1_CKE:	✓ P609	A12:	✓ P307
CS2_RAS:	✓ P311	A13:	✓ P308
CS3_CAS:	✓ P312	A14:	✓ P309
CS4:	None	A15:	✓ P310
CS5:	None	A16:	None
CS6:	None	A17:	None
CS7:	None	A18:	None
A00_BC0_DQM1:	✓ P608	A19:	None
A01:	✓ P115	A20:	None
A02:	✓ P114	A21:	None
A22:	None		
A23:	None	D8_DQ8:	✓ P612
D0_DQ0:	✓ P100	D9_DQ9:	✓ P613
D1_DQ1:	✓ P101	D10_DQ10:	✓ P614
D2_DQ2:	✓ P102	D11_DQ11:	✓ P605
D3_DQ3:	✓ P103	D12_DQ12:	✓ P604
D4_DQ4:	✓ P104	D13_DQ13:	✓ P603
D5_DQ5:	✓ P105	D14_DQ14:	✓ P800
D6_DQ6:	✓ P106	D15_DQ15:	✓ P801
D7_DQ7:	✓ P107	WAIT:	None

Figure 7 - Synergy SDRAM Pin Configuration

## 6.2 16MB QSPI Flash, MX25L12835FMI-10G



Macronix Serial Multi I/O (MXSMIO™) Flash provides not only Single I/O, but also Multi-I/O interfaces. MX66xxx35 or MX25xxx33/35/39/73/75 series offering Dual I/O or Quad I/O operations which double or quadruple the read performance of systems for high-end consumer applications.

The QSPI Flash provides additional Code Space if needed, but also provides storage for fonts and images (which can be large on WVGA displays such as this one).

This memory is accessed through the S7G2 MCU's dedicated QSPI0 peripheral port.

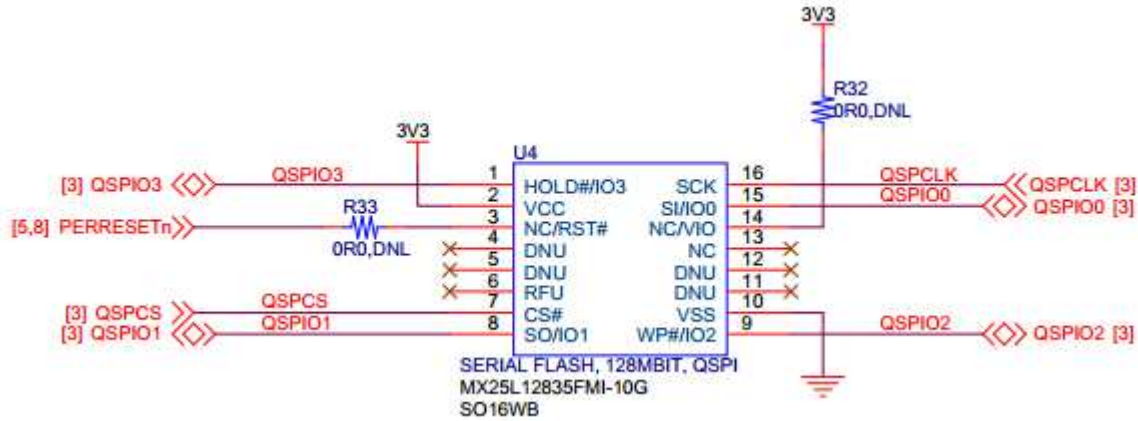


Figure 8 – QSPI Flash Pin Connections

Module name:	QSPI0
Usage:	For QSPI, same Pin Group Recommended
Pin Group Selection:	<input type="text" value="_A only"/>
Operation Mode:	<input type="text" value="Quad"/>
<b>Input/Output</b>	
QSPCLK:	<input checked="" type="checkbox"/> P500
QSSL:	<input checked="" type="checkbox"/> P501
QIO0:	<input checked="" type="checkbox"/> P502
QIO1:	<input checked="" type="checkbox"/> P503
QIO2:	<input checked="" type="checkbox"/> P504
QIO3:	<input checked="" type="checkbox"/> P505

Figure 9 - Synergy QSPI Flash Pin Configuration



## 7 Peripherals

The SYG-70CP has a large variety of peripherals available to use in a wide array of projects. A Board Support Package (BSP) is provided with the purchase of the SYG-70CP and is used to greatly simplify the configuration of the specific I/O needed for a given project. After installing the BSP, creating a New Synergy C Project dialog inside of e2 Studio or IAR Embedded Workbench will allow for the selection of the SYG-70CP. Creating a new project with this board choice will create a default pin configuration that will be used to configure the S7G2 MCU through the Synergy Configurator in e2 Studio or the Synergy Standalone Configurator (SSC) in IAR Embedded Workbench. There are certain options that are not configured by default, but are optional depending on your project requirements. Refer to the following sections to determine configuration requirements specific to your project and I/O needs.

### 7.1 LCD Panel

#### 7.1.1 7.0" TFT WVGA 800 x 480 PCAP Touch Screen Display (-70CP models)



only)

The SYG-70CP is equipped with a Tianma TM070RVHG01-01 7.0" TFT WVGA Projected Capacitance Touch screen display. This 800 x 480 touch screen has a 15:9 aspect ratio and 300 nits of brightness and a contrast ratio of 500:1.

The PCAP Display uses the SSD25XX Touch IC. The correct driver is shown below:

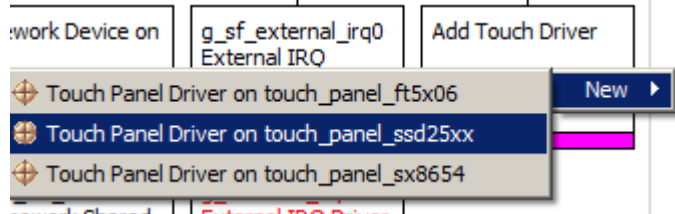


Figure 10 - Synergy Touch Panel Driver

### 7.1.2 Backlight Generator

Backlight brightness can be controlled using a PWM signal to control the backlight generator circuit. The pin for the PWM signal is configured in the BSP provided with the SYG-70CP, and the backlight circuit accepts 5KHz to 100KHz frequencies.

**Note: For Full brightness, drive P713 high (P713 = 1).**

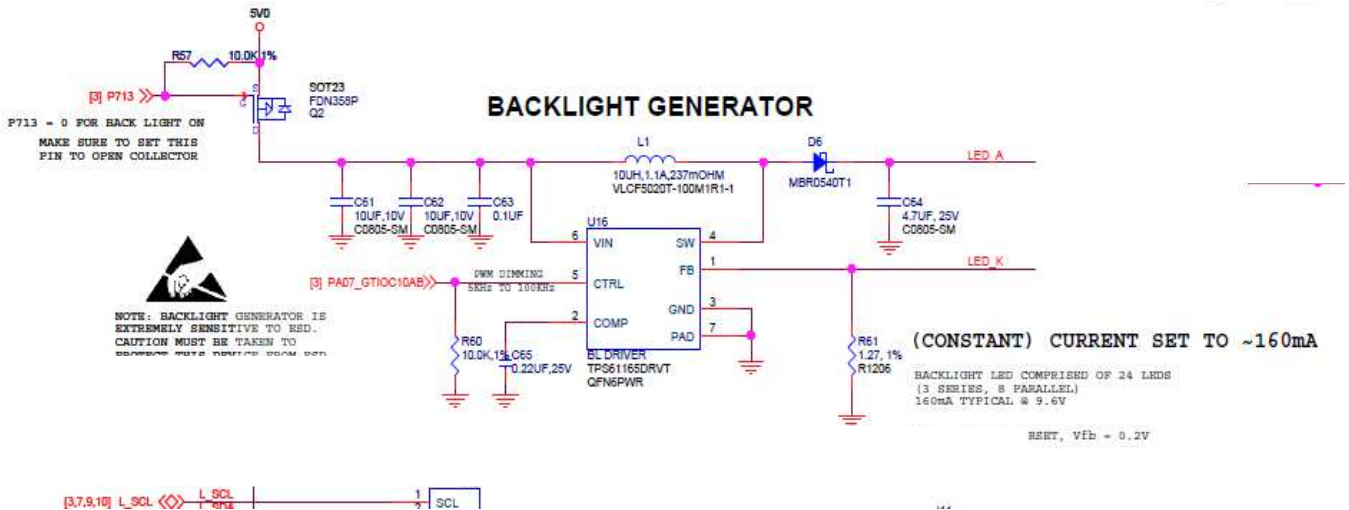


Figure 11 - Backlight Generator Circuit

It is also possible to turn off the backlight by setting P713 "low" (Low = 0). See the note on the schematic for more details.



### 7.1.3 LCD Interface

The LCD interfaces with the SYG-70CP through connector J9. This 0.5mm pitch flat ribbon cable connector is robust and allows for sturdy connection of the LCD cable to the SYG-70CP. Several resistor options are available to support a wide variety of optional LCD displays, if required. The LCD Interface connector schematic is shown below:

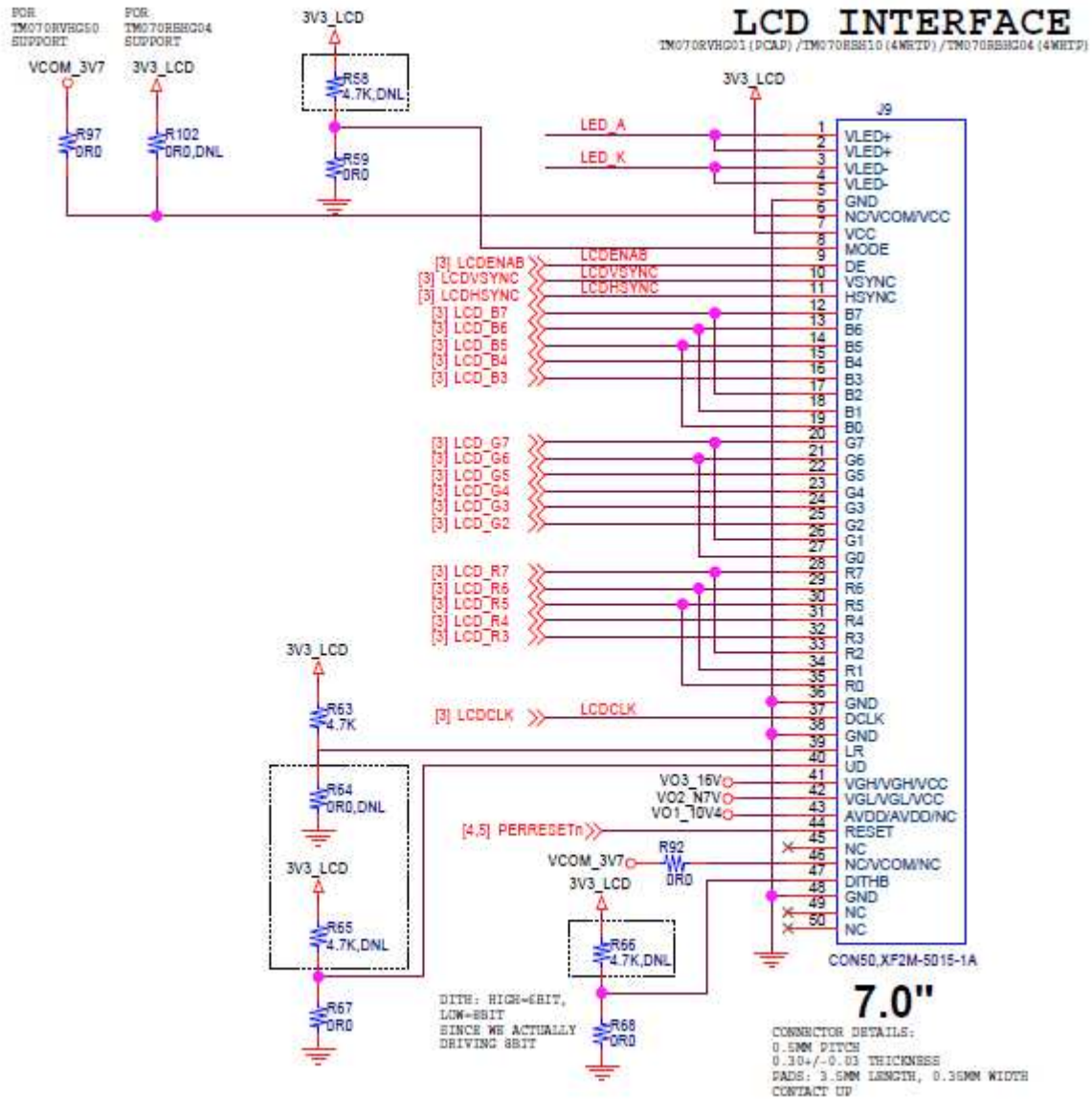


Figure 12 - LCD Interface Schematic

