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LCD Module Technical Specification

First Edition
Mar.28, 2008

Final Revision
******

Type No. **T-55149GD030J-MLW-AJN**

Customer : **OPTREX STANDARD**

Customer's Product No : ---------

OPTREX CORPORATION

Approved:	Minoru Akatsuka	QUALITY ASSURANCE DIVISION
Checked:	Toshiyuki Okamoto	DESIGN 2T
Prepared:	Takashi Yuchi	DESIGN 2T

APPROVED

By _____

Signature :

Date :

Please return this specification within two month with your signature.
If not returned within two month, specification will be considered as having been accepted.

Table of Contents

Revision History

Rev.	Date	Page	Comment

1.Application

This specification applies to 3.0"color TFT-LCD module (**T-55149GD030J-MLW-AJN**).

2.General Specifications

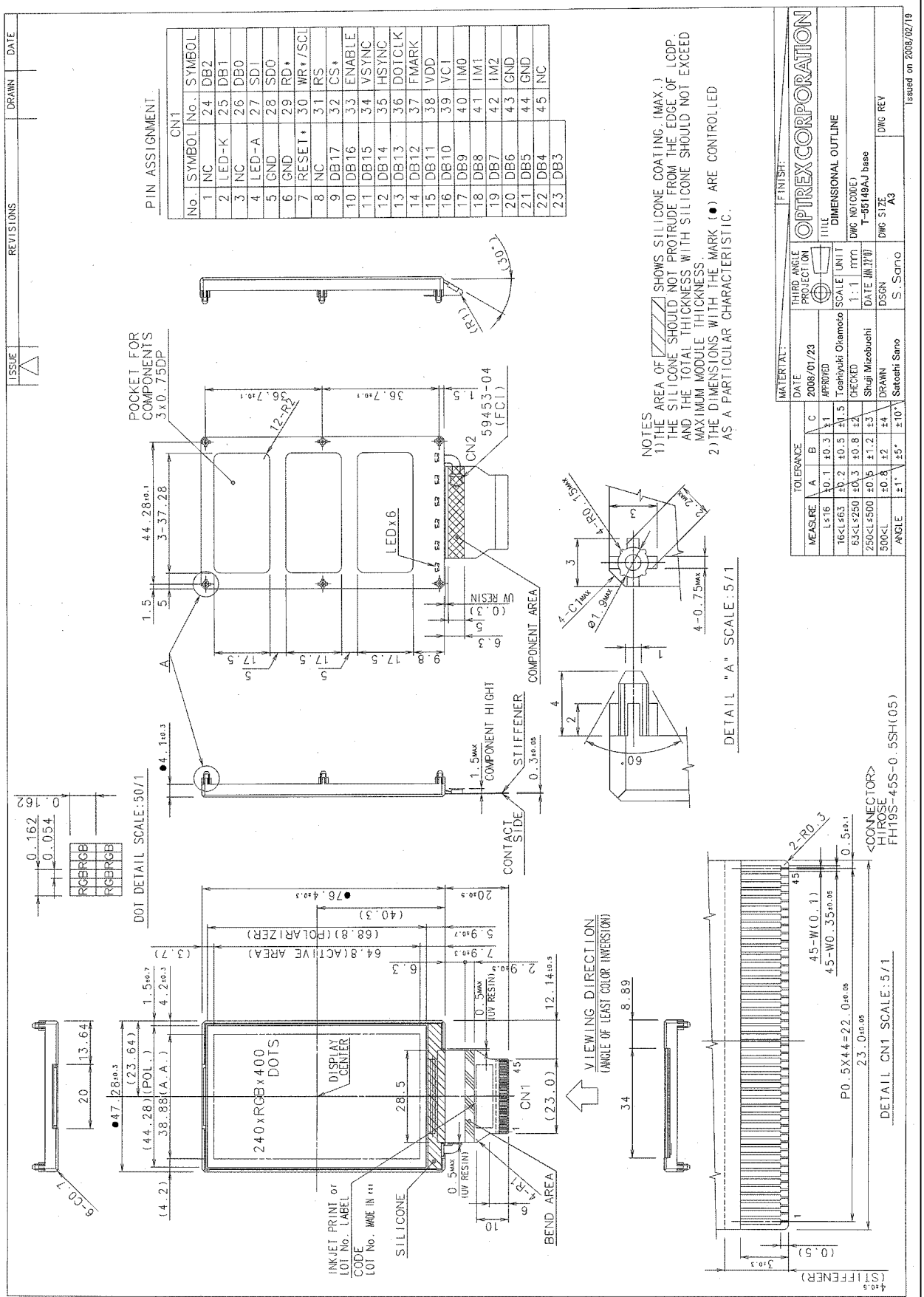
Dot Pixels	:	240×3 [R.G.B] (W) × 400 (H) dots
Dot Size	:	0.054 (W) × 0.162 (H) mm
Pixel Arrangement	:	RGB-Stripe
Color Depth	:	262144 color
Viewing Area	:	38.88 (W) × 64.8 (H) mm
Outline Dimensions*	:	47.28 (W) × 76.4* (H) × 4.4max.** (D) mm * Without FPC **Without Hook
Weight	:	24.3g max.
LCD Type	:	ASS-25521 (TFT / Normally white-mode / Transflective)
Viewing Direction	:	6:00
TFT Driver	:	Controler driver R61509(RENESAS)
Data Transfer	:	18 / 16 / 9 / 8-bit 80 system, Serial 18 / 16 / 6 RGB I/F
Back-light	:	LED Back-light / White
RoHS regulation	:	To our best knowledge, this product satisfies material requirement of RoHS regulation. Our company is doing the best efforts to obtain the equivalent certificate from our suppliers.

3.Operating Conditions

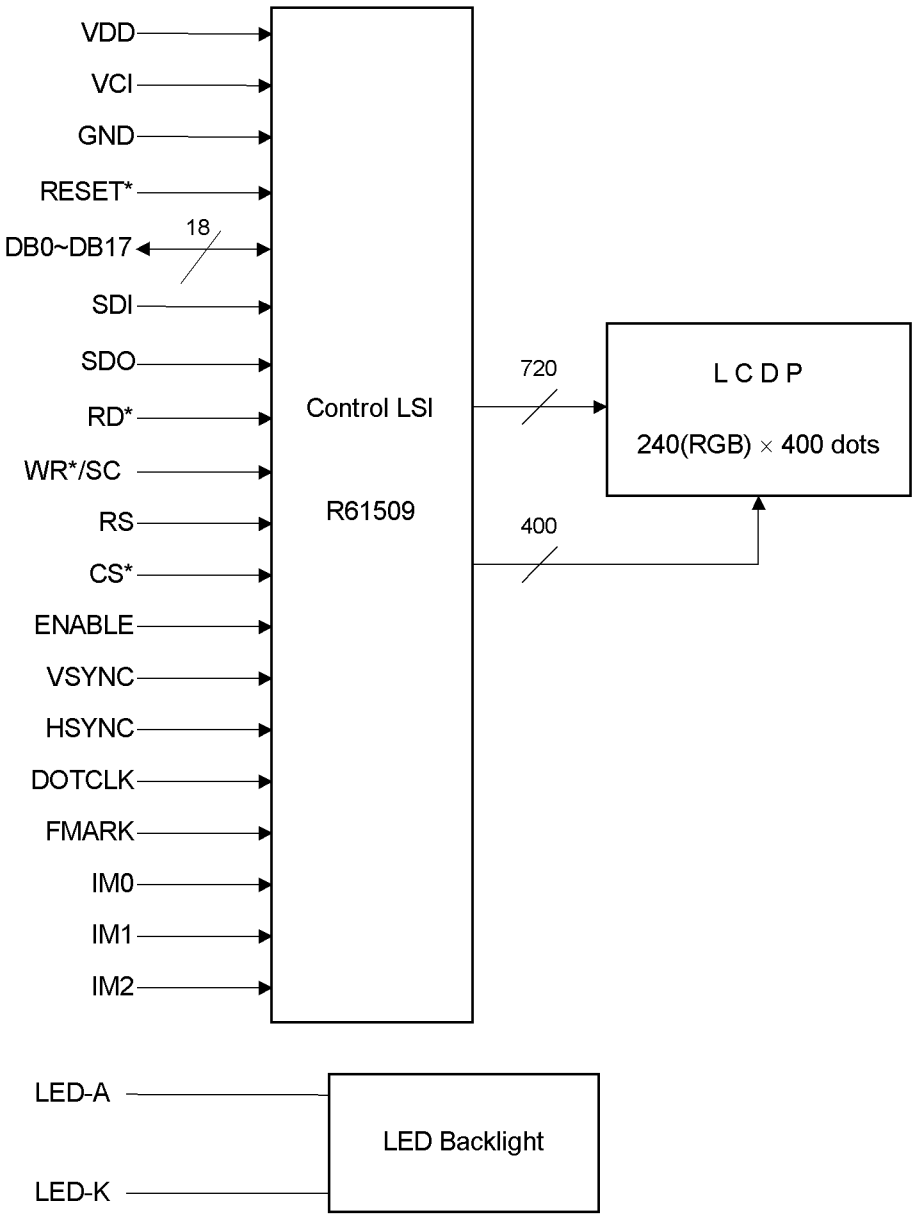
Item	Conditions	Temperature Range	Remark
Operating Temperature Range	PNL Surface	–20～70°C	Note1
Storage Temperature Range	PNL Surface	–30～80°C	

Note1: Operating temperature range defines the operation only and the contrast, response time and other display optical characteristics are set at Ta=+25°C.

4.Dimensinal Outline



5.Block Diagram



6.I/O Terminal

6.1.CN1 Pin Assignment

Corresponding Connector: HIROSE: FH19S-45S-0.5SH (05)

No.	Symbol	Functional Description
1	NC	Non Connection
2	LED-K	LED Cathode
3	NC	Non Connection
4	LED-A	LED Anode
5	GND	GND
6	GND	GND
7	RESET*	Reset Signal Input L:Active
8	NC	Non Connection
9	DB17	18-bit parallel bi-directional data bus for 80-system interface (Amplitude : IOVCC1-GND) 8 bit I/F : DB17-DB10 are used. 9 bit I/F : DB17-DB9 are used. 16 bit I/F : DB17-DB10 and DB8-1 are used. 18 bit I/F : DB17-DB0 are used. 18-bit parallel bi-directional data bus for RGB interface operation (Amplitude : IOVCC1-GND) 6 bit I/F : DB17-DB12 are used. 16 bit I/F : DB17-DB13 and DB11-1 are used. 18 bit I/F : DB17-DB0 are used.
10	DB16	
11	DB15	
12	DB14	
13	DB13	
14	DB12	
15	DB11	
16	DB10	
17	DB9	
18	DB8	
19	DB7	
20	DB6	
21	DB5	
22	DB4	
23	DB3	
24	DB2	
25	DB1	
26	DB0	
27	SDI	Input for Serial Data
28	SDO	Output for Serial Data
29	RD*	Read Control Input L:Active
30	WR*/SCL	Write Control Input L:Active / Input for Serial Clock
31	RS	Reister Select Input
32	CS*	Chip Select Input L:Active
33	ENABLE	Data enable signal for RGB interface
34	VSYNC	Vertical sync signal for RGB interface
35	HSYNC	Horizontal sync signal for RGB interface

<table>
<tr><td>36</td><td>DOTCLK</td><td>Clock signal for sampling catch data signal</td></tr>
<tr><td>37</td><td>FMARK</td><td>First Line Marker(Indicates Start of Frame)</td></tr>
<tr><td>38</td><td>VDD</td><td>Power Supply to the Intrface Pims</td></tr>
<tr><td>39</td><td>VCI</td><td>Power Supply to the LCD and Intrnal Logic</td></tr>
<tr><td>40</td><td>IM0</td><td rowspan="4">Select a mode to Interface to an MPU.In serial interface operation, the IM0 pin is used to set the ID bit of device code.
<table><tr><th>IM2</th><th>IM1</th><th>IM0</th><th>Interface Mode</th><th>DB Pin</th><th>Colors</th></tr><tr><td>0</td><td>0</td><td>0</td><td>80-system
18-bit interface</td><td>DB17-0</td><td>262,144</td></tr><tr><td>0</td><td>0</td><td>1</td><td>80-system
9-bit interface</td><td>DB17-9</td><td>262,144</td></tr><tr><td>0</td><td>1</td><td>0</td><td>80-system
16-bit interface</td><td>DB17-10
DB8-1</td><td>262,144</td></tr><tr><td>0</td><td>1</td><td>1</td><td>80-system
8-bit interface</td><td>DB17-10</td><td>262,144</td></tr><tr><td>1</td><td>0</td><td>(*ID)</td><td>Clock synchronous
serial interface</td><td>-</td><td>65,536</td></tr><tr><td>1</td><td>1</td><td>0</td><td>Setting Disabled</td><td>-</td><td>-</td></tr><tr><td>1</td><td>1</td><td>1</td><td>Setting Disabled</td><td>-</td><td>-</td></tr></table></td></tr>
<tr><td>41</td><td>IM1</td></tr>
<tr><td>42</td><td>IM2</td></tr>
<tr><td>43</td><td>GND</td><td>GND</td></tr>
<tr><td>44</td><td>GND</td><td>GND</td></tr>
<tr><td>45</td><td>NC</td><td>Non Connection</td></tr>
</table>

7.Electrical Specifications

7.1.Absolute Maximum Ratings

Ta=–20～70°C, GND=0V

Parameter	Symbol	Conditions	Min.	Max.	Units
Supply Voltage	VDD	-	-0.3	4.6	V
Supply for step-up Voltage	VCI	-	-0.3	4.6	V
Input Voltage	V_{IN}	-	-0.3	VDD+0.3	V

7.2.DC Characteristics

Ta=–20～70°C, VSS=0V

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Supply Voltage	VDD	-	1.7	1.8	1.9	V
Supply for step-up Voltage	VCI	-	2.6	2.8	3.0	V
High Level Input Voltage	V_{IH}	-	0.8VDD	-	VDD	V
Low Level Input Voltage	V_{IL}	-	GND	-	0.2VDD	V
High Level Output Voltage	V_{OH}	I_{OH}=2.0mA	VDD-0.5	-	VDD	V
Low Level Output Voltage	V_{OL}	I_{OL}=2.0mA	GND	-	0.5	V
Supply Current	IDD	Still picture VDD - GND = 1.8V without back-light (Note 1)I_{OL}=2.0mA	-	2.1	5.0	μA
Supply Current	ICI	Still picture VCI - GND = 2.8V without back-light (Note 1)	-	10.5	15.8	mA
VCOM High Level	V_{COMH}	Still picture VCI - GND = 2.8V	-	(3.1)	-	V
VCOM Low Level	V_{COML}	Still picture VCI - GND = 2.8V	-	(-0.8)	-	V

Note1: The driving conditions are to be described.

Note2: Please keep VCI VDD

: DB17~DB0, RESET, RD, WR/SCL, RS, CS, ENABLE, VSYNC, HSYNC, DOTCLK, FMARK

7.3.AC Characteristics

7.3.1. 80-system Bus Interface Timing Characteristics

(1) 16 or 18bit Inetrface (Normal write mode: R003h; IB9=0)

Condition: Ta=–20～70°C, VDD=1.7V~1.9V

Parameter		Symbol	Min.	Typ.	Max.	Units
Bus cycle Time	Write	t_{CYCW}	110	-	-	ns
	Read	t_{CYCR}	450	-	-	ns
Write low-level pulse width		PW_{LW}	30	-	-	ns
Read low-level pulse width		PW_{LR}	170	-	-	ns
Write High-level pulse width		PW_{HW}	30	-	-	ns
Read High-level pulse width		PW_{HR}	250	-	-	ns
Write Read Rise/Fall Time		t_{WRr}, t_{WRf}	-	-	10	ns
SetupTime	Write (RS to CS*,WR*)	t_{AS}	0	-	-	ns
	Read (RS to CS*,RD*)		10	-		
Address hold Time		t_{AH}	2	-	-	ns
Write Data Setup Time		t_{DSW}	20	-	-	ns
Write Data Hold Time		t_{HWR}	10	-	-	ns
Read Data Delay Time		t_{DDR}	-	-	150	ns
Read Data Hold Time		t_{DHR}	5	-	-	ns

(2) 16 or 18bit Inetrface (High speed write mode: R003h; IB9=1)

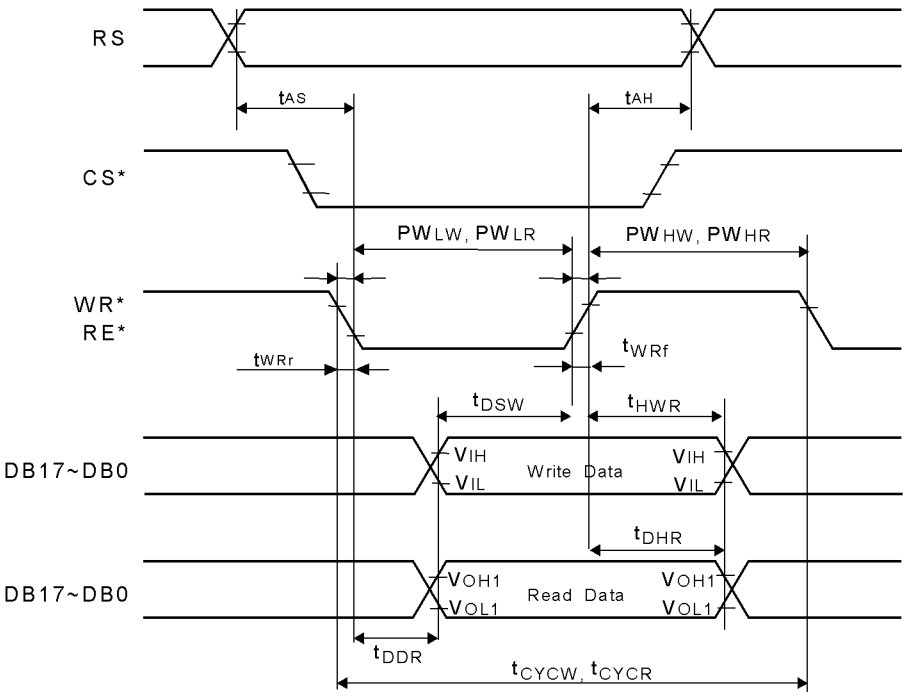
Condition: Ta=–20～70°C, VDD=1.7V~1.9V

Parameter		Symbol	Min.	Typ.	Max.	Units
Bus cycle Time	Write	t_{CYCW}	65	-	-	ns
	Read	t_{CYCR}	450	-	-	ns
Write low-level pulse width		PW_{LW}	30	-	-	ns
Read low-level pulse width		PW_{LR}	170	-	-	ns
Write High-level pulse width		PW_{HW}	20	-	-	ns
Read High-level pulse width		PW_{HR}	250	-	-	ns
Write Read Rise/Fall Time		t_{WRr}, t_{WRf}	-	-	10	ns
SetupTime	Write (RS to CS*,WR*)	t_{AS}	0	-	-	ns
	Read (RS to CS*,RD*)		10	-		
Address hold Time		t_{AH}	2	-	-	ns
Write Data Setup Time		t_{DSW}	20	-	-	ns
Write Data Hold Time		t_{HWR}	10	-	-	ns
Read Data Delay Time		t_{DDR}	-	-	150	ns
Read Data Hold Time		t_{DHR}	5	-	-	ns

(3) 8 or 9bit Inetrface (Normal / High speed write mode: R003h; IB9=0/1)

Condition: Ta=–20～70°C, VDD=1.7V~1.9V

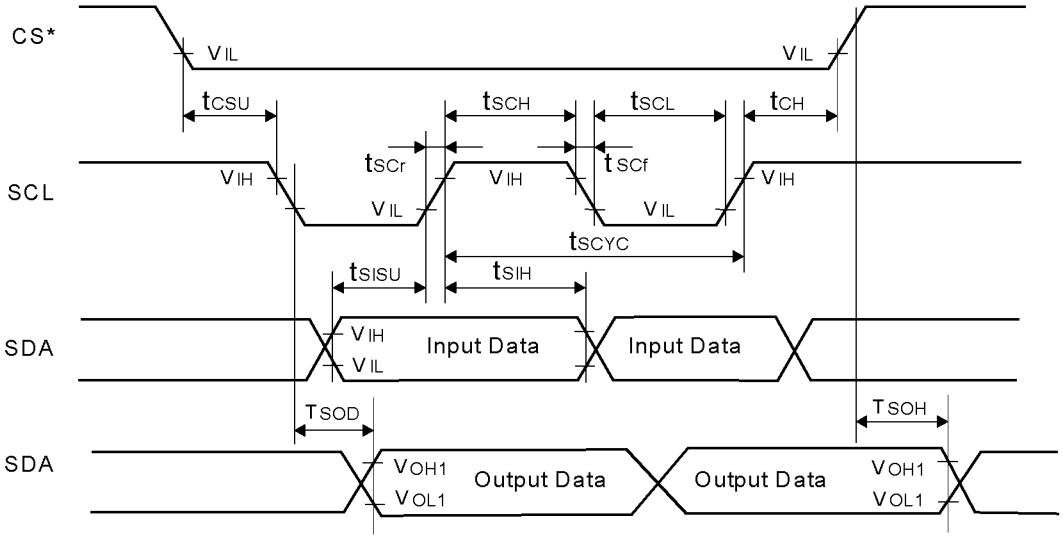
Parameter		Symbol	Min.	Typ.	Max.	Units
Bus cycle Time	Write	t_{CYCW}	60	-	-	ns
	Read	t_{CYCR}	450	-	-	ns
Write low-level pulse width		PW_{LW}	30	-	-	ns
Read low-level pulse width		PW_{LR}	170	-	-	ns
Write High-level pulse width		PW_{HW}	20	-	-	ns
Read High-level pulse width		PW_{HR}	250	-	-	ns
Write Read Rise/Fall Time		t_{WRr}, t_{WRf}	-	-	10	ns
SetupTime	Write (RS to CS*,WR*)	t_{AS}	0	-	-	ns
	Read (RS to CS*,RD*)		10	-		
Address hold Time		t_{AH}	2	-	-	ns
Write Data Setup Time		t_{DSW}	20	-	-	ns
Write Data Hold Time		t_{HWR}	10	-	-	ns
Read Data Delay Time		t_{DDR}	-	-	150	ns
Read Data Hold Time		t_{DHR}	5	-	-	ns



7.3.2.Clock-synchronized Serial Interface Timing Characteristics

Condition: Ta=–20～70°C, VDD=1.7V~1.9V

Parameter	Symbol	Min.	Typ.	Max.	Units
Serial Clock Cycle time (Write)	t_{SCYC}	100	-	20000	ns
Serial Clock Cycle time (Read)	t_{SCYC}	350	-	20000	ns
Serial Clock (High Level Width) (Write)	t_{SCH}	40	-	-	ns
Serial Clock (High Level Width) (Read)	t_{SCH}	150	-	-	ns
Serial Clock (Low Level Width) (Write)	t_{SCL}	40	-	-	ns
Serial Clock (Low Level Width) (Read)	t_{SCL}	150	-	-	ns
Serial Clock Rise/Fall Time	t_{SCf},t_{SCr}	-	-	20	ns
Chip Select Set-up Time	t_{CSU}	20	-	-	ns
Chip Select Hold Time	t_{CH}	60	-	-	ns
Serial Input Data Set-up Time	t_{SISU}	30	-	-	ns
Serial Input Data Hold Time	t_{SIH}	30	-	-	ns
Serial Output Data Delay Time	t_{SOD}	-	-	130	ns
Serial Output Data Hold Time	t_{SOH}	5	-	-	ns



7.3.3.RGB Interface

(1) 16 or 18bit RGB Inetrface (High speed write mode: R003h; IB9=1)

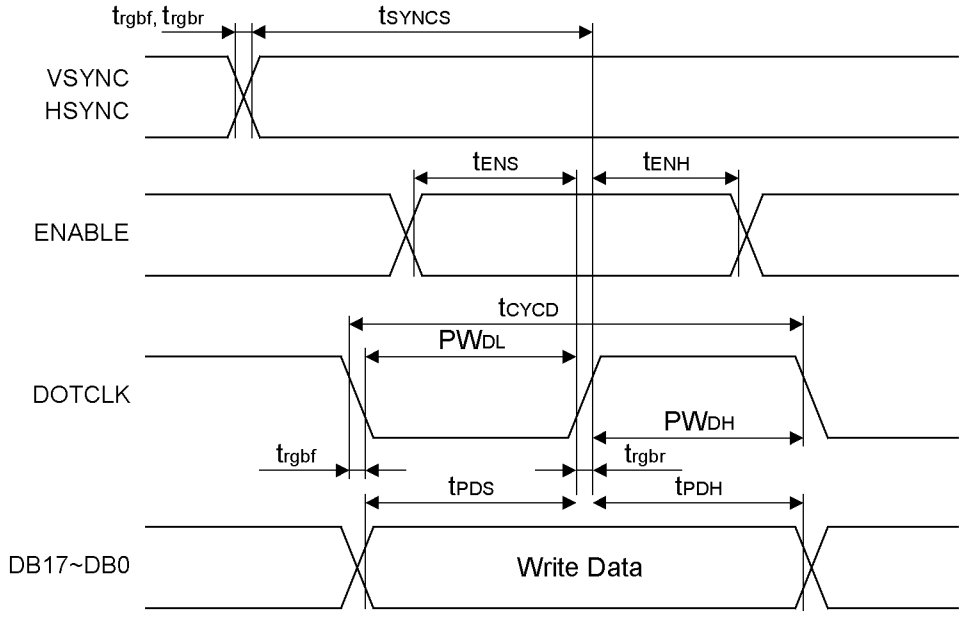
Ta=–20～70°C, VDD=1.7V~1.9V

Parameter	Symbol	Min.	Typ.	Max.	Units
VSYNC/HSYNC Setup Time	t_{SYNCS}	0	-	1	clock
Enable Setup Time	t_{ENS}	10	-	-	ns
Enable Hold Time	t_{ENH}	20	-	-	ns
DOTCLK Low-level pulse width	PW_{DL}	40	-	-	ns
DOTCLK High-level pulse width	PW_{DH}	40	-	-	ns
DOTCLK Cycle Time	t_{CYCD}	100	-	-	ns
Data Setup Time	t_{PDS}	10	-	-	ns
Data Hold Time	t_{PDH}	40	-	-	ns
DOTCLK, VSYNC, HSYNC Rise/Fall Time	t_{rgbr}, t_{rgbf}	-	-	25	ns

(2) 6bit RGB Inetrface (High speed write mode: R003h; IB9=1)

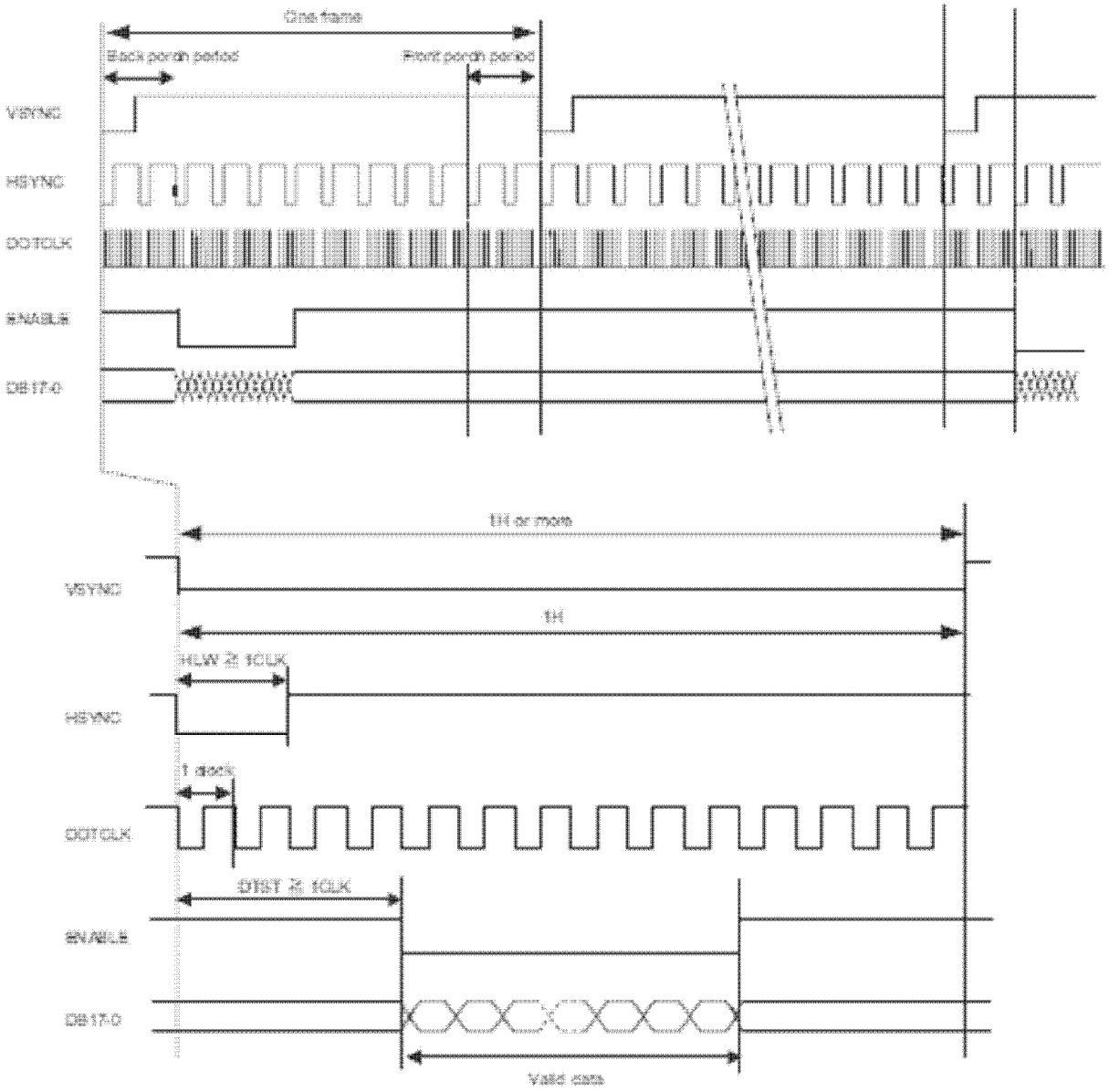
Ta=–20～70°C, VDD=1.7V~1.9V

Parameter	Symbol	Min.	Typ.	Max.	Units
VSYNC/HSYNC Setup Time	t_{SYNCS}	0	-	1	clock
Enable Setup Time	t_{ENS}	10	-	-	ns
Enable Hold Time	t_{ENH}	25	-	-	ns
DOTCLK Low-level pulse width	PW_{DL}	25	-	-	ns
DOTCLK High-level pulse width	PW_{DH}	25	-	-	ns
DOTCLK Cycle Time	t_{CYCD}	60	-	-	ns
Data Setup Time	t_{PDS}	10	-	-	ns
Data Hold Time	t_{PDH}	25	-	-	ns
DOTCLK, VSYNC, HSYNC Rise/Fall Time	t_{rgbr}, t_{rgbf}	-	-	25	ns

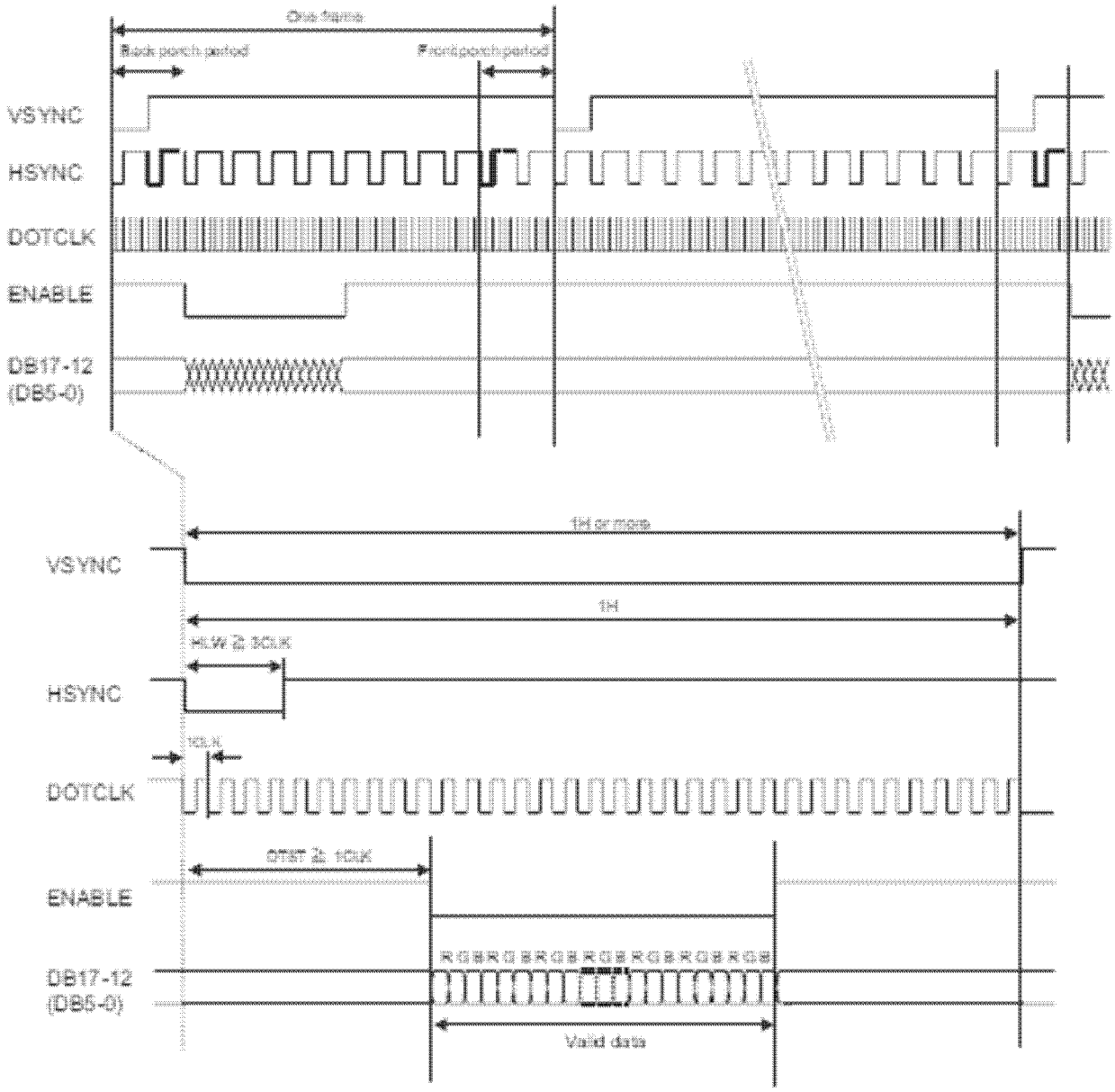


7.3.4.RGB Interface Timing

(1) 16 or 18bit RGB Interface Timing



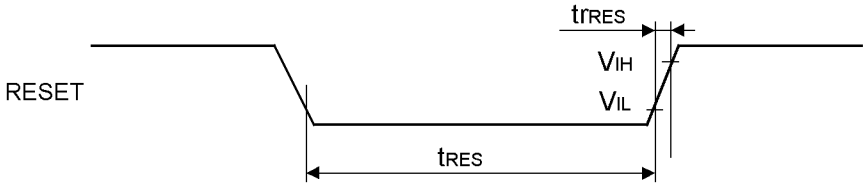
(2) 6bit RGB Interface Timing



7.3.5.Reset Timing Characteristics

Ta=–20～70°C, VDD=1.7V~1.9V

Parameter	Symbol	Min.	Max.	Units
Reset ”L” Pulse Width	t_{RES}	1	-	ms
Reset Rise Time	tr_{RES}	-	10	μs

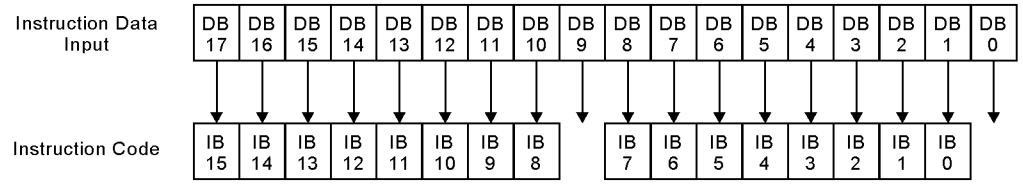


7.4.Data Format

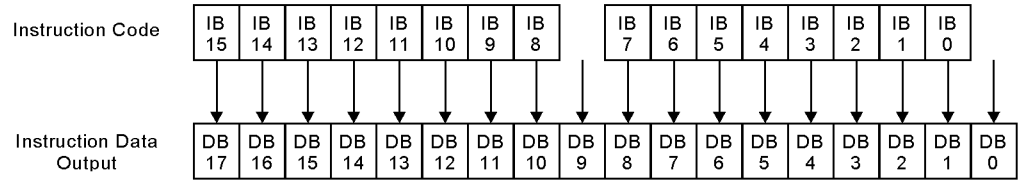
7.4.1.80-system Interface Data Format

(1) 18Bit Interface（IM2=0, IM1=0, IM0=0）

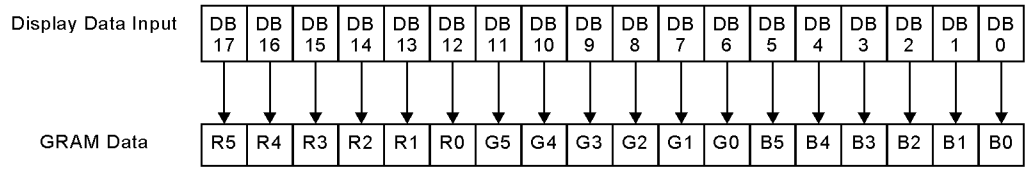
◆ Instruction Write



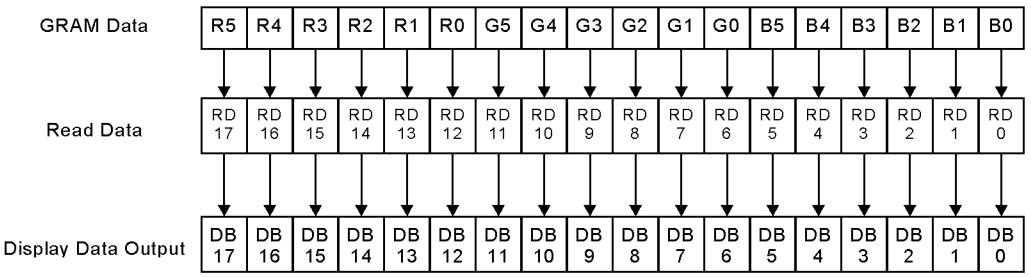
◆ Device Code Read



◆ RAM Data Write

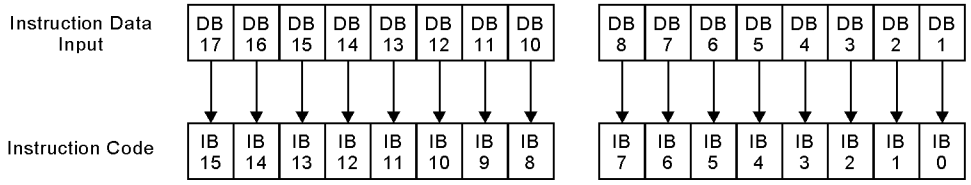


◆ RAM Data Read

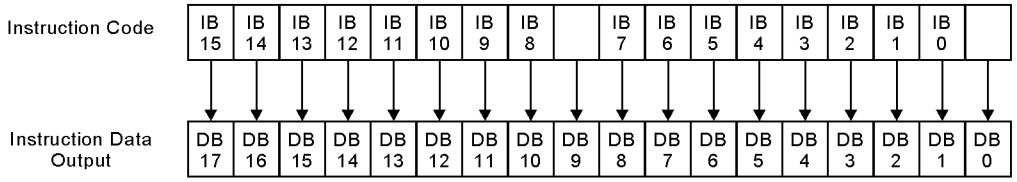


(2) 16Bit Interface（IM2=0, IM1=1, IM0=0）

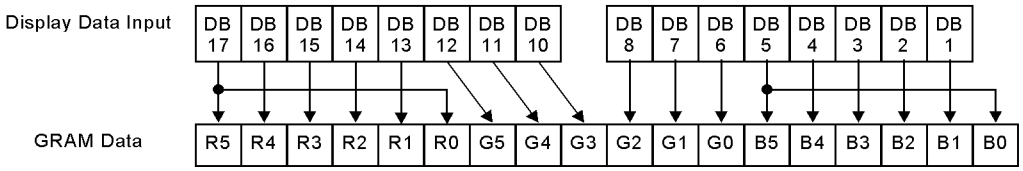
◆ Instruction Write



◆ Device Code Read

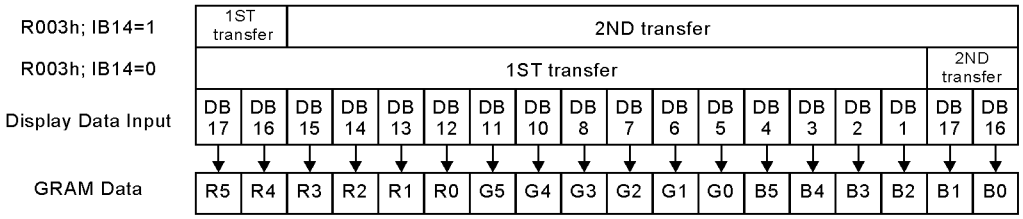


◆ RAM Data Write (1 time data transfer Mode: R003h; IB15=0) 65,536 colors

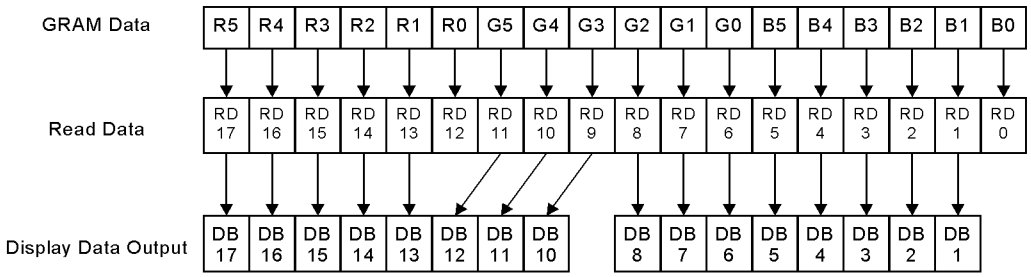


◆ RAM Data Write (2 times data transfer Mode: R003h; IB15=0) 262,144 colors

Note: Please refer to (5) Data Transfer Synchronization in 16, 9, 8-Bit Bus Interface Operation



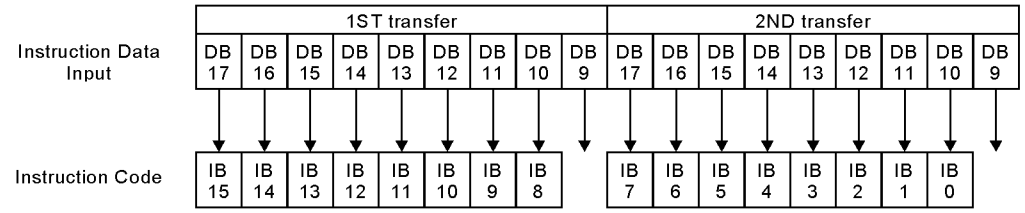
◆ RAM Data Read (1 time data transfer Mode: R003h; IB15=0) 65,536 colors



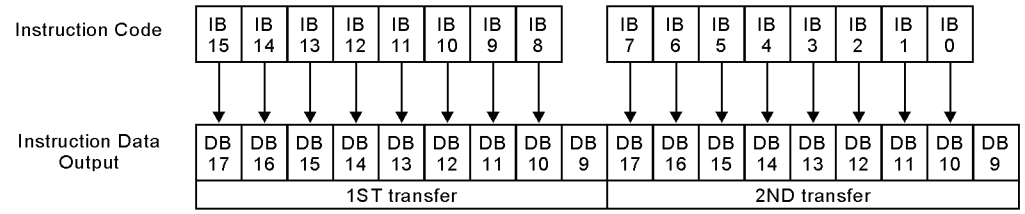
RAM Data Read in 2 times transfer mode cannot be performed.

(3) 9Bit Interface（IM2=0, IM1=0, IM0=1）

◆ Instruction Write

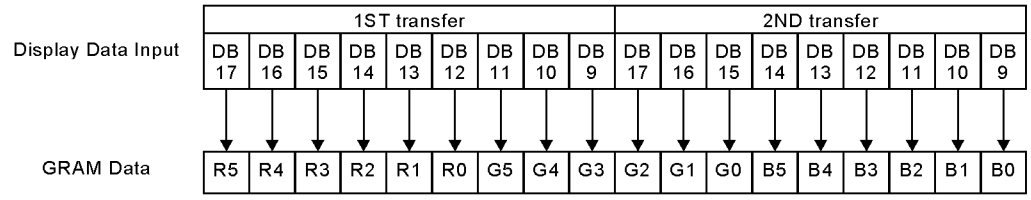


◆ Device Code Read

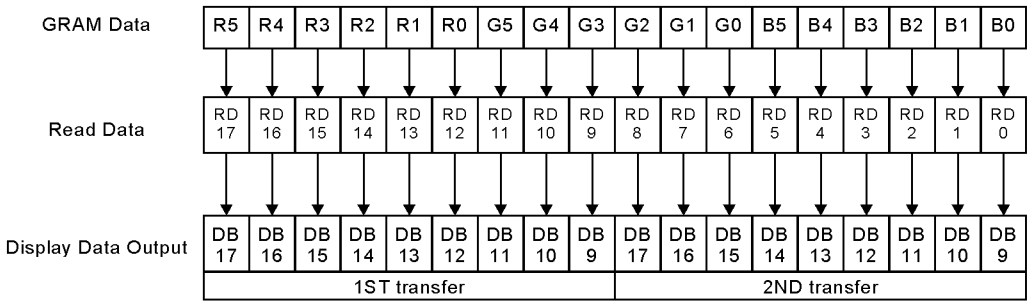


◆ RAM Data Write

Note: Please refer to (5) Data Transfer Synchronization in 16, 9, 8-Bit Bus Interface Operation

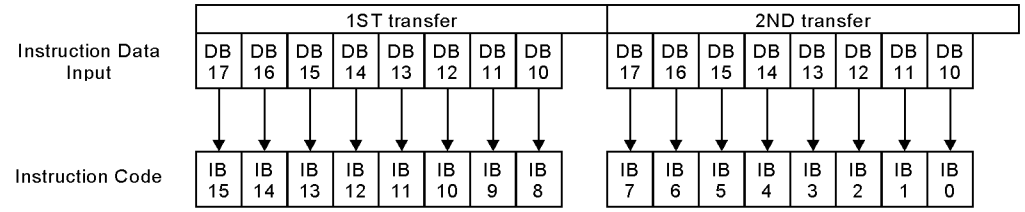


◆ RAM Data Read

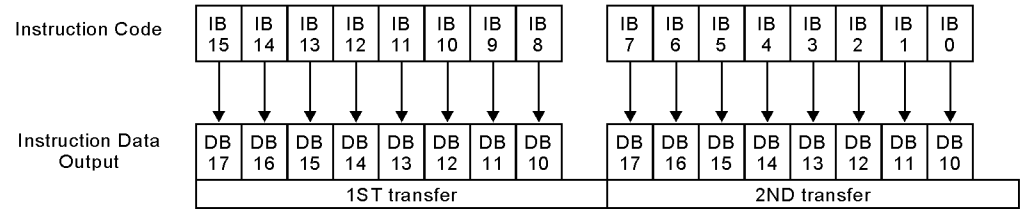


(4) 8Bit Interface（IM2=0, IM1=1, IM0=1）

◆ Instruction Write

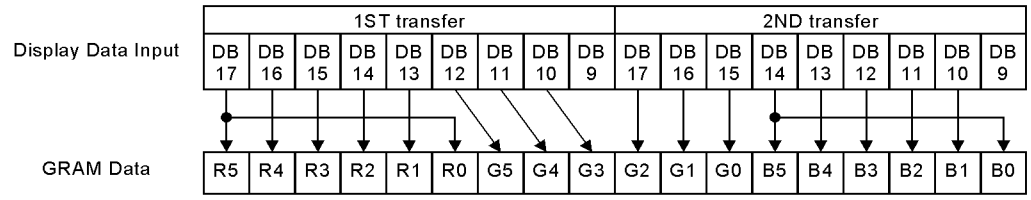


◆ Device Code Read



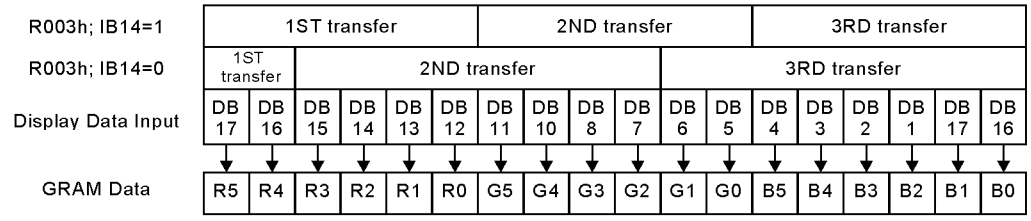
◆ RAM Data Write (2 times data transfer Mode:R003h; IB15=0) 65,536 colors

Note: Please refer to (5) Data Transfer Synchronization in 16, 9, 8-Bit Bus Interface Operation

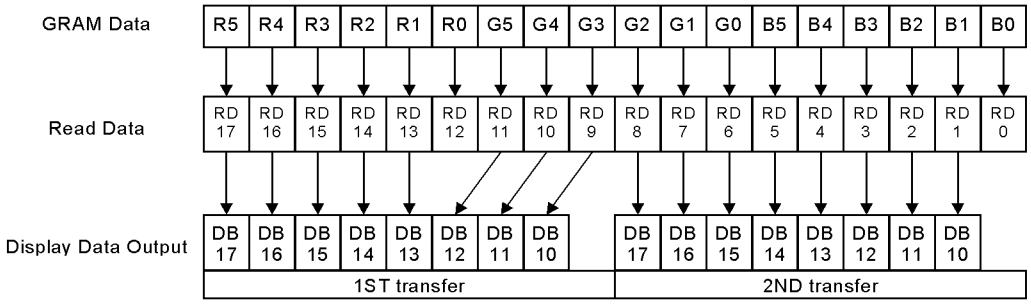


◆ RAM Data Write (3 times data transfer Mode:R003h; IB15=1) 262,144 colors

Note: Please refer to (5) Data Transfer Synchronization in 16, 9, 8-Bit Bus Interface Operation



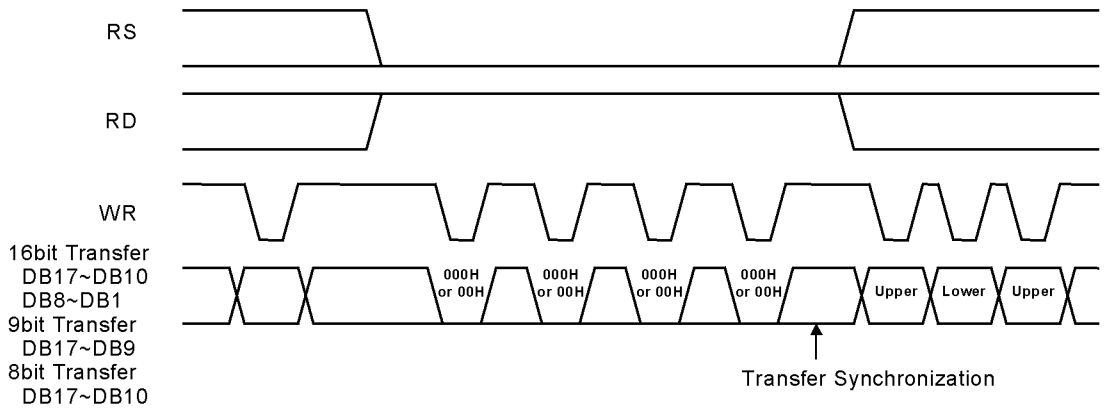
◆ RAM Data Read



RAM Data Read in 3 times transfer mode cannot be performed.

(5) Data Transfer Synchronization in 16, 9, 8-Bit Bus Interface Operation

When a mismatch occurs in upper and lower data transfers due to noise and so on, the 000H (or 00H) instruction is written four times consecutively to reset the upper and lower counters in order to restart the data transfer from upper bits.
The data transfer synchronization, when executed periodically, can help the display system recover from runaway.
Make sure to execute data transfer synchronization after reset operation before transferring instruction.



7.4.2. Clock-synchronized Serial Interface （IM2=1, IM1=0, IM0=ID）

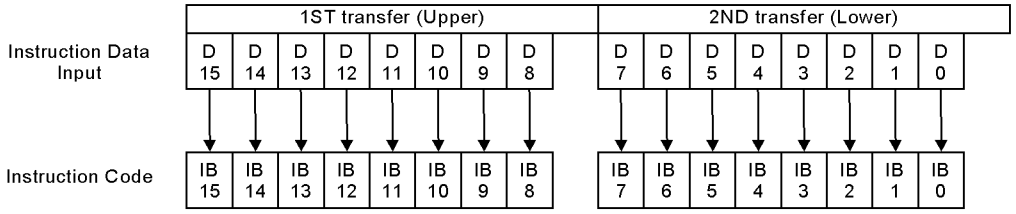
◆ Start Byte Format

Bit	1	2	3	4	5	6	7	8
Start Byte Format	0	1	1	1	0	ID	RS	R/W
IM=0	0	1	1	1	0	0	RS	R/W
IM=1	0	1	1	1	0	1	RS	R/W

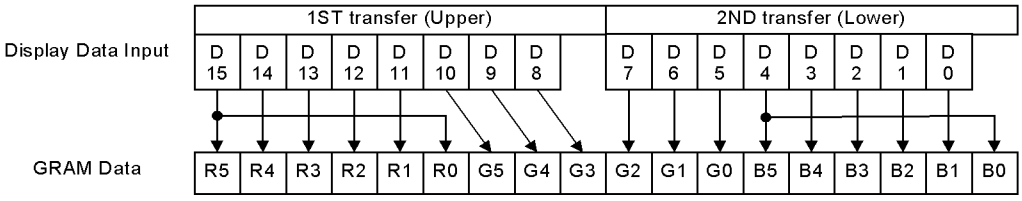
◆ Function of RS, R/W

RS	R/W	Function
0	0	Setting of Instruction Code
0	1	Prohibition
1	0	Write Instruction data
1	1	Read Instruction data

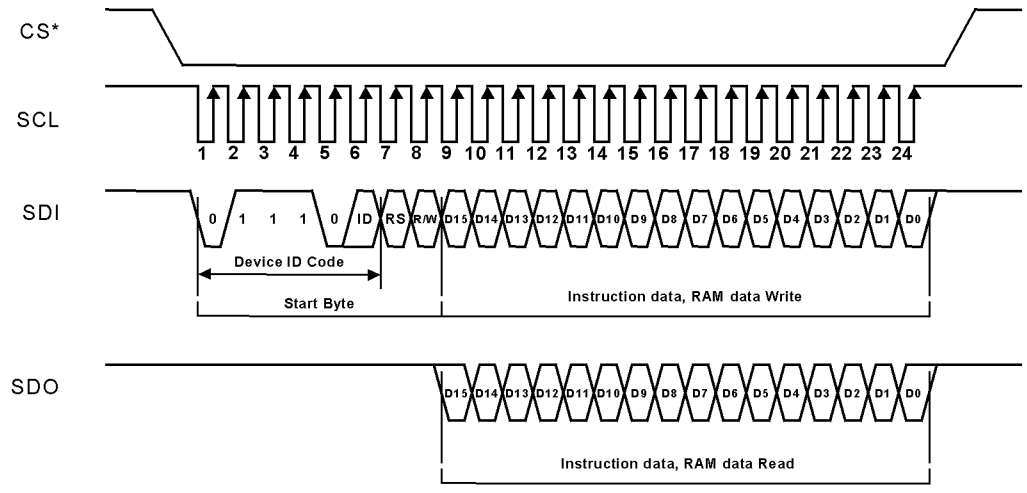
◆ Instruction Write



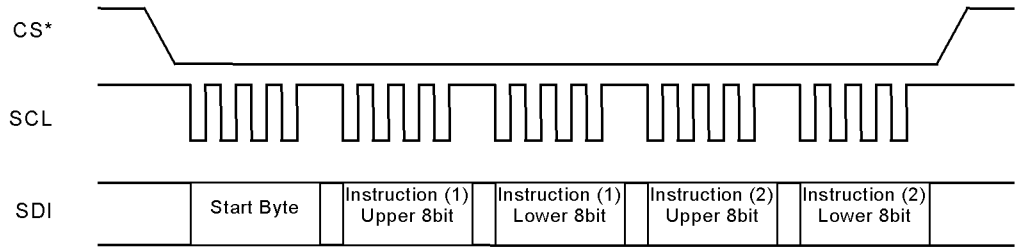
◆ RAM Data Write 65,536 colors



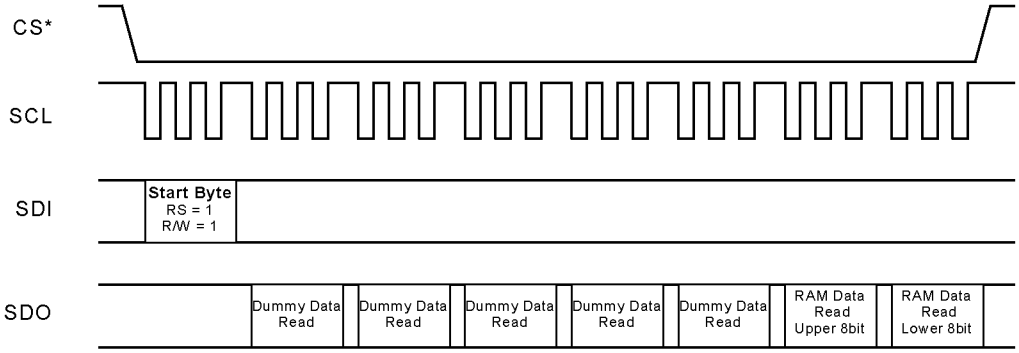
◆ **Transfer of Clock-synchronized Serial Inetrface**



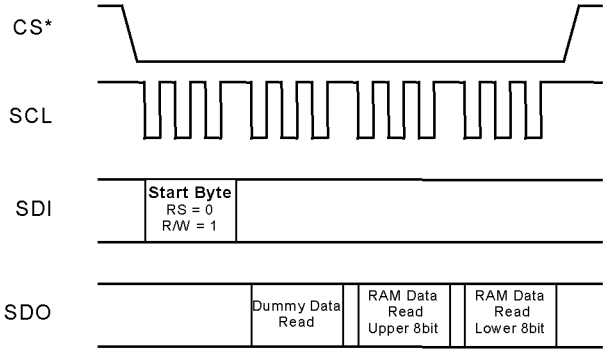
◆ **Transfer of Continuous Data**



◆ **RAM Data Read**



◆ **Instruction Data Read**



7.5.Power ON / OFF Sequence

7.5.1.Relationship of Instruction Code and Hexadecimal Number

Instruction Code	IB 15	IB 14	IB 13	IB 12	IB 11	IB 10	IB 9	IB 8	IB 7	IB 6	IB 5	IB 4	IB 3	IB 2	IB 1	IB 0	
Example (Binary)	0	0	0	1	1	0	1	1	1	0	0	0	1	1	1	0	**Bin**
Example (Hexadecimal)		1				B				8				E			**Hex**

7.5.2.Command List for Power ON (Recommended Setting)

Setting Item	Index (Value)	Value(2byte Setting)	Remark
Power ON			
Power ON	Input VDD=1.80V VDD2=2.80V		
Reset			
Reset	RESET Pulse "L"		Reset
Wait	10msec		
Release Reset	RESET Pulse "H"		Release Reset
Wait	10msec		
Application Setup			
Device Cord Read (/RD)	0000 h	1509 h	Access check
Base Image Number of Line	0400 h	3100 h	NL0=400Lines, SCN=0
Driver Output	0001 h	0100 h	S720→S1
LCD Driving Wave Control	0002 h	0100 h	C Pattern Waveform
Entry Mode	0003 h	1230 h	BGR=1, HMW=1, I/D=11
Display Control 2	0008 h	0808 h	FP=BP=8Lines
Low Power Control 2	000b h	0010 h	VEM=1, 262,144color
External Display Interface Control 2	000F h	0000 h	DOTCLK ↓, ENABLE=L(Valid), HSYNC=VSYNC=Low Active
PNL Interface Control 1	0010 h	001F h	Div ratio = 1/2 1H(Line)=16clock
PNL Interface Control 2	0011 h	0000 h	1clock
PNL Interface Control 3	0012 h	0000 h	0clock
PNL Interface Control 4	0020 h	021E h	30clock/8
PNL Interface Control 5	0021 h	0000 h	0clock
PNL Interface Control 6	0022 h	0000 h	0clock
Window Horizontal RAM Address 1	0210 h	0000 h	Start Address X=00h
Window Horizontal RAM Address 2	0211 h	00EF h	End Address X=EFh
Window Vertical RAM Address 1	0212 h	0000 h	Start Address Y=00h
Window Vertical RAM Address 2	0213 h	018F h	Start Address Y=18Fh
Gamma Control 1	0300 h	0706 h	Gamma Setting
Gamma Control 2	0301 h	0607 h	Gamma Setting
Gamma Control 3	0302 h	0301 h	Gamma Setting
Gamma Control 4	0303 h	0202 h	Gamma Setting
Gamma Control 5	0304 h	0303 h	Gamma Setting
Gamma Control 6	0305 h	0207 h	Gamma Setting
Gamma Control 7	0306 h	0808 h	Gamma Setting
Gamma Control 8	0307 h	0706 h	Gamma Setting
Gamma Control 9	0308 h	0607 h	Gamma Setting
Gamma Control 10	0309 h	0301 h	Gamma Setting
Gamma Control 11	030A h	0303 h	Gamma Setting
Gamma Control 12	030B h	0202 h	Gamma Setting
Gamma Control 13	030C h	0207 h	Gamma Setting
Gamma Control 14	030D h	1f1f h	Gamma Setting
Base Image Display Control	0401 h	0001h	Reversed Image
Base Image Vertical Scroll Control	0404 h	0000 h	Non-Scroll
LCD Power Setup			
Display Control 1	0007 h	0001 h	FMARK = IC internal = Operating
Power Control 6	0110 h	0001 h	LCD Power ON
Power Sequence Control 1	0112 h	0060 h	
Power Control 1	0100 h	17B0 h	G/S=ON, Booster: VGH=6times, VGL=3times, AMP=1
Power Control 2	0101 h	0007 h	Booster Clock: 1st=1, 2nd=1/16, x1.00
Power Control 3	0102 h	01A8 h	Internal reference voltage = 4.0V
Power Control 4	0103 h	2e00 h	x0.98
VCOM High Voltage 1	0281 h	0015 h	x0.90
Power Control 2	0101 h	0014 h	Booster Clock: 1st=1, 2nd=1/32, x0.76
Power Control 3	0102 h	01AC h	Internal reference voltage = 4.5V, PSON =0, PON=1
Wait	150msec		

Display ON			
Display Control 1	0007 h	0021 h	Gatr = ON, Source = OFF VCOM=OFF
Wait	1msec		
Power Control 6	0110 h	0001 h	LCD Power ON
Power Control 1	0100 h	16B0 h	G/S=ON, Booster: VGH=6times, VGL=4times, AMP=1
Power Control 2	0101 h	0117 h	Booster Clock: 1st=1/2, 2nd=1/32, x1.00
Power Control 3	0102 h	01B8 h	Internal reference voltage = 4.0V, PSON =1, PON=1
Power Control 4	0103 h	2e00 h	x0.98
VCOM High Voltage 1	0281 h	0015 h	x0.90
Display Control 1	0007 h	0061 h	Gatr = ON, Source = OFF VCOM=ON
Wait	50msec		
Display Control 1	0007 h	0173 h	Base Image Display

7.5.3.Command List for Power OFF (Recommended Setting)

Setting Item	Index (Value)	Value(2byte Setting)	Remark
Display OFF			
Display Control 1	0007 h	0072 h	Display OFF
Wait	(50msec)		
Display Control 1	0007 h	0001 h	Display OFF
Wait	(150msec)		
Display Control 1	0007 h	0000 h	Display OFF
Power ON1			
Power Control 1	0100 h	0680 h	G/S=ON, Booster: VGH=6times, VGL=4times, AMP=1
Power Control 2	0101 h	0667 h	Booster Clock: 1st=1/2, 2nd=1/32, x1.00
Power Control 3	0102 h	01A8 h	Internal reference voltage = 4.5V, PSON =1, PON=0
Power Control 4	0103 h	0e00 h	VCOMG=0
Wait	(10msec)		
Power Control 1	0100 h	0600 h	G/S=ON, Booster: VGH=6times, VGL=4times, AMP=0
Power OFF2			
Power OFF	–		

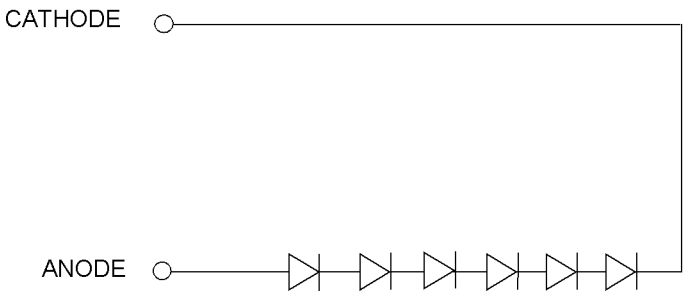
7.6.Back-light Specifications

7.6.1.Absolute Maximum Ratings (6 chips)

Ta=25°C

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Foward Current	I_F	-	-	-	30	mA
Reverse Voltage	V_R	Note1	-	-	2.0	V
LED Power Dissipation	P_D	-	-	-	115	mW

Note 1 : IR=10mA



7.6.2.Operating Characteristics

Ta=25°C

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Foward Voltage	V_F	I_F=20mA	18.0	19.2	20.4	V

8.Optical Specifications

8.1.Back-light Off

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit	Remark
Contrast Ratio	CR	Optimal	-	13	-	-	Note1
Reflectivity	R	Optimal	15	20	-	%	Note1,2
White Chromaticity	X	CIE	0.29	0.32	0.35	-	Note1
	Y		0.31	0.34	0.37	-	Note1,8
Red Chromaticity	X	CIE	0.37	0.40	0.43	-	Note1,8
	Y		0.31	0.34	0.37	-	Note1,8
Green Chromaticity	X	CIE	0.29	0.32	0.35	-	Note1,8
	Y		0.37	040	0.43	-	Note1,8
Blue Chromaticity	X	CIE	0.15	0.18	0.21	-	Note1,8
	Y		0.18	0.21	0.24	-	Note1,8

8.2.Back-light On

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit	Remark
Viewing angle range	θ_{LEFT}	CR≥5	-	70	-	Degrees	Note3,4,5,12
	θ_{UP}		-	80	-	Degrees	Note3,4,5,12
	θ_{RIGHT}		-	70	-	Degrees	Note3,4,5,12
	θ_{DOWN}		-	58	-	Degrees	Note3,4,5,12
Contrast Ratio	CR	Optimal	-	105	-	-	Note4,8,11,12
Brightness	Y	Optimal	-	400	-	cd/m^2	Note8,10,11,12
Brightness Uniformity	Y	Optimal	70	-		%	Note7,10,11,12
Viewing Direction				6:00		o'clock	Note7,11
Response Rise Time	τr	θ=0°	-	23.0	-	ms	Note7,11,12
Response Fall Time	τd	Ta=25°C	-	53.0	-	ms	Note7,11,12
White Chromaticity	X	CIE	0.25	0.30	0.35	-	Note8,11,12
	Y		0.29	0.34	0.39	-	Note8,11,12
Red Chromaticity	X	CIE	0.48	0.53	0.58	-	Note8,11,12
	Y		0.32	0.37	0.42	-	Note8,11,12
Green Chromaticity	X	CIE	0.28	0.33	0.38	-	Note8,11,12
	Y		0.47	0.52	0.57	-	Note8,11,12
Blue Chromaticity	X	CIE	0.10	0.15	0.20	-	Note8,11,12
	Y		0.10	0.15	0.20	-	Note8,11,12