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# QorIQ T1024/14 and T1023/13 Communications Processors

Next-generation system-on-chip (SoC) for low-cost enterprise and service provider edge and network control applications

## TARGET APPLICATIONS

- ▶ Wired and wireless branch routers
- ▶ WLAN 11ac enterprise access points
- ▶ Service provider WLAN access points
- ▶ Unified threat management gateways
- ▶ Multifunction printers
- ▶ Router and switch controllers
- ▶ Line card controllers
- ▶ Industrial automation and computing, single board computers
- ▶ Aerospace and defense ruggedized network equipment

The QorIQ T1024/23 communications processors combine single or dual 64-bit cores, built on Power Architecture® technology, with high-performance Data Path Acceleration Architecture (DPAA) and network peripheral bus interfaces required for networking and telecommunications applications. The T1024 and T1014 processors come in a full featured 23 x 23 mm package which provides scalable pin compatibility with the quad-core T1042 processor, and even the eight-core T2081 processor, for price and power scaling with a single system design. The T1023 and T1013 processors are interfaces and power-optimized SoCs designed to deliver impressive

single- or dual-core performance for cost and power sensitive networking systems. Both versions offer an excellent software compatible 64-bit and I/O upgrade path for the popular QorIQ P10XX family of 32-bit communications processors.

## SOFTWARE AND TOOL SUPPORT

With the help of our partner network, we deliver a wide range of tools, run-time software, reference solutions and services to accelerate your designs.

- ▶ CodeWarrior Development Studio for Power Architecture technology
- ▶ Proprietary QorIQ Linux® SDK
- ▶ VortiQa application software
  - VortiQa application identification software (AIS)
  - Enterprise software for networking
  - VortiQa open network switch software
  - VortiQa open network director software

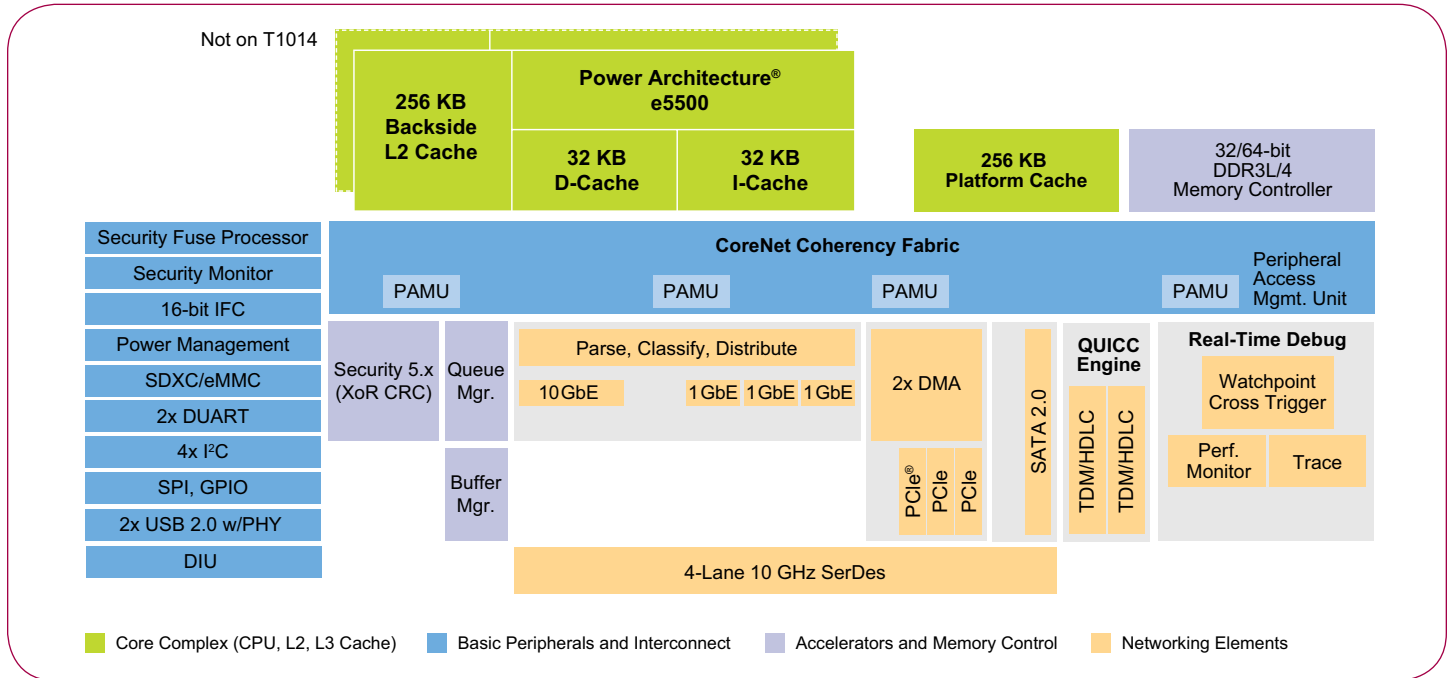


- ▶ Professional services and support
  - Commercial services
  - Linux SDK support package
  - Reference design software (RDS) support package
- ▶ Third-party software and tools
  - Enea, Green Hills, Mentor Graphics and Wind River

### QorIQ P1020 AND T102X PROCESSORS COMPARISON TABLE

	P1020/11	T1023/13	T1024/14	T1042
<b>Core</b>	1-2 x e500v2	1-2 x e5500	1-2 x e5500	4 x e5500
<b>Power ISA</b>	32-bit	64-bit	64-bit	64-bit
<b>Max MHz</b>	800	1400	1400	1400
<b>L2 Backside Cache</b>	–	256 KB	256 KB	256 KB
<b>Platform Cache</b>	256 KB	256 KB	256 KB	256 KB
<b>DDR Type and Speed</b>	2/3 1333MTs	3L/4 1600MTs	3L/4 1600MTs	3L/4 1600MTs
<b>DDR Speed</b>	to 1333MTs	to 1600MTs	to 1600MTs	to 1600MTs
<b>DDR Width</b>	36 b	36 b	36 b/72 b	36 b/72 b
<b>SerDes</b>	4	4	4	8
<b>PCIe Lanes</b>	2 x 1 v1	3 x 1 v2	3 x 1 v2	4 x 1 v2
<b>GbE</b>	up to 3	up to 4	up to 4	up to 5
<b>10GbE I/O</b>	–	1	1	–
<b>MACSEC</b>	–	All ports	All ports	All ports
<b>Hardware Offload</b>	–	DPAA	DPAA	DPAA
<b>Crypto</b>	SEC 3.x	SEC 5.x	SEC 5.x	SEC 5.x
<b>Pattern Matching</b>	–	–	–	Yes
<b>QUICC Engine TDM/HDLC, ISDN, Industrial</b>	Yes	–	Yes	Yes
<b>SATA</b>	–	2.0 x 1	2.0 x 1	2.0 x 2
<b>USB</b>	2.0 x 2	2.0 x 2 w Phy	2.0 x 2 w Phy	2.0 x 2 w Phy
<b>Lossless Deep Sleep</b>	–	–	Yes	Yes
<b>Auto Response</b>	–	–	Yes	Yes
<b>Display Interface</b>	–	–	Yes	Yes
<b>Single Clock Source</b>	–	Yes	Yes	Yes
<b>Package</b>	31 x 31 PBGA	19 x 19 FCBGA	23 x 23 FCBGA	23 x 23 FCBGA
<b>Pin Compatible</b>	No	No	Yes	Yes

### QORIQ T1014 AND T1024 COMMUNICATIONS PROCESSOR



## QorIQ T1023/24 PROCESSORS FEATURES LIST

Two or four e5500 single-threaded cores built on Power Architecture technology	<ul style="list-style-type: none"> <li>• Up to 1.4 GHz with 64-bit ISA support</li> <li>• Low latency, per core, core clocked 256 KB dedicated cache</li> <li>• Hybrid 32-bit mode to support legacy software and transition to a 64-bit architecture</li> <li>• Nap, wait and doze low-power modes</li> </ul>
CoreNet platform cache	<ul style="list-style-type: none"> <li>• 256 KB shared platform cache for stashing support</li> </ul>
Hierarchical interconnect fabric	<ul style="list-style-type: none"> <li>• CoreNet fabric supporting coherent and non-coherent transactions with prioritization and bandwidth allocation amongst CoreNet endpoints</li> <li>• QMAN fabric supporting packet-level queue management and quality of service</li> </ul>
64-bit DDR3L/4 SDRAM memory controller with ECC support	<ul style="list-style-type: none"> <li>• 32-bit or 64-bit low power DDR up to 1600 MT/s</li> </ul>
DPAA incorporating acceleration for the following functions	<ul style="list-style-type: none"> <li>• Full L2/3 tunneling and en/decrypt offload support for functions such as WLAN</li> <li>• CAPWAP/DTLS secure wired links</li> <li>• Packet parsing, classification and distribution</li> <li>• Queue management for scheduling, packet sequencing and congestion management</li> <li>• Hardware buffer management for buffer allocation and de-allocation</li> <li>• Cryptography acceleration (SEC 5.x)</li> </ul>
SerDes	<ul style="list-style-type: none"> <li>• Four lanes at up to 10 Gbit/s</li> <li>• Supports SGMII, 2.5 Gbit SGMII, QSGMII, XFI, 10G BASE-KR, PCI Express® and SATA</li> </ul>
Ethernet interfaces	<ul style="list-style-type: none"> <li>• Up to 4 x Ethernet MACs</li> </ul>
QUICC Engine module	<ul style="list-style-type: none"> <li>• Integrated support for legacy WAN protocols TDM, HDLC, UART, ISDN and industrial protocols</li> </ul>
High-speed peripheral interfaces	<ul style="list-style-type: none"> <li>• Three PCI Express 2.0 controller</li> </ul>
Additional peripheral interfaces	<ul style="list-style-type: none"> <li>• One serial ATA (SATA 2.0) controller</li> <li>• Two high-speed USB 2.0 controllers with integrated PHYs</li> <li>• Enhanced secure digital host controller (SD/MMC/eMMC)</li> <li>• Enhanced serial peripheral interface</li> <li>• Two I<sup>2</sup>C controllers</li> <li>• Four UARTS</li> <li>• Integrated flash controller supporting NAND and NOR flash memory</li> </ul>
DMA	<ul style="list-style-type: none"> <li>• Dual four channel</li> </ul>
Support for hardware virtualization and partitioning enforcement	<ul style="list-style-type: none"> <li>• Extra privileged level for hypervisor support</li> </ul>
QorIQ trust architecture	<ul style="list-style-type: none"> <li>• Secure boot, secure debug, tamper detection, volatile key storage</li> </ul>
Single source clocking	<ul style="list-style-type: none"> <li>• For BOM cost reduction</li> </ul>

[www.nxp.com/QorIQ](http://www.nxp.com/QorIQ)

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