Features

- ***Single Package Fully-integrated 4-bit Microcontroller with RF Transmitter***
- ***Low Power Consumption in Sleep Mode (< 1 µA Typically)***
- ***Flash Controller for Application Program Available***
- ***Maximum Output Power (10 dBm) with Low Supply Current (9.5 mA Typically)***
- ***2.0 V to 4.0 V Operation Voltage for Single Li-cell Power Supply***
- ***-40°C to +125°C Operation Temperature***
- ***SSO24 Package***
- ***About Seven External Components***

Microcontroller with UHF ASK/FSK Transmitter

T48C862-R3

Preliminary

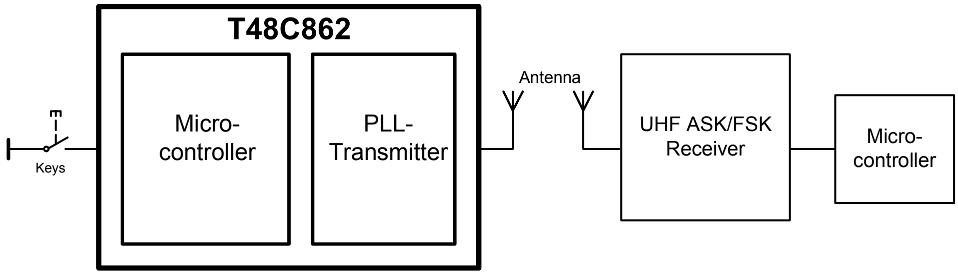
Description

The T48C862-R3 is a single package dual-chip circuit. It combines a UHF ASK/FSK transmitter with a 4-bit microcontroller. It supports highly integrated solutions in car access and tire pressure monitoring applications, as well as manifold applications in the industrial and consumer segment. It is available for the frequency range of 429 MHz to 439 MHz with data rates up to 32 kbaud.

For further frequency ranges such as 310 MHz to 330 MHz and 868 MHz to 928 MHz separate data sheets are available.

The device contains a flash microcontroller.

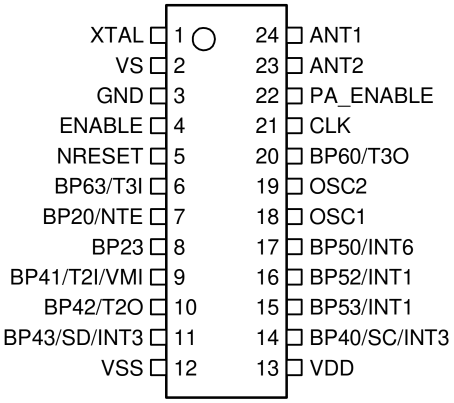
Figure 1. Application Diagram



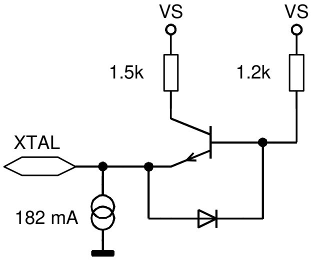
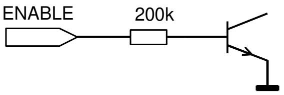
Rev. 4554A–4BMCU–02/03

Pin Configuration

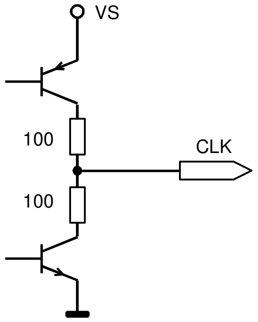
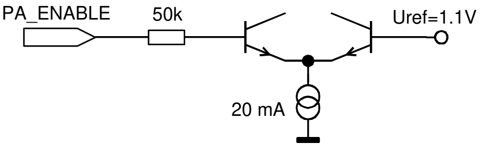
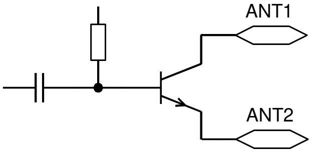
Figure 2. Pinning SSO24



Pin Description: RF Part

Pin	Symbol	Function	Configuration
1	XTAL	Connection for crystal	
2	VS	Supply voltage	ESD protection circuitry (see Figure 8)
3	GND	Ground	ESD protection circuitry (see Figure 8)
4	ENABLE	Enable input	

Pin Description: RF Part (Continued)

Pin	Symbol	Function	Configuration
21	CLK	Clock output signal for microcontroller The clock output frequency is set by the crystal to $f_{XTAL}/4$.	
22	PA_ENABLE	Switches on power amplifier, used for ASK modulation	
23	ANT2	Emitter of antenna output stage	
24	ANT1	Open collector antenna output	

Pin Description: Microcontroller Part

Name	Type	Function	Alternate Function	Pin No.	Reset State
V_{DD}	–	Supply voltage	–	13	NA
V_{SS}	–	Circuit ground	–	12	NA
BP20	I/O	Bi-directional I/O line of Port 2.0	NTE-test mode enable, see also section "Master Reset"	7	Input
BP40	I/O	Bi-directional I/O line of Port 4.0	SC-serial clock or INT3 external interrupt input	14	Input
BP41	I/O	Bi-directional I/O line of Port 4.1	VMI voltage monitor input or T2I external clock input Timer 2	9	Input
BP42	I/O	Bi-directional I/O line of Port 4.2	T2O Timer 2 output	10	Input
BP43	I/O	Bi-directional I/O line of Port 4.3	SD serial data I/O or INT3-external interrupt input	11	Input
BP50	I/O	Bi-directional I/O line of Port 5.0	INT6 external interrupt input	17	Input
BP52	I/O	Bi-directional I/O line of Port 5.2	INT1 external interrupt input	16	Input
BP53	I/O	Bi-directional I/O line of Port 5.3	INT1 external interrupt input	15	Input
BP60	I/O	Bi-directional I/O line of Port 6.0	T3O Timer 3 output	20	Input
BP63	I/O	Bi-directional I/O line of Port 6.3	T3I Timer 3 input	6	Input
OSC1	I	Oscillator input	4-MHz crystal input or 32-kHz crystal input or external clock input or external trimming resistor input	18	Input
OSC2	O	Oscillator output	4-MHz crystal output or 32-kHz crystal output or external clock input	19	Input
NRESET	I/O	Bi-directional reset pin	–	5	I/O

UHF ASK/FSK Transmitter Block

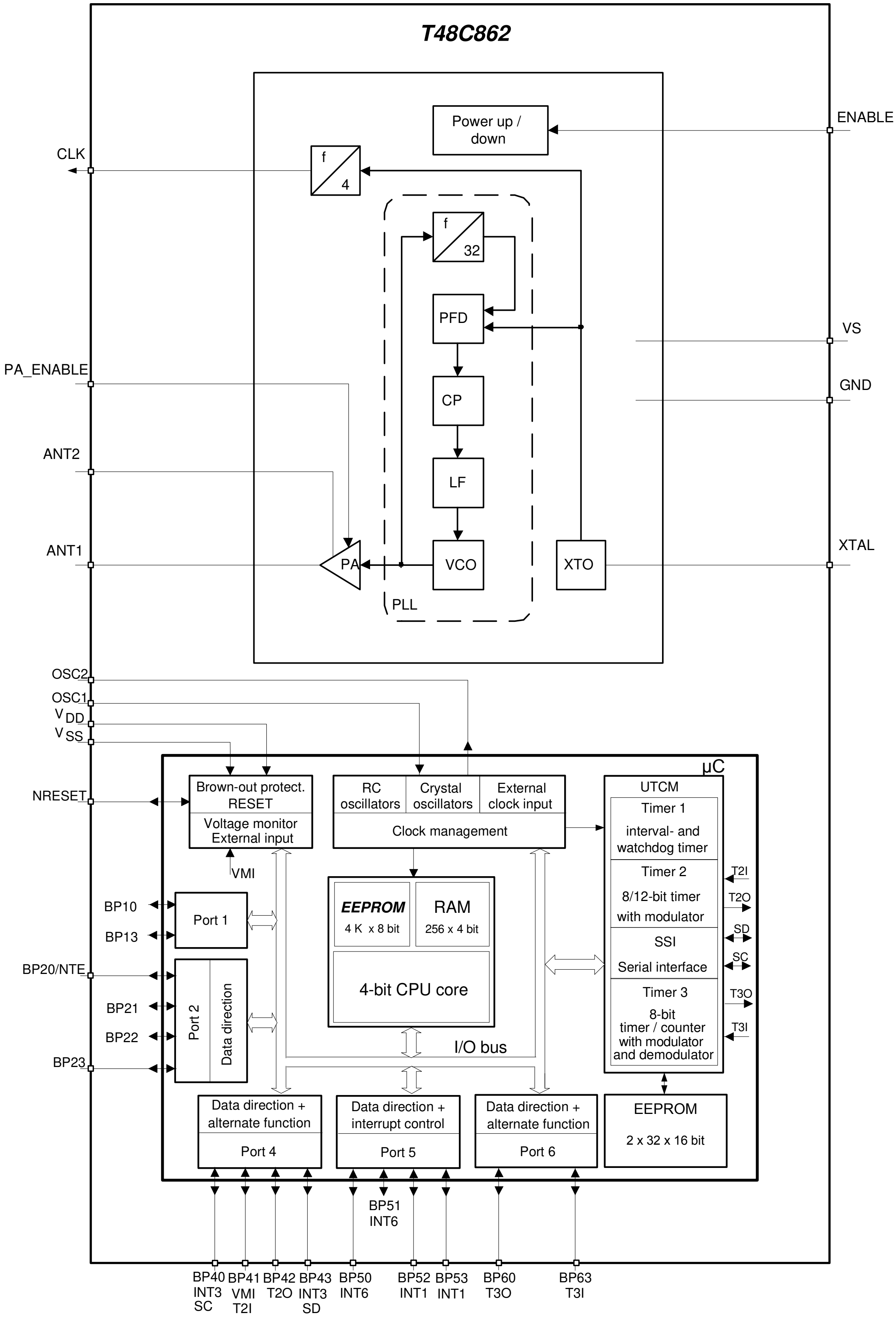
Features

- *Integrated PLL Loop Filter*
- *ESD Protection (4 kV HBM/200 V MM, Except Pin 2: 4 kV HBM/100 V MM) also at ANT1/ANT2*
- *High Output Power (8 dBm) with Low Supply Current (9.0 mA)*
- *Modulation Scheme ASK/FSK*
  - *FSK Modulation is Achieved by Connecting an Additional Capacitor between the XTAL Load Capacitor and the Open-drain Output of the Modulating Microcontroller*
- *Easy to Design-in Due to Excellent Isolation of the PLL from the PA and Power Supply*
- *Single Li-cell for Power Supply*
- *Supply Voltage 2.0 V to 4.0 V in the Temperature Range of -40°C to +85°C/+125°C*
- *Single-ended Antenna Output with High Efficient Power Amplifier*
- *CLK Output for Clocking the Microcontroller*
- *One-chip Solution with Minimum External Circuitry*
- *125°C Operation for Tire Pressure Systems*

Description

The PLL transmitter block has been developed for the demands of RF low-cost transmission systems, at data rates up to 32 kbaud. The transmitting frequency range is 310 MHz to 330 MHz. It can be used in both FSK and ASK systems.

Figure 3. Block Diagram



General Description

This fully-integrated PLL transmitter that allows particularly simple, low-cost RF miniature transmitters to be assembled. The VCO is locked to 32 f_{XTAL}, thus, a 9.8438 MHz crystal is needed for a 315 MHz transmitter. All other PLL and VCO peripheral elements are integrated.

The XTO is a series resonance oscillator so that only one capacitor together with a crystal connected in series to GND are needed as external elements.

The crystal oscillator together with the PLL needs maximum <1 ms until the PLL is locked and the CLK output is stable. A wait time of ≥ 1 ms until the CLK is used for the microcontroller and the PA is switched on.

The power amplifier is an open-collector output delivering a current pulse which is nearly independent from the load impedance. The delivered output power is controlled via the connected load impedance.

This output configuration enables a simple matching to any kind of antenna or to 50 Ω. A high power efficiency of $\eta = P_{out}/(I_{S,PA}\ V_S)$ of 40% for the power amplifier results when an optimized load impedance of Z_{Load} = (255 + j192) Ω is used at 3 V supply voltage.

Functional Description

If ENABLE = L and PA_ENABLE = L, the circuit is in standby mode consuming only a very small amount of current so that a lithium cell used as power supply can work for several years.

With ENABLE = H, the XTO, PLL and the CLK driver are switched on. If PA_ENABLE remains L, only the PLL and the XTO are running and the CLK signal is delivered to the microcontroller. The VCO locks to 32 times the XTO frequency.

With ENABLE = H and PA_ENABLE = H, the PLL, XTO, CLK driver and the power amplifier are on. With PA_ENABLE, the power amplifier can be switched on and off, which is used to perform the ASK modulation.

ASK Transmission

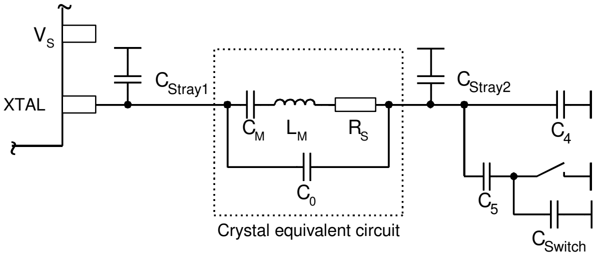
The PLL transmitter block is activated by ENABLE = H. PA_ENABLE must remain L for t ≥ 1 ms, then the CLK signal can be taken to clock the microcontroller and the output power can be modulated by means of pin PA_ENABLE. After transmission, PA_ENABLE is switched to L and the microcontroller switches back to internal clocking. The PLL transmitter block is switched back to standby mode with ENABLE = L.

FSK Transmission

The PLL transmitter block is activated by ENABLE = H. PA_ENABLE must remain L for t ≥ 1 ms, then the CLK signal can be taken to clock the microcontroller and the power amplifier is switched on with PA_ENABLE = H. The chip is then ready for FSK modulation. The microcontroller starts to switch on and off the capacitor between the XTAL load capacitor and GND with an open-drain output port, thus changing the reference frequency of the PLL. If the switch is closed, the output frequency is lower than if the switch is open. After transmission PA_ENABLE is switched to L and the microcontroller switches back to internal clocking. The PLL transmitter block is switched back to standby mode with ENABLE = L.

The accuracy of the frequency deviation with XTAL pulling method is about ±25% when the following tolerances are considered.

Figure 4. Tolerances of Frequency Modulation



Using C_4 = 8.2 pF ±5%, C_5 = 10 pF ±5%, a switch port with C_{Switch} = 3 pF ±10%, stray capacitances on each side of the crystal of C_{Stray1} = C_{Stray2} = 1 pF ±10%, a parallel capacitance of the crystal of C_0 = 3.2 pF ±10% and a crystal with C_M = 13 fF ±10%, an FSK deviation of ±21.5 kHz typical with worst case tolerances of ±16.25 kHz to ±28.01 kHz results.

CLK Output

An output CLK signal is provided for a connected microcontroller, the delivered signal is CMOS compatible if the load capacitance is lower than 10 pF.

Clock Pulse Take Over

The clock of the crystal oscillator can be used for clocking the microcontroller. Atmel's M4xCx9x has the special feature of starting with an integrated RC-oscillator to switch on the PLL transmitter block with ENABLE = H, and after 1 ms to assume the clock signal of the transmission IC, so the message can be sent with crystal accuracy.

Output Matching and Power Setting

The output power is set by the load impedance of the antenna. The maximum output power is achieved with a load impedance of $Z_{Load,opt}$ = (255 + j192) Ω. There must be a low resistive path to V_S to deliver the DC current.

The delivered current pulse of the power amplifier is 9 mA and the maximum output power is delivered to a resistive load of 400 Ω if the 1.0 pF output capacitance of the power amplifier is compensated by the load impedance.

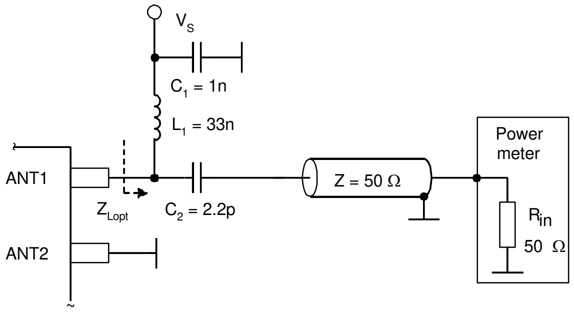
An optimum load impedance of:
Z_{Load} = 400 Ω || j/(2 × π 1.0 pF) = (255 + j192) Ω thus results for the maximum output power of 8 dBm.

The load impedance is defined as the impedance seen from the PLL transmitter block's ANT1, ANT2 into the matching network. Do not confuse this large signal load impedance with a small signal input impedance delivered as input characteristic of RF amplifiers and measured from the application into the IC instead of from the IC into the application for a power amplifier.

Less output power is achieved by lowering the real parallel part of 400 Ω where the parallel imaginary part should be kept constant.

Output power measurement can be done with the circuit shown in Figure 5. Note that the component values must be changed to compensate the individual board parasitics until the PLL transmitter block has the right load impedance $Z_{Load,opt}$ = (255 + j192) Ω. Also the damping of the cable used to measure the output power must be calibrated.

Figure 5. Output Power Measurement



Application Circuit

For the supply-voltage blocking capacitor C_3, a value of 68 nF/X7R is recommended (see Figure 6 and Figure 7). C_1 and C_2 are used to match the loop antenna to the power amplifier where C_1 typically is 22 pF/NP0 and C_2 is 10.8 pF/NP0 (18 pF + 27 pF in series); for C_2 two capacitors in series should be used to achieve a better tolerance value and to have the possibility to realize the $Z_{Load,opt}$ by using standard valued capacitors.

C_1 forms together with the pins of PLL transmitter block and the PCB board wires a series resonance loop that suppresses the 1^{st} harmonic, thus, the position of C_1 on the PCB is important. Normally the best suppression is achieved when C_1 is placed as close as possible to the pins ANT1 and ANT2.

The loop antenna should not exceed a width of 1.5 mm, otherwise the Q-factor of the loop antenna is too high.

L_1 (50 nH to 100 nH) can be printed on PCB. C_4 should be selected so the XTO runs on the load resonance frequency of the crystal. Normally, a value of 12 pF results for a 15 pF load-capacitance crystal.

Figure 6. ASK Application Circuit

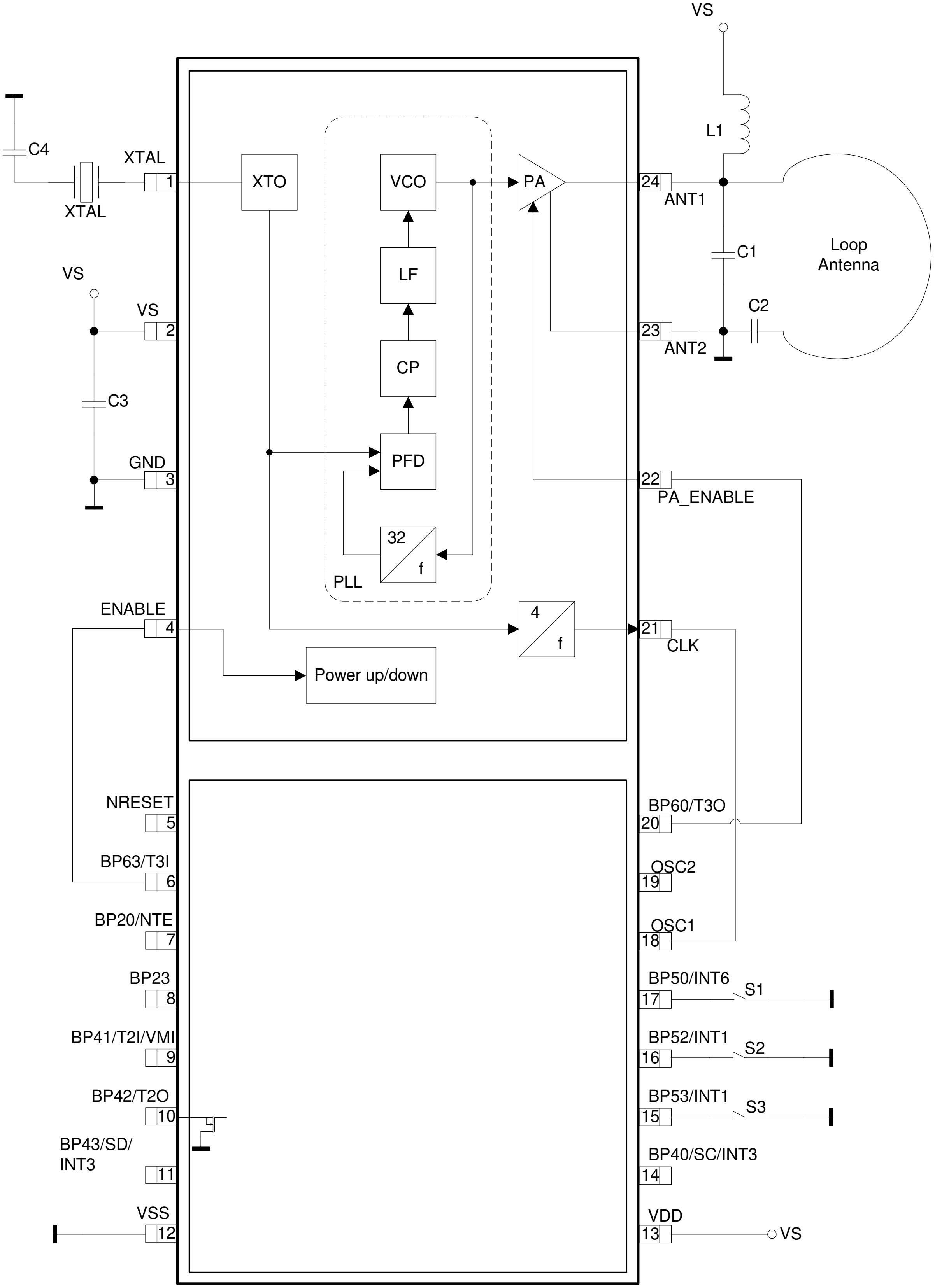


Figure 7. FSK Application Circuit

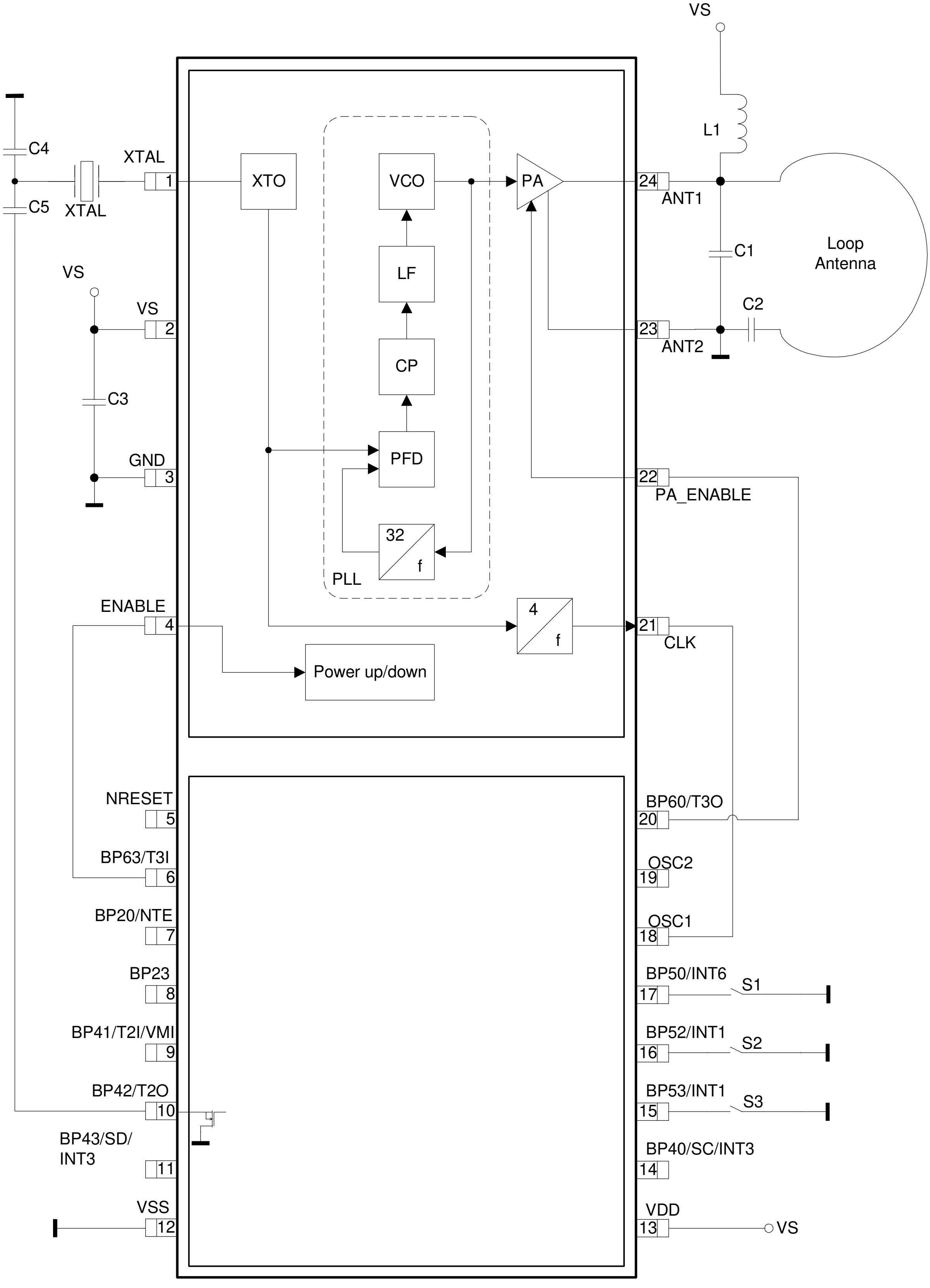
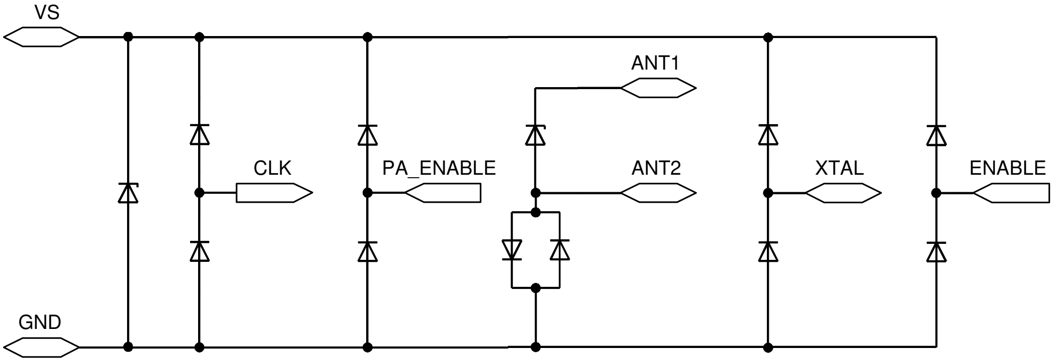


Figure 8. ESD Protection Circuit



Absolute Maximum Ratings

Parameters	**Symbol**	**Min.**	**Max.**	**Unit**
Supply voltage	V_S		5	V
Power dissipation	P_{tot}		100	mW
Junction temperature	T_j		150	°C
Storage temperature	T_{stg}	-55	+125	°C
Ambient temperature	T_{amb}	-55	+125	°C

Thermal Resistance

Parameters	**Symbol**	**Value**	**Unit**
Junction ambient	R_{thJA}	170	K/W

Electrical Characteristics

V_S = 2.0 V to 4.0 V, T_{amb} = -40°C to +125°C, unless otherwise specified.
Typical values are given at V_S = 3.0 V and T_{amb} = 25°C. All parameters are referred to GND (Pin 7).

Parameters	**Test Conditions**	**Symbol**	**Min.**	**Typ.**	**Max.**	**Unit**
Supply current	Power down, V_{ENABLE} < 0.25 V, -40°C to +85°C $V_{PA\text{-}ENABLE}$ < 0.25 V, -85°C to +125°C $V_{PA\text{-}ENABLE}$ < 0.25 V, 25°C (100% correlation tested)	I_{S_Off}		<10	350 7	nA µA nA
Supply current	Power up, PA off, V_S = 3 V V_{ENABLE} > 1.7 V, $V_{PA\text{-}ENABLE}$ < 0.25 V	I_S		3.7	4.8	mA
Supply current	Power up, V_S = 3.0 V V_{ENABLE} > 1.7 V, $V_{PA\text{-}ENABLE}$ > 1.7 V	$I_{S\_Transmit}$		9	11.6	mA
Output power	V_S = 3.0 V, T_{amb} = 25°C f = 315 MHz, Z_{Load} = (255 + j192) Ω	P_{Ref}	6.0	8.0	10.5	dBm

Electrical Characteristics (Continued)

V_S = 2.0 V to 4.0 V, T_{amb} = -40°C to +125°C, unless otherwise specified.
Typical values are given at V_S = 3.0 V and T_{amb} = 25°C. All parameters are referred to GND (Pin 7).

Parameters	*Test Conditions*	*Symbol*	*Min.*	*Typ.*	*Max.*	*Unit*
Output power variation for the full temperature range	T_{amb} = -40°C to +85°C V_S = 3.0 V V_S = 2.0 V	ΔP_{Ref} ΔP_{Ref}			-1.5 -4.0	dB dB
Output power variation for the full temperature range	T_{amb} = -40°C to +125°C V_S = 3.0 V V_S = 2.0 V $P_{Out} = P_{Ref} + \Delta P_{Ref}$	ΔP_{Ref} ΔP_{Ref}			-2.0 -4.5	dB dB
Achievable output-power range	Selectable by load impedance	P_{Out_typ}	0		8.0	dBm
Spurious emission	$f_{CLK} = f_0/128$ Load capacitance at Pin CLK = 10 pF $f_O \pm 1\times f_{CLK}$ $f_O \pm 4 \times f_{CLK}$ other spurious are lower			-55 -52		dBc dBc
Oscillator frequency XTO (= phase comparator frequency)	$f_{XTO} = f_0/32$ f_{XTAL} = resonant frequency of the XTAL, $C_M \leq$ 10 fF, load capacitance selected accordingly T_{amb} = -40°C to +85°C T_{amb} = -40°C to +125°C	f_{XTO}	-30 -40	f_{XTAL}	+30 +40	ppm ppm
PLL loop bandwidth				250		kHz
Phase noise of phase comparator	Referred to $f_{PC} = f_{XT0,}$ 25 kHz distance to carrier			-116	-110	dBc/Hz
In loop phase noise PLL	25 kHz distance to carrier			-86	-80	dBc/Hz
Phase noise VCO	at 1 MHz at 36 MHz			-94 -125	-90 -121	dBc/Hz dBc/Hz
Frequency range of VCO		f_{VCO}	310		330	MHz
Clock output frequency (CMOS microcontroller compatible)				f_0/128		MHz
Voltage swing at Pin CLK	$C_{Load} \leq$ 10 pF	V_{0h} V_{0l}	$V_S \times 0.8$		$V_S \times 0.2$	V V
Series resonance R of the crystal		Rs			110	Ω
Capacitive load at Pin XT0					7	pF
FSK modulation frequency rate	Duty cycle of the modulation signal = 50%		0		32	kHz
ASK modulation frequency rate	Duty cycle of the modulation signal = 50%		0		32	kHz
ENABLE input	Low level input voltage High level input voltage Input current high	V_{Il} V_{Ih} I_{In}	1.7		0.25 20	V V µA
PA_ENABLE input	Low level input voltage High level input voltage Input current high	V_{Il} V_{Ih} I_{In}	1.7		0.25 5	V V µA

Microcontroller Block

Features

- ***4-Kbyte ROM, 256 x 4-bit RAM***
- ***EEPROM Programmable Options***
- ***Read Protection for the EEPROM Program Memory***
- ***16 Bi-directional I/Os***
- ***Up to Seven External/Internal Interrupt Sources***
- ***Eight Hardware and Software Interrupt Priorities***
- ***Multifunction Timer/Counter***
  - IR Remote Control Carrier Generator
  - Biphase-, Manchester- and Pulse-width Modulator and Demodulator
  - Phase Control Function
- ***Programmable System Clock with Prescaler and Five Different Clock Sources***
- ***Very Low Sleep Current (< 1 µA)***
- ***2 × 512-bBit EEPROM Data Memory***
- ***256 × 4-bit RAM Data Memory***
- ***Synchronous Serial Interface (2-wire, 3-wire)***
- ***Watchdog, POR and Brown-out Function***
- ***Voltage Monitoring Inclusive Lo_BAT Detect***

Description

The microcontroller is designed with EEPROM cells so it can be programmed several times. To offer full compatibility with each ROM version, the I/O configuration is stored into a separate internal EEPROM block during programming. The configuration is downloaded to the I/Os with every power-on reset.

Introduction

The microcontroller block is a member of Atmel's family of 4-bit single-chip microcontrollers. Instead of ROM it contains EEPROM, RAM, parallel I/O ports, two 8-bit programmable multifunction timer/counters, voltage supervisor, interval timer with watchdog function and a sophisticated on-chip clock generation with integrated RC-, 32-kHz and 4-MHz crystal oscillators.

Differences between T48C862-R3 and ATAR862 Microcontrollers

Program Memory

The program memory of the devices is realized as an EEPROM. The memory size for user programs is 4096 bytes. It is programmed as 258 × 16 bytes blocks of data. the implement LOCK-bit function is user-selectable and protects the device from unauthorized read-out of the program memory.

Configuration Memory

An additional area of 32 bytes of the EEPROM is used to store information about the hardware configuration. All the options that are selectable for the ROM versions are available to the user. This includes not only the different port options but also the possibilities to select different capacitors for OSC1 and OSC2, the option to enable or disable the hardlock for the watchdog, the option to select OSC2 instead of OSC1 as external clock input and the option to enable the external clock monitor as a reset source.

Data Memory

The microcontroller block contains an internal data EEPROM that is organized as two pages of 32 × 16-bit. To be compatible with the ROM parts, the page used has to be defined within the application software by writing the 2-wire interface (TWI) command "09h" to the EEPROM. This command has no effect for the microcontroller block, if it is left inside the HEX-file for the ROM version. Also for compatibility reasons, the access to the EEPROM is handled via the MCL (serial interface) as in the corresponding ROM parts.

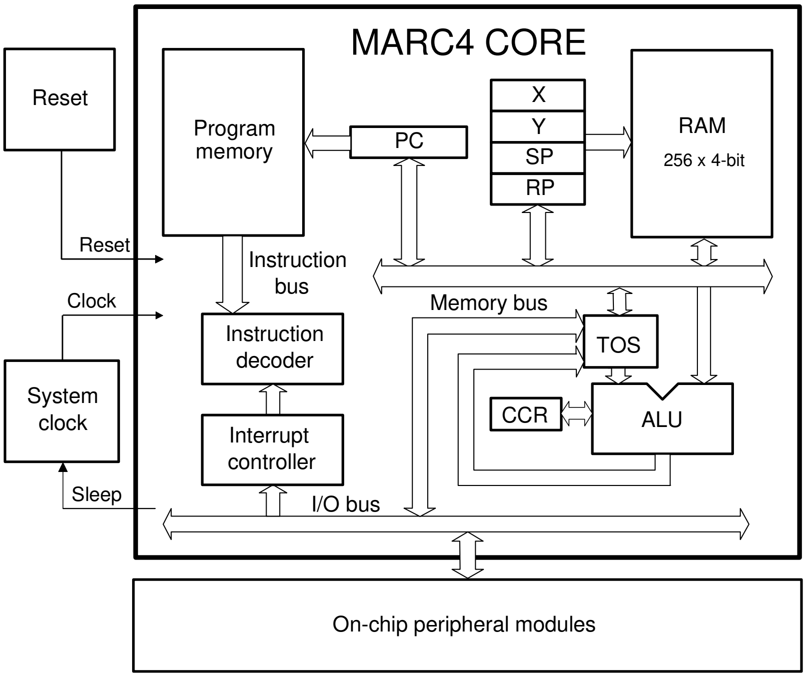
Reset Function

During each reset (power-on or brown-out), the I/O configuration is deleted and reloaded with the data from the configuration memory. This leads to a slightly different behavior compared to the ROM versions. Both devices switch their I/Os to input during reset but the ROM part has the mask selected pull-up or pull-down resistors active while the MTP has them removed until the download is finished.

Microcontroller Architecture General Description

The microcontroller consists of an advanced stack-based, 4-bit CPU core and on-chip peripherals. The CPU is based on the Harvard architecture with physically separated program memory (ROM) and data memory (RAM). Three independent buses, the instruction bus, the memory bus and the I/O bus, are used for parallel communication between ROM, RAM and peripherals. This enhances program execution speed by allowing both instruction prefetching, and a simultaneous communication to the on-chip peripheral circuitry. The extremely powerful integrated interrupt controller with associated eight prioritized interrupt levels supports fast and efficient processing of hardware events. The microcontroller is designed for the high-level programming language qFORTH. The core includes both an expression and a return stack. This architecture enables high-level language programming without any loss of efficiency or code density.

Figure 9. Microcontroller Core



Components of Microcontroller Core

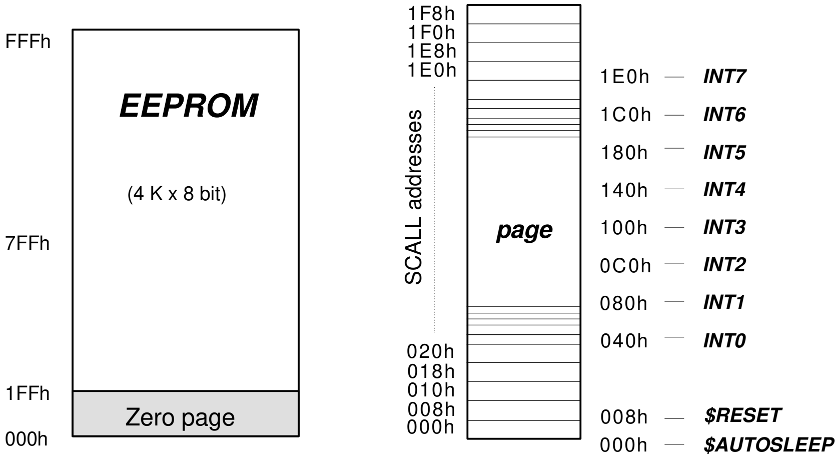
The core contains ROM, RAM, ALU, program counter, RAM address registers, instruction decoder and interrupt controller. The following sections describe each functional block in more detail.

Program Memory

The program memory (EEPROM) is programmable with the customer application program during the fabrication of the microcontroller. The EEPROM is addressed by a 12-bit wide program counter, thus predefining a maximum program bank size of 4-Kbytes. The lowest user program memory address segment is taken up by a 512 bytes Zero page which contains predefined start addresses for interrupt service routines and special subroutines accessible with single byte instructions (SCALL).

The corresponding memory map is shown in Figure 4. Look-up tables of constants can also be held in ROM and are accessed via the microcontrollers' built-in table instruction.

Figure 10. ROM Map of the Microcontroller Block



RAM

The microcontroller block contains a 256 x 4-bit wide static random access memory (RAM), which is used for the expression stack. The return stack and data memory are used for variables and arrays. The RAM is addressed by any of the four 8-bit wide RAM address registers SP, RP, X and Y.

Expression Stack

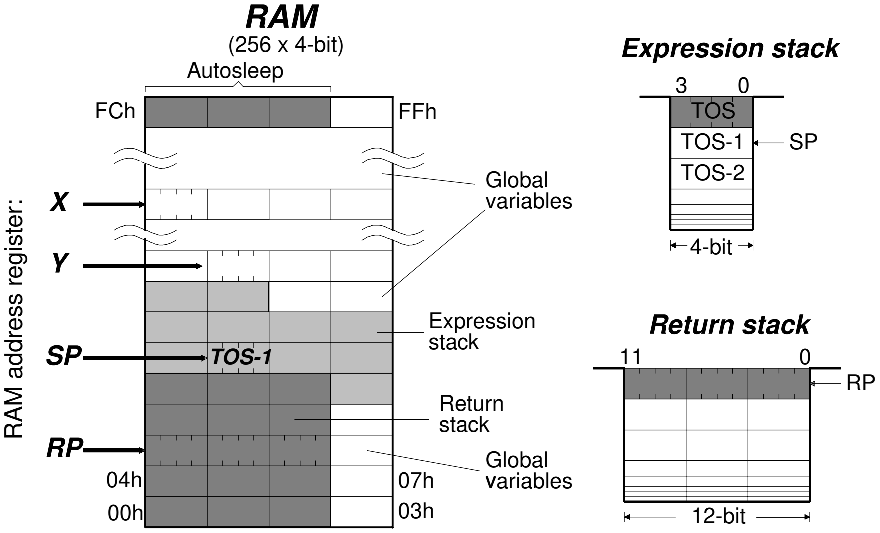
The 4-bit wide expression stack is addressed with the expression stack pointer (SP). All arithmetic, I/O and memory reference operations take their operands, and return their results to the expression stack. The microcontroller performs the operations with the top of stack items (TOS and TOS-1). The TOS register contains the top element of the expression stack and works in the same way as an accumulator. This stack is also used for passing parameters between subroutines and as a scratch pad area for temporary storage of data.

Return Stack

The 12-bit wide return stack is addressed by the return stack pointer (RP). It is used for storing return addresses of subroutines, interrupt routines and for keeping loop index counts. The return stack can also be used as a temporary storage area.

The microcontroller instruction set supports the exchange of data between the top elements of the expression stack and the return stack. The two stacks within the RAM have a user definable location and maximum depth.

Figure 11. RAM Map



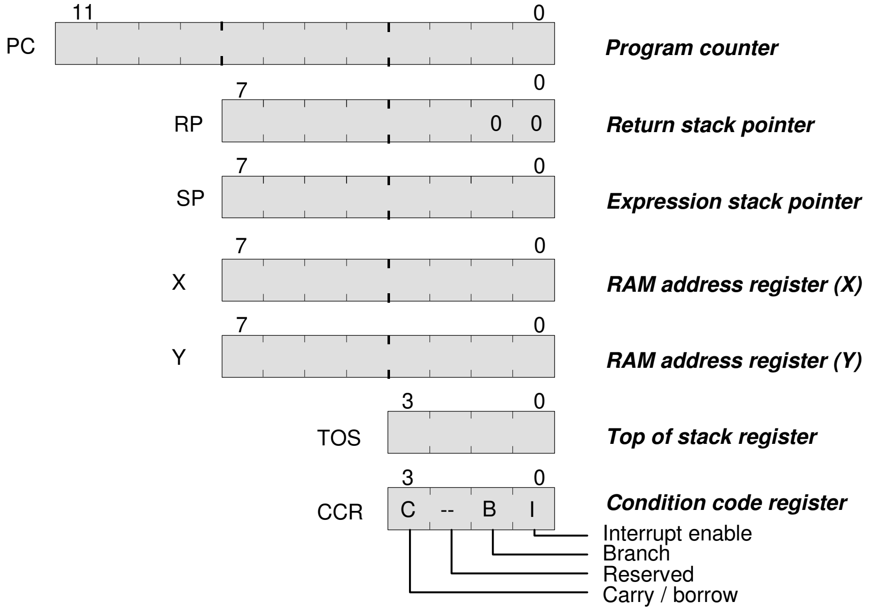
Registers

The microcontroller has seven programmable registers and one condition code register (seeFigure 12).

Program Counter (PC)

The program counter is a 12-bit register which contains the address of the next instruction to be fetched from the EEPROM. Instructions currently being executed are decoded in the instruction decoder to determine the internal micro-operations. For linear code (no calls or branches), the program counter is incremented with every instruction cycle. If a branch-, call-, return-instruction or an interrupt is executed, the program counter is loaded with a new address. The program counter is also used with the table instruction to fetch 8-bit wide EEPROM constants.

Figure 12. Programming Mode I



RAM Address Registers

The RAM is addressed with the four 8-bit wide RAM address registers: SP, RP, X and Y. These registers allow access to any of the 256 RAM nibbles.

Expression Stack Pointer (SP)

The stack pointer contains the address of the next-to-top 4-bit item (TOS-1) of the expression stack. The pointer is automatically pre-incremented if a nibble is moved onto the stack or post-decremented if a nibble is removed from the stack. Every post-decrement operation moves the item (TOS-1) to the TOS register before the SP is decremented. After a reset, the stack pointer has to be initialized with >SP S0 to allocate the start address of the expression stack area.

Return Stack Pointer (RP)

The return stack pointer points to the top element of the 12-bit wide return stack. The pointer automatically pre-increments if an element is moved onto the stack, or it post-decrements if an element is removed from the stack. The return stack pointer increments and decrements in steps of 4. This means that every time a 12-bit element is stacked, a 4-bit RAM location is left unwritten. This location is used by the qFORTH compiler to allocate 4-bit variables. After a reset the return stack pointer has to be initialized via >RP FCh.

RAM Address Registers (X and Y)

The X and Y registers are used to address any 4-bit item in the RAM. A fetch operation moves the addressed nibble onto the TOS. A store operation moves the TOS to the addressed RAM location. By using either the pre-increment or post-decrement addressing mode arrays in the RAM can be compared, filled or moved.

Top of Stack (TOS)

The top of stack register is the accumulator of the microcontroller block. All arithmetic/logic, memory reference and I/O operations use this register. The TOS register receives data from the ALU, EEPROM, RAM or I/O bus.

Condition Code Register (CCR)

The 4-bit wide condition code register contains the branch, the carry and the interrupt enable flag. These bits indicate the current state of the CPU. The CCR flags are set or reset by ALU operations. The instructions SET_BCF, TOG_BF, CCR! and DI allow direct manipulation of the condition code register.

Carry/Borrow (C)

The carry/borrow flag indicates that the borrowing or carrying out of arithmetic logic unit (ALU) occurred during the last arithmetic operation. During shift and rotate operations, this bit is used as a fifth bit. Boolean operations have no effect on the C-flag.

Branch (B)

The branch flag controls the conditional program branching. Should the branch flag has been set by a previous instruction, a conditional branch will cause a jump. This flag is affected by arithmetic, logic, shift, and rotate operations.

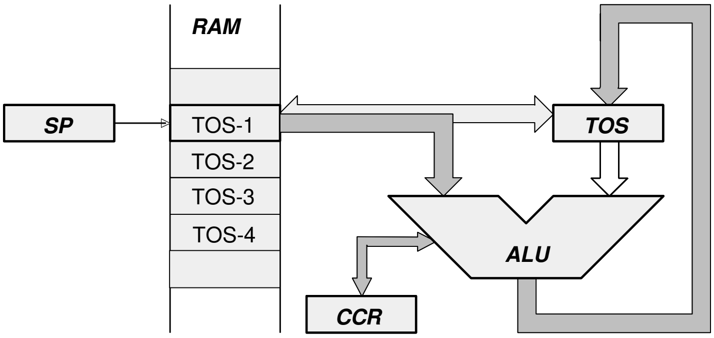
Interrupt Enable (I)

The interrupt enable flag globally enables or disables the triggering of all interrupt routines with the exception of the non-maskable reset. After a reset or while executing the DI instruction, the interrupt enable flag is reset, thus disabling all interrupts. The core will not accept any further interrupt requests until the interrupt enable flag has been set again by either executing an EI or SLEEP instruction.

ALU

The 4-bit ALU performs all the arithmetic, logical, shift and rotate operations with the top two elements of the expression stack (TOS and TOS-1) and returns the result to the TOS. The ALU operations affects the carry/borrow and branch flag in the condition code register (CCR).

Figure 13. ALU Zero-address Operations



I/O Bus

The I/O ports and the registers of the peripheral modules are I/O mapped. All communication between the core and the on-chip peripherals take place via the I/O bus and the associated I/O control. With the microcontroller IN and OUT instructions, the I/O bus allows a direct read or write access to one of the 16 primary I/O addresses. More about the I/O access to the on-chip peripherals is described in the section “Peripheral Modules”. The I/O bus is internal and is not accessible by the customer on the final microcontroller device, but it is used as the interface for the microcontroller emulation (see also the section “Emulation”).

Instruction Set

The microcontroller instruction set is optimized for the high level programming language qFORTH. Many microcontroller instructions are qFORTH words. This enables the compiler to generate a fast and compact program code. The CPU has an instruction pipeline allowing the controller to prefetch an instruction from EEPROM at the same time as the present instruction is being executed. The microcontroller is a zero-address machine, the instructions contain only the operation to be performed and no source or destination address fields. The operations are implicitly performed on the data placed on the stack. There are one- and two-byte instructions which are executed within 1 to 4 machine cycles. A microcontroller machine cycle is made up of two system clock cycles (SYSCL). Most of the instructions are only one byte long and are executed in a single machine cycle. For more information refer to the “MARC4 Programmer’s Guide”.

Interrupt Structure

The microcontroller can handle interrupts with eight different priority levels. They can be generated from the internal and external interrupt sources or by a software interrupt from the CPU itself. Each interrupt level has a hard-wired priority and an associated vector for the service routine in the EEPROM (see Table 1). The programmer can postpone the processing of interrupts by resetting the interrupt enable flag (I) in the CCR. An interrupt occurrence will still be registered, but the interrupt routine only started after the I-flag is set. All interrupts can be masked, and the priority individually software configured by programming the appropriate control register of the interrupting module (see section “Peripheral Modules”).

Interrupt Processing

For processing the eight interrupt levels, the microcontroller includes an interrupt controller with two 8-bit wide interrupt pending and interrupt active registers. The interrupt controller samples all interrupt requests during every non-I/O instruction cycle and latches these in the interrupt pending register. If no higher priority interrupt is present in the interrupt active register, it signals the CPU to interrupt the current program execution. If the interrupt enable bit is set, the processor enters an interrupt acknowledge cycle. During this cycle a short call (SCALL) instruction to the service routine is executed and the current PC is saved on the return stack. An interrupt service routine is completed with the RTI instruction. This instruction resets the corresponding bits in the interrupt pending/active register and fetches the return address from the return stack to the program counter. When the interrupt enable flag is reset (triggering of interrupt routines is disabled), the execution of new interrupt service routines is inhibited but not the logging of the interrupt requests in the interrupt pending register. The execution of the interrupt is delayed until the interrupt enable flag is set again. Note that interrupts are only lost if an interrupt request occurs while the corresponding bit in the pending register is still set (i.e., the interrupt service routine is not yet finished).

It should be noted that automatic stacking of the RBR is not carried out by the hardware and so if ROM banking is used, the RBR must be stacked on the expression stack by the application program and restored before the RTI. After a master reset (power-on, brown-out or watchdog reset), the interrupt enable flag and the interrupt pending and interrupt active register are all reset.

Interrupt Latency

The interrupt latency is the time from the occurrence of the interrupt to the interrupt service routine being activated. This is extremely short (taking between 3 to 5 machine cycles depending on the state of the core).

Figure 14. Interrupt Handling

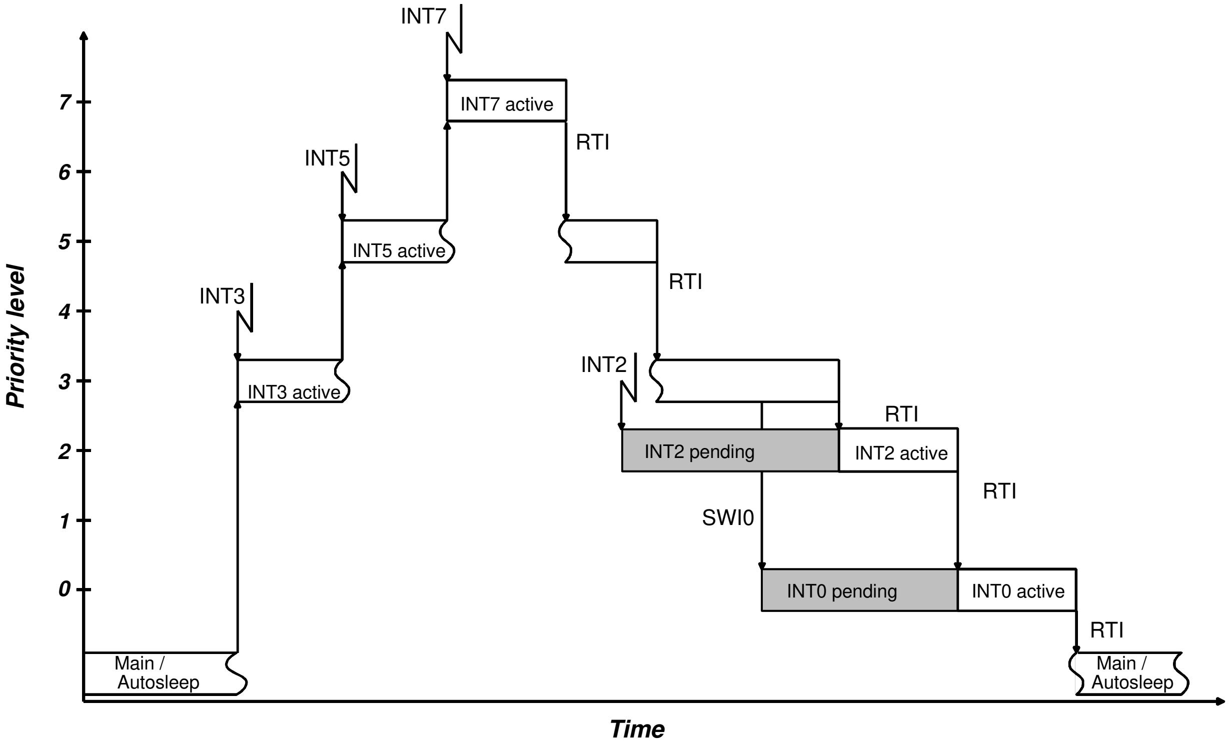


Table 1. Interrupt Priority

Interrupt	Priority	ROM Address	Interrupt Opcode	Function
INT0	Lowest	040h	C8h (SCALL 040h)	Software interrupt (SWI0)
INT1	|	080h	D0h (SCALL 080h)	External hardware interrupt, any edge at BP52 or BP53
INT2	|	0C0h	D8h (SCALL 0C0h)	Timer 1 interrupt
INT3	|	100h	E8h (SCALL 100h)	SSI interrupt or external hardware interrupt at BP40 or BP43
INT4	|	140h	E8h (SCALL 140h)	Timer 2 interrupt
INT5	|	180h	F0h (SCALL 180h)	Timer 3 interrupt
INT6	|	1C0h	F8h (SCALL 1C0h)	External hardware interrupt, at any edge at BP50 or BP51
INT7	Highest	1E0h	FCh (SCALL 1E0h)	Voltage monitor (VM) interrupt

Table 2. Hardware Interrupts

Interrupt	Interrupt Mask		Interrupt Source
	Register	Bit	
INT1	P5CR	P52M1, P52M2 P53M1, P53M2	Any edge at BP52 any edge at BP53
INT2	T1M	T1IM	Timer 1
INT3	SISC	SIM	SSI buffer full/empty or BP40/BP43 interrupt
INT4	T2CM	T2IM	Timer 2 compare match/overflow
INT5	T3CM1 T3CM2 T3C	T3IM1 T3IM2 T3EIM	Timer 3 compare register 1 match Timer 3 compare register 2 match Timer 3 edge event occurs (T3I)
INT6	P5CR	P50M1, P50M2 P51M1, P51M2	Any edge at BP50, any edge at BP51
INT7	VCM	VIM	External/internal voltage monitoring

Software Interrupts

The programmer can generate interrupts by using the software interrupt instruction (SWI), which is supported in qFORTH by predefined macros named SWI0...SWI7. The software triggered interrupt operates exactly like any hardware triggered interrupt. The SWI instruction takes the top two elements from the expression stack and writes the corresponding bits via the I/O bus to the interrupt pending register. Therefore, by using the SWI instruction, interrupts can be re-prioritized or lower priority processes scheduled for later execution.

Hardware Interrupts

In the microcontroller block, there are eleven hardware interrupt sources with seven different levels. Each source can be masked individually by mask bits in the corresponding control registers. An overview of the possible hardware configurations is shown in Table 3.

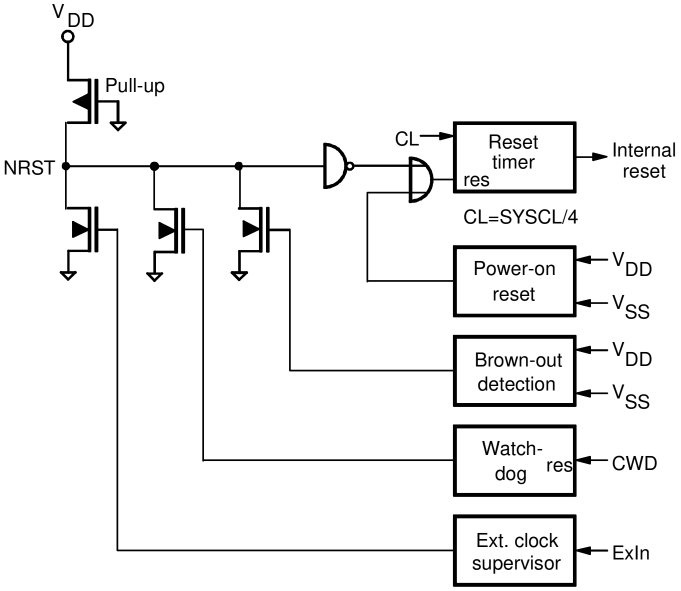
Master Reset

The master reset forces the CPU into a well-defined condition. It is unmaskable and is activated independent of the current program state. It can be triggered by either initial supply power-up, a short collapse of the power supply, brown-out detection circuitry, watchdog time-out, or an external input clock supervisor stage (see Figure 15). A master reset activation will reset the interrupt enable flag, the interrupt pending register and the interrupt active register. During the power-on reset phase, the I/O bus control signals are set to reset mode, thereby, initializing all on-chip peripherals. All bi-directional ports are set to input mode

Attention: During any reset phase, the BP20/NTE input is driven towards V_{DD} by an additional internal strong pull-up transistor. This pin must not be pulled down to V_{SS} during reset by any external circuitry representing a resistor of less than 150 kΩ.

Releasing the reset results in a short call instruction (opcode C1h) to the ROM address 008h. This activates the initialization routine $RESET which in turn has to initialize all necessary RAM variables, stack pointers and peripheral configuration registers (see Table 6).

Figure 15. Reset Configuration



Power-on Reset and Brown-out Detection

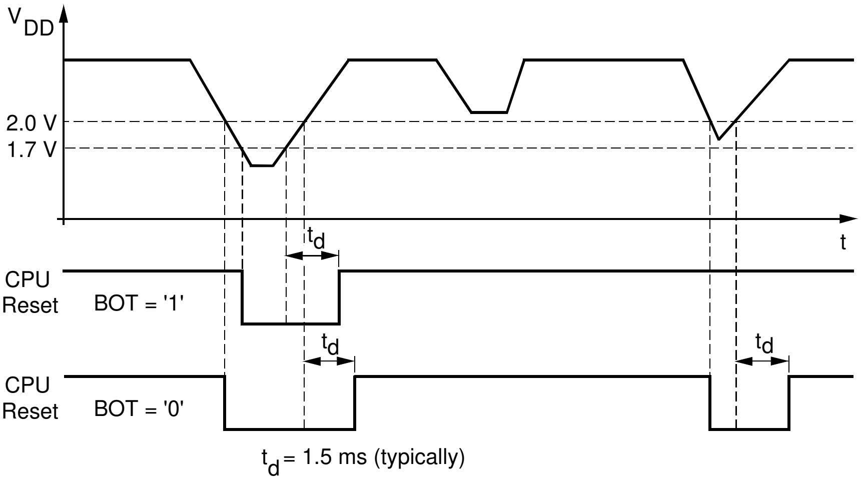
The microcontroller block has a fully integrated power-on reset and brown-out detection circuitry. For reset generation no external components are needed.

These circuits ensure that the core is held in the reset state until the minimum operating supply voltage has been reached. A reset condition will also be generated should the supply voltage drop momentarily below the minimum operating level except when a power-down mode is activated (the core is in SLEEP mode and the peripheral clock is stopped). In this power-down mode the brown-out detection is disabled.

Two values for the brown-out voltage threshold are programmable via the BOT-bit in the SC-register.

A power-on reset pulse is generated by a V_{DD} rise across the default BOT voltage level (1.7 V). A brown-out reset pulse is generated when V_{DD} falls below the brown-out voltage threshold. Two values for the brown-out voltage threshold are programmable via the BOT-bit in the SC-register. When the controller runs in the upper supply voltage range with a high system clock frequency, the high threshold must be used. When it runs with a lower system clock frequency, the low threshold and a wider supply voltage range may be chosen. For further details, see the electrical specification and the SC-register description for BOT programming.

Figure 16. Brown-out Detection



BOT = 1, low brown-out voltage threshold 1.7 V (is reset value).
BOT = 0, high brown-out voltage threshold 2.0 V.

Watchdog Reset

The watchdog's function can be enabled at the WDC-register and triggers a reset with every watchdog counter overflow. To suppress the watchdog reset, the watchdog counter must be regularly reset by reading the watchdog register address (CWD). The CPU reacts in exactly the same manner as a reset stimulus from any of the above sources.

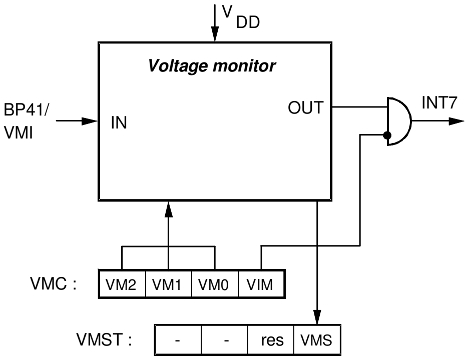
External Clock Supervisor

The external input clock supervisor function can be enabled if the external input clock is selected within the CM- and SC-registers of the clock module. The CPU reacts in exactly the same manner as a reset stimulus from any of the above sources.

Voltage Monitor

The voltage monitor consists of a comparator with internal voltage reference. It is used to supervise the supply voltage or an external voltage at the VMI-pin. The comparator for the supply voltage has three internal programmable thresholds one lower threshold (2.2 V), one middle threshold (2.6 V) and one higher threshold (3.0 V). For external voltages at the VMI-pin, the comparator threshold is set to V_{BG} = 1.3 V. The VMS-bit indicates if the supervised voltage is below (VMS = 0) or above (VMS = 1) this threshold. An interrupt can be generated when the VMS-bit is set or reset to detect a rising or falling slope. A voltage monitor interrupt (INT7) is enabled when the interrupt mask bit (VIM) is reset in the VMC-register.

Figure 17. Voltage Monitor



Voltage Monitor Control/Status Register

Primary register address: "F"hex

	Bit 3	Bit 2	Bit 1	Bit 0	
VMC: Write	***VM2***	***VM1***	***VM0***	***VIM***	***Reset value: 1111b***
VMST: Read	***–***	***–***	***reserved***	***VMS***	***Reset value: xx11b***

VM2: ***V***oltage monitor ***M***ode bit ***2***
VM1: ***V***oltage monitor ***M***ode bit ***1***
VM0: ***V***oltage monitor ***M***ode bit ***0***

VM2	*VM1*	*VM0*	*Function*
1	1	1	Disable voltage monitor
1	1	0	External (VIM-input), internal reference threshold (1.3 V), interrupt with negative slope
1	0	1	Not allowed
1	0	0	External (VMI-input), internal reference threshold (1.3 V), interrupt with positive slope
0	1	1	Internal (supply voltage), high threshold (3.0 V), interrupt with negative slope
0	1	0	Internal (supply voltage), middle threshold (2.6 V), interrupt with negative slope
0	0	1	Internal (supply voltage), low threshold (2.2 V), interrupt with negative slope
0	0	0	Not allowed

VIM ***V***oltage ***I***nterrupt ***M***ask bit
VIM = 0, voltage monitor interrupt is enabled
VIM = 1, voltage monitor interrupt is disabled

VMS ***V***oltage ***M***onitor ***S***tatus bit
VMS = 0, the voltage at the comparator input is below V_{Ref}
VMS = 1, the voltage at the comparator input is above V_{Ref}

Figure 18. Internal Supply Voltage Supervisor

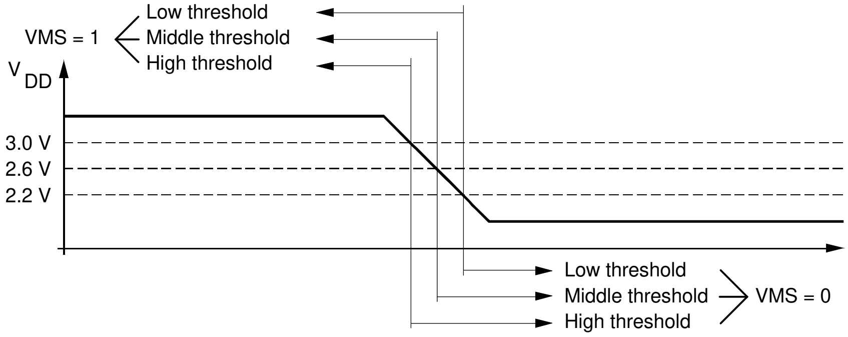
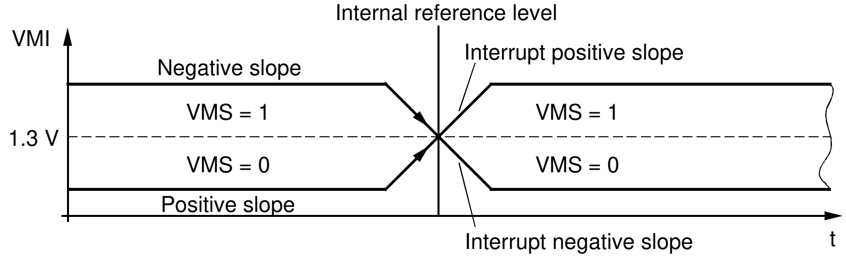


Figure 19. External Input Voltage Supervisor



Clock Generation

Clock Module

The T48C862-R3 contains a clock module with 4 different internal oscillator types: two RC-oscillators, one 4-MHz crystal oscillator and one 32-kHz crystal oscillator. The pins OSC1 and OSC2 are the interface to connect a crystal either to the 4-MHz, or to the 32-kHz crystal oscillator. OSC1 can be used as input for external clocks or to connect an external trimming resistor for the RC-oscillator 2. All necessary circuitry, except the crystal and the trimming resistor, is integrated on-chip. One of these oscillator types or an external input clock can be selected to generate the system clock (SYSCL).

In applications that do not require exact timing, it is possible to use the fully integrated RC-oscillator 1 without any external components. The RC-oscillator 1 center frequency tolerance is better than ± 50%. The RC-oscillator 2 is a trimmable oscillator whereby the oscillator frequency can be trimmed with an external resistor attached between OSC1 and V_{DD}. In this configuration, the RC-oscillator 2 frequency can be maintained stable with a tolerance of ± 15% over the full operating temperature and voltage range.

The clock module is programmable via software with the clock management register (CM) and the system configuration register (SC). The required oscillator configuration can be selected with the OS1-bit and the OS0-bit in the SC-register. A programmable 4-bit divider stage allows the adjustment of the system clock speed. A special feature of the clock management is that an external oscillator may be used and switched on and off via a port pin for the power-down mode. Before the external clock is switched off, the internal RC-oscillator 1 must be selected with the CCS-bit and then the SLEEP mode may be activated. In this state an interrupt can wake up the controller with the RC-oscillator, and the external oscillator can be activated and selected by software. A synchronization stage avoids too short clock periods if the clock source or the clock speed is changed. If an external input clock is selected, a supervisor circuit monitors the external input and generates a hardware reset if the external clock source fails or drops below 500 kHz for more than 1 ms.

Figure 20. Clock Module

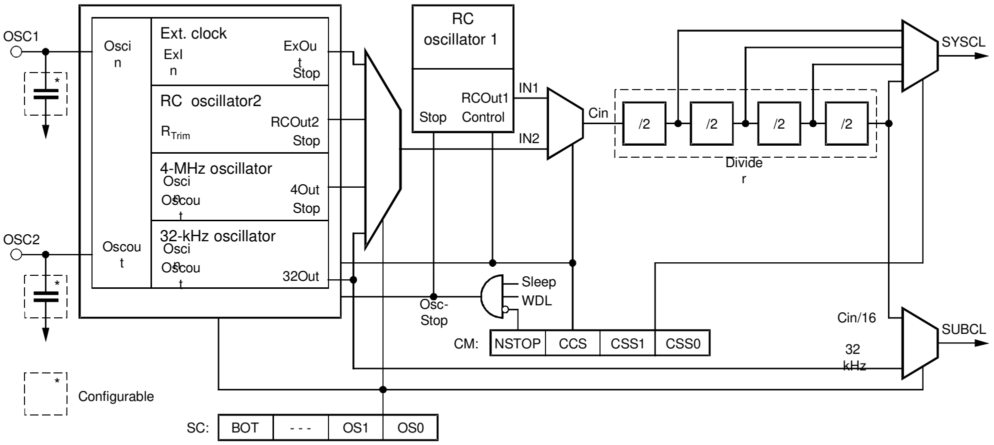


Table 3. Clock Modes

Mode	OS1	OS0	Clock Source for SYSCL		Clock Source for SUBCL
			CCS = 1	CCS = 0	
1	1	1	RC-oscillator 1 (internal)	External input clock	$C_{in}/16$
2	0	1	RC-oscillator 1 (internal)	RC-oscillator 2 with external trimming resistor	$C_{in}/16$
3	1	0	RC-oscillator 1 (internal)	4-MHz oscillator	$C_{in}/16$
4	0	0	RC-oscillator 1 (internal)	32-kHz oscillator	32 kHz

The clock module generates two output clocks. One is the system clock (SYSCL) and the other the periphery (SUBCL). The SYSCL can supply the core and the peripherals and the SUBCL can supply only the peripherals with clocks. The modes for clock sources are programmable with the OS1-bit and OS0-bit in the SC-register and the CCS-bit in the CM-register.

Oscillator Circuits and External Clock Input Stage

The microcontroller block series consists of four different internal oscillators: two RC-oscillators, one 4-MHz crystal oscillator, one 32-kHz crystal oscillator and one external clock input stage.

RC-oscillator 1 Fully Integrated

For timing insensitive applications, it is possible to use the fully integrated RC oscillator 1. It operates without any external components and saves additional costs. The RC-oscillator 1 center frequency tolerance is better than ±50% over the full temperature and voltage range. The basic center frequency of the RC-oscillator 1 is $f_O \approx 3.8$ MHz. The RC oscillator 1 is selected by default after power-on reset.