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Features

- *Frequency Receiving Range of*
  f_0 = 868 MHz to 870 MHz or f_0 = 902 MHz to 928 MHz
- *30 dB Image Rejection*
- *Receiving Bandwidth B_{IF} = 600 kHz for Low Cost 90-ppm Crystals*
- *Fully Integrated LC-VCO and PLL Loop Filter*
- *Very High Sensitivity with Power Matched LNA*
- *High System IIP3 (-16 dBm), System 1-dB Compression Point (-25 dBm)*
- *High Large-signal Capability at GSM Band*
  (Blocking -30 dBm at +20 MHz, IIP3 = -12 dBm at +20 MHz)
- *5 V to 20 V Automotive Compatible Data Interface*
- *Data Clock Available for Manchester- and Bi-phase-coded Signals*
- *Programmable Digital Noise Suppression*
- *Low Power Consumption Due to Configurable Polling*
- *Temperature Range -40°C to +105°C*
- *ESD Protection 2 kV HBM, All Pins*
- *Communication to Microcontroller Possible Via a Single Bi-directional Data Line*
- *Low-cost Solution Due to High Integration Level with Minimum External Circuitry Requirements*

UHF ASK/FSK Receiver

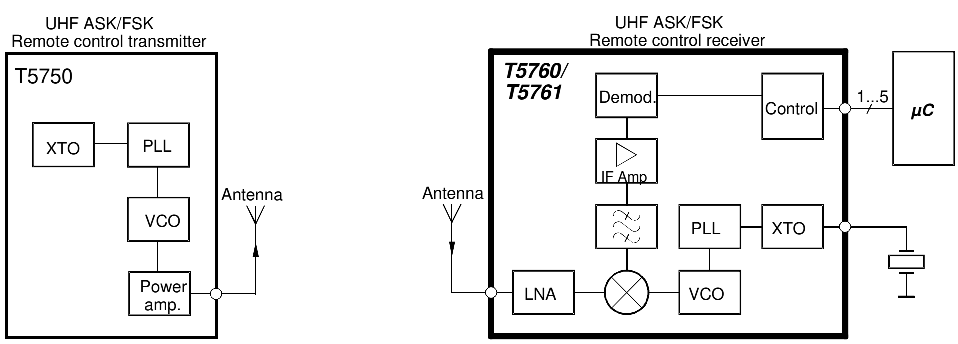
T5760/T5761

Preliminary

Description

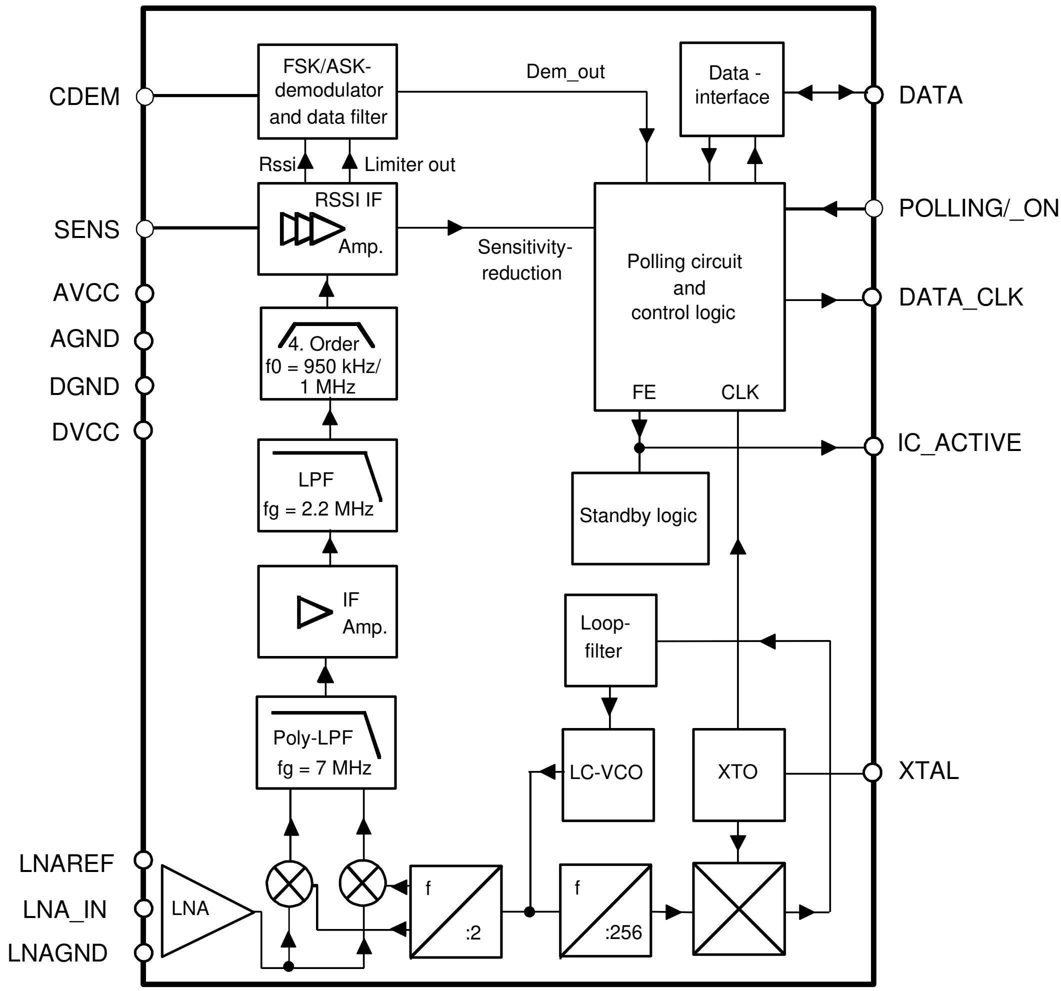
The T5760/T5761 is a multi-chip PLL receiver device supplied in an SO20 package. It has been especially developed for the demands of RF low-cost data transmission systems with data rates from 1 kBaud to 10 kBaud in Manchester or Bi-phase code. The receiver is well suited to operate with the Atmel's PLL RF transmitter T5750. Its main applications are in the areas of telemetering, security technology and keyless-entry systems. It can be used in the frequency receiving range of f_0 = 868 MHz to 870 MHz or f_0 = 902 MHz to 928 MHz for ASK or FSK data transmission. All the statements made below refer to 868.3 MHz and 915.0 MHz applications.

Figure 1. System Block Diagram



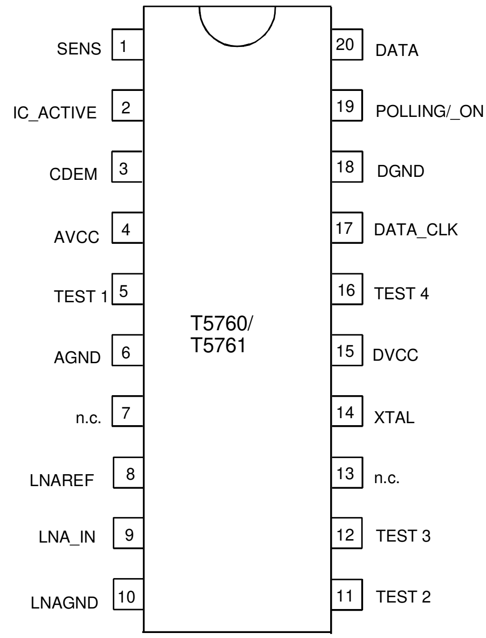
Rev. 4561B–RKE–10/02

Figure 2. Block Diagram



Pin Configuration

Figure 3. Pinning SO20



Pin Description

Pin	Symbol	Function
1	SENS	Sensitivity-control resistor
2	IC_ACTIVE	IC condition indicator: Low = sleep mode, High = active mode
3	CDEM	Lower cut-off frequency data filter
4	AVCC	Analog power supply
5	TEST 1	Test pin, during operation at GND
6	AGND	Analog ground
7	n.c.	Not connected, connect to GND
8	LNAREF	High-frequency reference node LNA and mixer
9	LNA_IN	RF input
10	LNAGND	DC ground LNA and mixer
11	TEST 2	Do not connect during operating
12	TEST 3	Test pin, during operation at GND
13	n.c.	Not connected, connect to GND
14	XTAL	Crystal oscillator XTAL connection
15	DVCC	Digital power supply
16	TEST 4	Test pin, during operation at DVCC
17	DATA_CLK	Bit clock of data stream
18	DGND	Digital ground
19	POLLING/_ON	Selects polling or receiving mode; Low: receiving mode, High: polling mode
20	DATA	Data output/configuration input

RF Front End

The RF front end of the receiver is a low-IF heterodyne configuration that converts the input signal into a 950 kHz/1 MHz IF signal with an image rejection of typical 30 dB. According to Figure 3 the front end consists of an LNA (Low Noise Amplifier), LO (Local Oscillator), I/Q mixer, polyphase lowpass filter and an IF amplifier.

The PLL generates the carrier frequency for the mixer via a full integrated synthesizer with integrated low noise LC-VCO (Voltage Controlled Oscillator) and PLL-loop filter. The XTO (crystal oscillator) generates the reference frequency f_{XTO}. The integrated LC-VCO generates two times the mixer drive frequency f_{VCO}. The I/Q signals for the mixer are generated with a divide by two circuit ($f_{LO} = f_{VCO}/2$). f_{VCO} is divided by a factor of 256 and feeds into a phase frequency detector and compared with f_{XTO}. The output of the phase frequency detector is fed into an integrated loop filter and thereby generates the control voltage for the VCO. If f_{LO} is determined, f_{XTO} can be calculated using the following formula:

$f_{XTO} = f_{LO}/128$

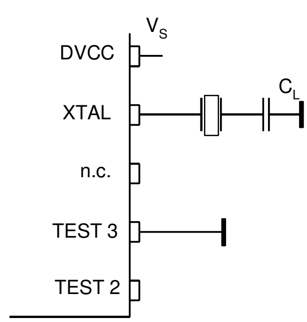
The XTO is a one-pin oscillator that operates at the series resonance of the quartz crystal with high current but low voltage signal, so that there is only a small voltage at the crystal oscillator frequency at Pin XTAL. According to Figure 4, the crystal should be connected to GND with a series capacitor C_L. The value of that capacitor is recommended by the crystal supplier. Due to a somewhat inductive impedance at steady state oscillation and some PCB parasitics a lower value of C_L is normally necessary.

The value of C_L should be optimized for the individual board layout to achieve the exact value of f_{XTO} (the best way is to use a crystal with known load resonance frequency to find the right value for this capacitor) and hereby of f_{LO}. When designing the system in terms of receiving bandwidth and local oscillator accuracy, the accuracy of the crystal and the XTO must be considered.

If a crystal with ±30 ppm adjustment tolerance at 25°C, ±50 ppm over temperature -40°C to +105°C, ±10 ppm of total aging and a CM (motional capacitance) of 7 fF is used, an additional XTO pulling of ±30 ppm has to be added.

The resulting total LO tolerance of ±120 ppm agrees with the receiving bandwidth specification of the T5760/T5761 if the T5750 has also a total LO tolerance of ±120 ppm.

Figure 4. XTO Peripherals



The nominal frequency f_{LO} is determined by the RF input frequency f_{RF} and the IF frequency f_{IF} using the following formula (low side injection):

$f_{LO} = f_{RF} - f_{IF}$

To determine f_{LO}, the construction of the IF filter must be considered at this point. The nominal IF frequency is f_{IF} = 950 kHz. To achieve a good accuracy of the filter corner frequencies, the filter is tuned by the crystal frequency f_{XTO}. This means that there is a fixed relation between f_{IF} and f_{LO}.

$f_{IF} = f_{LO}/915$

The relation is designed to achieve the nominal IF frequency of f_{IF} = 950 kHz for the 868.3 MHz version. For the 915 MHz version an IF frequency of f_{IF} = 1.0 MHz results.

The RF input either from an antenna or from an RF generator must be transformed to the RF input Pin LNA_IN. The input impedance of that pin is provided in the electrical parameters. The parasitic board inductances and capacitances influence the input matching. The RF receiver T5760/T5761 exhibits its highest sensitivity if the LNA is power matched. This makes the matching to an SAW filter as well as to 50 Ω or an antenna easier.

Figure 33 shows a typical input matching network for f_{RF} = 868.3 MHz to 50 Ω. Figure 34 illustrates an according input matching for 868.3 MHz to an SAW. The input matching network shown in Figure 33 is the reference network for the parameters given in the electrical characteristics.

Analog Signal Processing

IF Filter

The signals coming from the RF front-end are filtered by the fully integrated 4th-order IF filter. The IF center frequency is f_{IF} = 950 kHz for applications where f_{RF} = 868.3 MHz and f_{IF} =1.0 MHz for f_{RF} = 915 MHz. The nominal bandwidth is 600 kHz.

Limiting RSSI Amplifier

The subsequent RSSI amplifier enhances the output signal of the IF amplifier before it is fed into the demodulator. The dynamic range of this amplifier is DR_{RSSI} = 60 dB. If the RSSI amplifier is operated within its linear range, the best S/N ratio is maintained in ASK mode. If the dynamic range is exceeded by the transmitter signal, the S/N ratio is defined by the ratio of the maximum RSSI output voltage and the RSSI output voltage due to a disturber. The dynamic range of the RSSI amplifier is exceeded if the RF input signal is about 60 dB higher compared to the RF input signal at full sensitivity.

In FSK mode the S/N ratio is not affected by the dynamic range of the RSSI amplifier, because only the hard limited signal from a high gain limiting amplifier is used by the demodulator.

The output voltage of the RSSI amplifier is internally compared to a threshold voltage V_{Th_red}. V_{Th_red} is determined by the value of the external resistor R_{Sens}. R_{Sens} is connected between Pin SENS and GND or V_S. The output of the comparator is fed into the digital control logic. By this means it is possible to operate the receiver at a lower sensitivity.

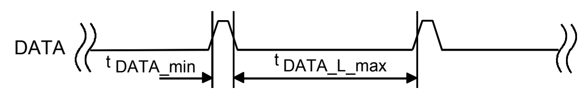
If R_{Sens} is connected to GND, the receiver switches to full sensitivity. It is also possible to connect the Pin SENS directly to GND to get the maximum sensitivity.

If R_{Sens} is connected to V_S, the receiver operates at a lower sensitivity. The reduced sensitivity is defined by the value of R_{Sens}, the maximum sensitivity by the signal-to-noise ratio of the LNA input. The reduced sensitivity depends on the signal strength at the output of the RSSI amplifier.

Since different RF input networks may exhibit slightly different values for the LNA gain, the sensitivity values given in the electrical characteristics refer to a specific input matching. This matching is illustrated in Figure 33 and exhibits the best possible sensitivity and at the same time power matching at RF_IN.

R_{Sens} can be connected to V_S or GND via a microcontroller. The receiver can be switched from full sensitivity to reduced sensitivity or vice versa at any time. In polling mode, the receiver will not wake up if the RF input signal does not exceed the selected sensitivity. If the receiver is already active, the data stream at Pin DATA will disappear when the input signal is lower than defined by the reduced sensitivity. Instead of the data stream, the pattern according to Figure 5 is issued at Pin DATA to indicate that the receiver is still active (see Figure 32).

Figure 5. Steady L State Limited DATA Output Pattern



FSK/ASK Demodulator and Data Filter

The signal coming from the RSSI amplifier is converted into the raw data signal by the ASK/FSK demodulator. The operating mode of the demodulator is set via the bit ASK/_FSK in the OPMODE register. Logic 'L' sets the demodulator to FSK, applying 'H' to ASK mode.

In ASK mode an automatic threshold control circuit (ATC) is employed to set the detection reference voltage to a value where a good signal to noise ratio is achieved. This circuit also implies the effective suppression of any kind of in-band noise signals or competing transmitters. If the S/N (ratio to suppress in-band noise signals) exceeds about 10 dB the data signal can be detected properly, but better values are found for many modulation schemes of the competing transmitter.

The FSK demodulator is intended to be used for an FSK deviation of 10 kHz $\leq \Delta f \leq$ 100 kHz. In FSK mode the data signal can be detected if the S/N (ratio to suppress in-band noise signals) exceeds about 2 dB. This value is valid for all modulation schemes of a disturber signal.

The output signal of the demodulator is filtered by the data filter before it is fed into the digital signal processing circuit. The data filter improves the S/N ratio as its passband can be adopted to the characteristics of the data signal. The data filter consists of a 1^{st-} order high pass and a 2^{nd-}order lowpass filter.

The highpass filter cut-off frequency is defined by an external capacitor connected to Pin CDEM. The cut-off frequency of the highpass filter is defined by the following formula:

$$\text{fcu\_DF} = \frac{1}{2 \times \pi \times 30\ \text{k}\Omega \times \text{CDEM}}$$

In self-polling mode, the data filter must settle very rapidly to achieve a low current consumption. Therefore, CDEM cannot be increased to very high values if self-polling is used. On the other hand CDEM must be large enough to meet the data filter requirements according to the data signal. Recommended values for CDEM are given in the electrical characteristics.

The cut-off frequency of the lowpass filter is defined by the selected baud-rate range (BR_Range). The BR_Range is defined in the OPMODE register (refer to chapter 'Configuration of the Receiver'). The BR_Range must be set in accordance to the used baud-rate.

The T5760/T5761 is designed to operate with data coding where the DC level of the data signal is 50%. This is valid for Manchester and Bi-phase coding. If other modulation schemes are used, the DC level should always remain within the range of V_{DC_min} = 33% and V_{DC_max} = 66%. The sensitivity may be reduced by up to 2 dB in that condition.

Each BR_Range is also defined by a minimum and a maximum edge-to-edge time (t_{ee_sig}). These limits are defined in the electrical characteristics. They should not be exceeded to maintain full sensitivity of the receiver.

Receiving Characteristics

The RF receiver T5760/T5761 can be operated with and without a SAW front-end filter. In a typical automotive application, a SAW filter is used to achieve better selectivity and large signal capability. The receiving frequency response without a SAW front-end filter is illustrated in Figure 6 and Figure 7. This example relates to ASK mode. FSK mode exhibits a similar behavior. The plots are printed relatively to the maximum sensitivity. If a SAW filter is used, an insertion loss of about 3 dB must be considered, but the overall selectivity is much better.

When designing the system in terms of receiving bandwidth, the LO deviation must be considered as it also determines the IF center frequency. The total LO deviation is calculated, to be the sum of the deviation of the crystal and the XTO deviation of the T5760/T5761. Low-cost crystals are specified to be within ±90 ppm over tolerance, temperature and aging. The XTO deviation of the T5760/T5761 is an additional deviation due to the XTO circuit. This deviation is specified to be ±30 ppm worst case for a crystal with CM = 7 fF. If a crystal of ±90 ppm is used, the total deviation is ±120 ppm in that case. Note that the receiving bandwidth and the IF-filter bandwidth are equivalent in ASK mode but not in FSK mode.

Figure 6. Narrow Band Receiving Frequency Response

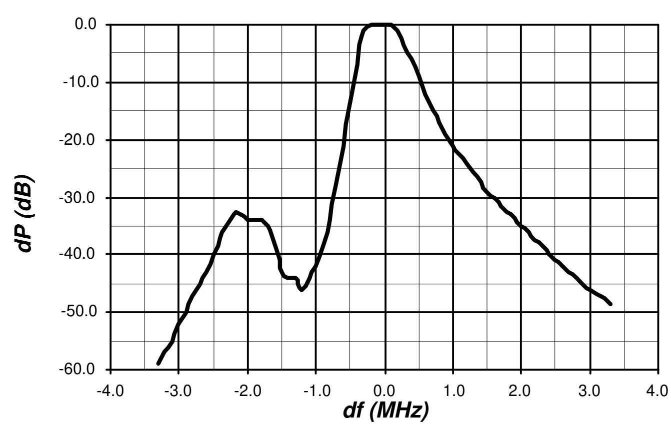
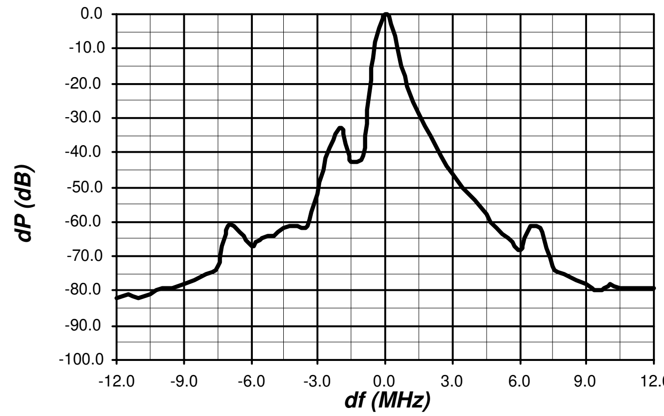


Figure 7. Wide Band Receiving Frequency Response



Polling Circuit and Control Logic

The receiver is designed to consume less than 1 mA while being sensitive to signals from a corresponding transmitter. This is achieved via the polling circuit. This circuit enables the signal path periodically for a short time. During this time the bit-check logic verifies the presence of a valid transmitter signal. Only if a valid signal is detected, the receiver remains active and transfers the data to the connected microcontroller. If there is no valid signal present, the receiver is in sleep mode most of the time resulting in low current consumption. This condition is called polling mode. A connected microcontroller is disabled during that time.

All relevant parameters of the polling logic can be configured by the connected microcontroller. This flexibility enables the user to meet the specifications in terms of current consumption, system response time, data rate etc.

Regarding the number of connection wires to the microcontroller, the receiver is very flexible. It can be either operated by a single bi-directional line to save ports to the connected microcontroller or it can be operated by up to five uni-directional ports.

Basic Clock Cycle of the Digital Circuitry

The complete timing of the digital circuitry and the analog filtering is derived from one clock. This clock cycle T_{Clk} is derived from the crystal oscillator (XTO) in combination with a divide by 14 circuit. According to chapter 'RF Front End', the frequency of the crystal oscillator (f_{XTO}) is defined by the RF input signal (f_{RFin}) which also defines the operating frequency of the local oscillator (f_{LO}). The basic clock cycle is $T_{Clk} = 14/f_{XTO}$ giving $T_{Clk} = 2.066$ µs for $f_{RF} = 868.3$ MHz and $T_{Clk} = 1.961$ µs for $f_{RF} = 915$ MHz.

T_{Clk} controls the following application-relevant parameters:

- Timing of the polling circuit including bit check
- Timing of the analog and digital signal processing
- Timing of the register programming
- Frequency of the reset marker
- IF filter center frequency (f_{IF0})

Most applications are dominated by two transmission frequencies: $f_{Transmit} = 915$ MHz is mainly used in USA, $f_{Transmit} = 868.3$ MHz in Europe. In order to ease the usage of all T_{Clk}-dependent parameters on this electrical characteristics display three conditions for each parameter.

- Application USA (f_{XTO} = 7.14063 MHz, T_{Clk} = 1.961 µs)
- Application Europe (f_{XTO} = 6.77617 MHz, T_{Clk} = 2.066 µs)
- Other applications The electrical characteristic is given as a function of T_{Clk}.

The clock cycle of some function blocks depends on the selected baud-rate range (BR_Range) which is defined in the OPMODE register. This clock cycle T_{XClk} is defined by the following formulas for further reference:

BR_Range = BR_Range0: $T_{XClk} = 8 \times T_{Clk}$
BR_Range1: $T_{XClk} = 4 \times T_{Clk}$
BR_Range2: $T_{XClk} = 2 \times T_{Clk}$
BR_Range3: $T_{XClk} = 1 \times T_{Clk}$

Polling Mode

According to Figure 11, the receiver stays in polling mode in a continuous cycle of three different modes. In sleep mode the signal processing circuitry is disabled for the time period T_{Sleep} while consuming low current of $I_S = I_{Soff}$. During the start-up period, $T_{Startup}$, all signal processing circuits are enabled and settled. In the following bit-check mode, the incoming data stream is analyzed bit by bit contra a valid transmitter signal. If no valid signal is present, the receiver is set back to sleep mode after the period $T_{Bit\text{-}check}$. This period varies check by check as it is a statistical process. An average value for $T_{Bit\text{-}check}$ is given in the electrical characteristics. During $T_{Startup}$ and $T_{Bit\text{-}check}$ the current consumption is $I_S = I_{Son}$. The condition of the receiver is indicated on Pin IC_ACTIVE. The average current consumption in polling mode is dependent on the duty cycle of the active mode and can be calculated as:

$$I_{Spoll} = \frac{I_{Soff} \times T_{Sleep} + I_{Son} \times (T_{Startup} + T_{Bit\text{-}check})}{T_{Sleep} + T_{Startup} + T_{Bit\text{-}check}}$$

During T_{Sleep} and $T_{Startup}$ the receiver is not sensitive to a transmitter signal. To guarantee the reception of a transmitted command the transmitter must start the telegram with an adequate preburst. The required length of the preburst depends on the polling parameters T_{Sleep}, $T_{Startup}$, $T_{Bit\text{-}check}$ and the start-up time of a connected microcontroller ($T_{Start\_microcontroller}$). Thus, $T_{Bit\text{-}check}$ depends on the actual bit rate and the number of bits ($N_{Bit\text{-}check}$) to be tested.

The following formula indicates how to calculate the preburst length.

$$T_{Preburst} \geq T_{Sleep} + T_{Startup} + T_{Bit\text{-}check} + T_{Start\_microcontroller}$$

Sleep Mode

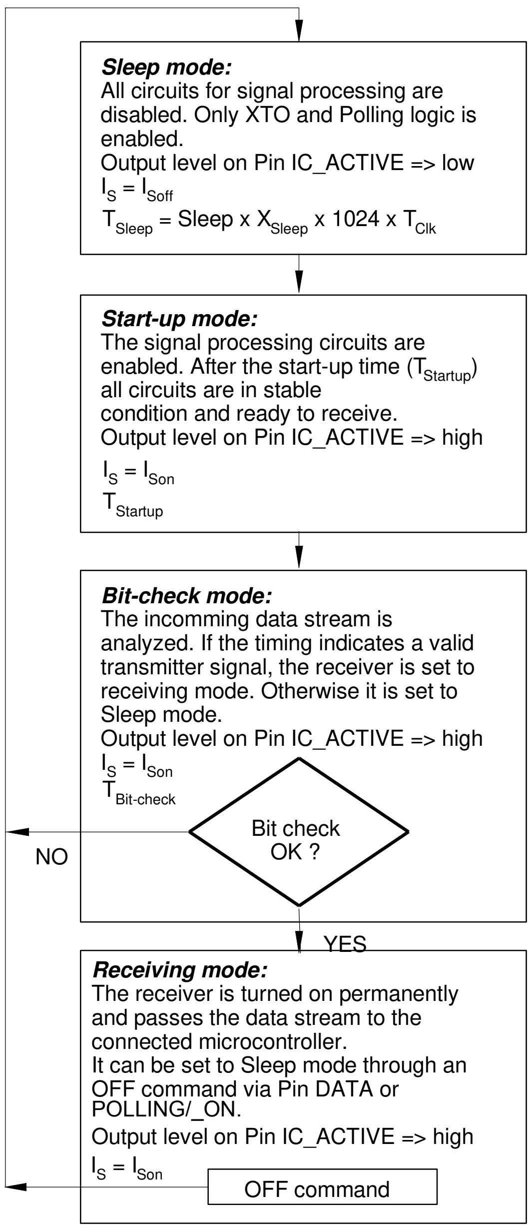
The length of period T_{Sleep} is defined by the 5-bit word Sleep of the OPMODE register, the extension factor XSleep (according to Table 8), and the basic clock cycle T_{Clk}. It is calculated to be:

$$T_{Sleep} = Sleep \times X_{Sleep} \times 1024 \times T_{Clk}$$

In US- and European applications, the maximum value of T_{Sleep} is about 60 ms if XSleep is set to 1. The time resolution is about 2 ms in that case. The sleep time can be extended to almost half a second by setting XSleep to 8. XSleep can be set to 8 by bit $XSleep_{Std}$ to'1'.

According to Table 7, the highest register value of sleep sets the receiver into a permanent sleep condition. The receiver remains in that condition until another value for Sleep is programmed into the OPMODE register. This function is desirable where several devices share a single data line and may also be used for microcontroller polling – via Pin POLLING/_ON, the receiver can be switched on and off.

Figure 8. Polling Mode Flow Chart



Sleep: 5-bit word defined by Sleep0 to Sleep4 in OPMODE register

X_{Sleep}: Extension factor defined by XSleepStd according to Table 9

T_{Clk}: Basic clock cycle defined by fXTO and Pin MODE

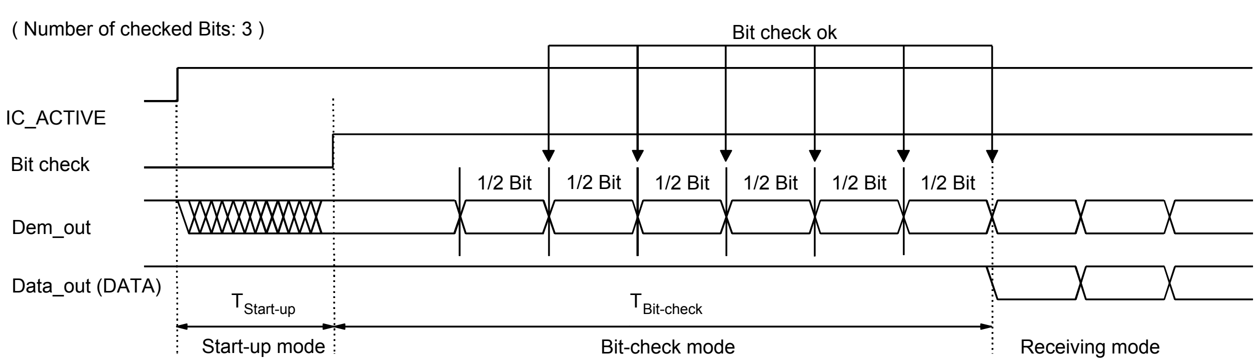
$T_{Startup}$: Is defined by the selected baud rate range and TClk. The baud-rate range is defined by Baud0 and Baud1 in the OPMODE register.

$T_{Bit\text{-}check}$: Depends on the result of the bit check

If the bit check is ok, $T_{Bit\text{-}check}$ depends on the number of bits to be checked ($N_{Bit\text{-}check}$) and on the utilized data rate.

If the bit check fails, the average time period for that check depends on the selected baud-rate range and on T_{Clk}. The baud-rate range is defined by Baud0 and Baud1 in the OPMODE register.

Figure 9. Timing Diagram for Complete Successful Bit Check



Bit-check Mode

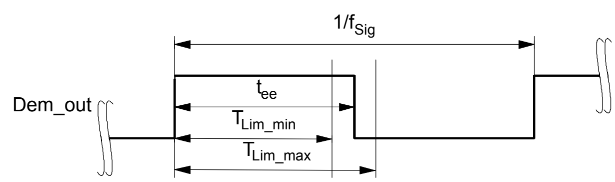
In bit-check mode the incoming data stream is examined to distinguish between a valid signal from a corresponding transmitter and signals due to noise. This is done by subsequent time frame checks where the distances between 2 signal edges are continuously compared to a programmable time window. The maximum count of this edge-to-edge tests before the receiver switches to receiving mode is also programmable.

Configuring the Bit Check

Assuming a modulation scheme that contains 2 edges per bit, two time frame checks are verifying one bit. This is valid for Manchester, Bi-phase and most other modulation schemes. The maximum count of bits to be checked can be set to 0, 3, 6 or 9 bits via the variable $N_{Bit\text{-}check}$ in the OPMODE register. This implies 0, 6, 12 and 18 edge-to-edge checks respectively. If $N_{Bit\text{-}check}$ is set to a higher value, the receiver is less likely to switch to receiving mode due to noise. In the presence of a valid transmitter signal, the bit check takes less time if $N_{Bit\text{-}check}$ is set to a lower value. In polling mode, the bit-check time is not dependent on $N_{Bit\text{-}check}$. Figure 9 shows an example where 3 bits are tested successfully and the data signal is transferred to Pin DATA.

According to Figure 10, the time window for the bit check is defined by two separate time limits. If the edge-to-edge time t_{ee} is in between the lower bit-check limit T_{Lim_min} and the upper bit-check limit T_{Lim_max}, the check will be continued. If t_{ee} is smaller than T_{Lim_min} or t_{ee} exceeds T_{Lim_max}, the bit check will be terminated and the receiver switches to sleep mode.

Figure 10. Valid Time Window for Bit Check



For best noise immunity it is recommended to use a low span between T_{Lim_min} and T_{Lim_max}. This is achieved using a fixed frequency at a 50% duty cycle for the transmitter preburst. A '11111...' or a '10101...' sequence in Manchester or Bi-phase is a good choice concerning that advice. A good compromise between receiver sensitivity and susceptibility to noise is a time window of ± 30% regarding the expected edge-to-edge time t_{ee}. Using pre-burst patterns that contain various edge-to-edge time periods, the bit-check limits must be programmed according to the required span.

The bit-check limits are determined by means of the formula below.

$T_{Lim\_min} = Lim\_min \times T_{XClk}$
$T_{Lim\_max} = (Lim\_max - 1) \times T_{XClk}$

Lim_min and Lim_max are defined by a 5-bit word each within the LIMIT register.

Using above formulas, Lim_min and Lim_max can be determined according to the required T_{Lim_min}, T_{Lim_max} and T_{XClk}. The time resolution defining T_{Lim_min} and T_{Lim_max} is T_{XClk}. The minimum edge-to-edge time t_{ee} ($t_{DATA\_L\_min}$, $t_{DATA\_H\_min}$) is defined according to the chapter 'Receiving Mode'. The lower limit should be set to Lim_min ≥10. The maximum value of the upper limit is Lim_max = 63.

If the calculated value for Lim_min is <19, it is recommended to check 6 or 9 bits ($N_{Bit\text{-}check}$) to prevent switching to receiving mode due to noise.

Figure 14, Figure 15 and Figure 16 illustrate the bit check for the bit-check limits Lim_min = 14 and Lim_max = 24. When the IC is enabled, the signal processing circuits are enabled during $T_{Startup}$. The output of the ASK/FSK demodulator (Dem_out) is undefined during that period. When the bit check becomes active, the bit-check counter is clocked with the cycle T_{XClk}.

Figure 14 shows how the bit check proceeds if the bit-check counter value CV_Lim is within the limits defined by Lim_min and Lim_max at the occurrence of a signal edge. In Figure 15 the bit check fails as the value CV_Lim is lower than the limit Lim_min. The bit check also fails if CV_Lim reaches Lim_max. This is illustrated in Figure 16.

Figure 11. Timing Diagram During Bit Check

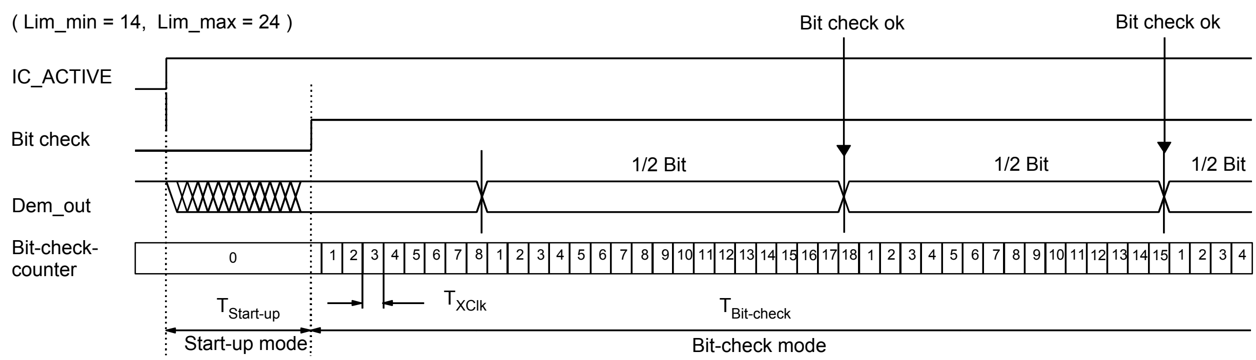


Figure 12. Timing Diagram for Failed Bit Check (Condition: CV_Lim < Lim_min)

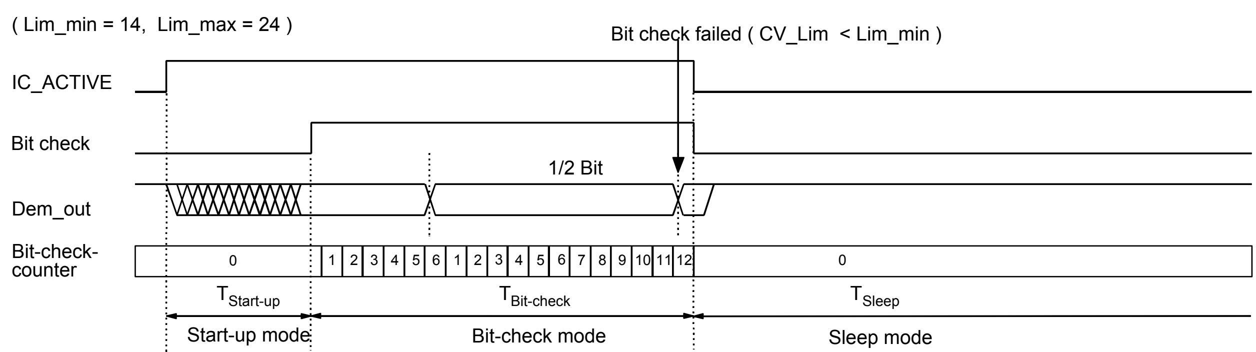
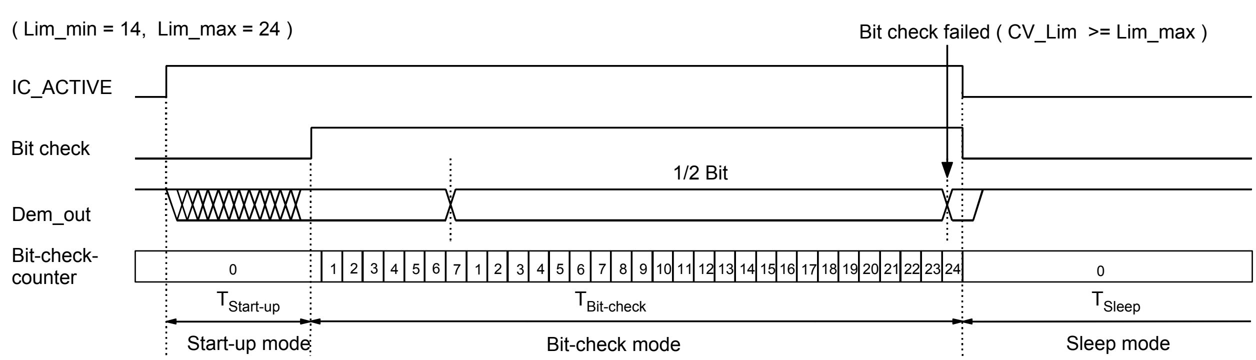


Figure 13. Timing Diagram for Failed Bit Check (Condition: CV_Lim >= Lim_max)



Duration of the Bit Check

If no transmitter signal is present during the bit check, the output of the ASK/FSK demodulator delivers random signals. The bit check is a statistical process and $T_{Bit\text{-}check}$ varies for each check. Therefore, an average value for $T_{Bit\text{-}check}$ is given in the electrical characteristics. $T_{Bit\text{-}check}$ depends on the selected baud-rate range and on T_{Clk}. A higher baud-rate range causes a lower value for $T_{Bit\text{-}check}$ resulting in a lower current consumption in polling mode.

In the presence of a valid transmitter signal, $T_{Bit\text{-}check}$ is dependent on the frequency of that signal, f_{Sig}, and the count of the checked bits, $N_{Bit\text{-}check}$. A higher value for $N_{Bit\text{-}check}$ thereby results in a longer period for $T_{Bit\text{-}check}$ requiring a higher value for the transmitter pre-burst $T_{Preburst}$.

Receiving Mode

If the bit check was successful for all bits specified by $N_{Bit\text{-}check}$, the receiver switches to receiving mode. According to Figure 9, the internal data signal is switched to Pin DATA in that case and the data clock is available after the start bit has been detected (see Figure 20). A connected microcontroller can be woken up by the negative edge at Pin DATA or by the data clock at Pin DATA_CLK. The receiver stays in that condition until it is switched back to polling mode explicitly.

Digital Signal Processing

The data from the ASK/FSK demodulator (Dem_out) is digitally processed in different ways and as a result converted into the output signal data. This processing depends on the selected baud-rate range (BR_Range). Figure 14 illustrates how Dem_out is synchronized by the extended clock cycle T_{XClk}. This clock is also used for the bit-check counter. Data can change its state only after T_{XClk} has elapsed. The edge-to-edge time period t_{ee} of the Data signal as a result is always an integral multiple of T_{XClk}.

The minimum time period between two edges of the data signal is limited to $t_{ee} \geq T_{DATA\_min}$. This implies an efficient suppression of spikes at the DATA output. At the same time it limits the maximum frequency of edges at DATA. This eases the interrupt handling of a connected microcontroller.

The maximum time period for DATA to stay Low is limited to $T_{DATA\_L\_max}$. This function is employed to ensure a finite response time in programming or switching off the receiver via Pin DATA. $T_{DATA\_L\_max}$ is thereby longer than the maximum time period indicated by the transmitter data stream. Figure 16 gives an example where Dem_out remains Low after the receiver has switched to receiving mode.

Figure 14. Synchronization of the Demodulator Output

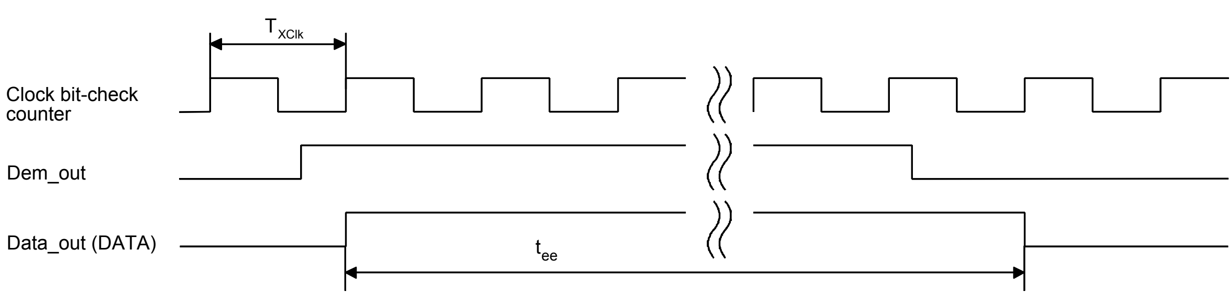


Figure 15. Debouncing of the Demodulator Output

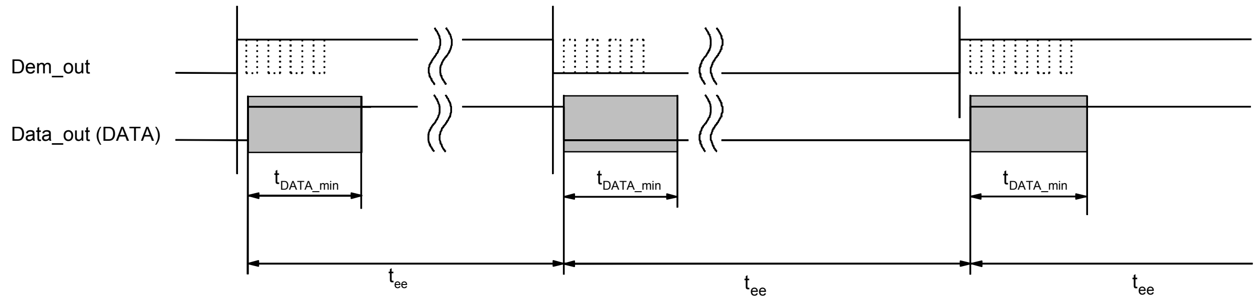
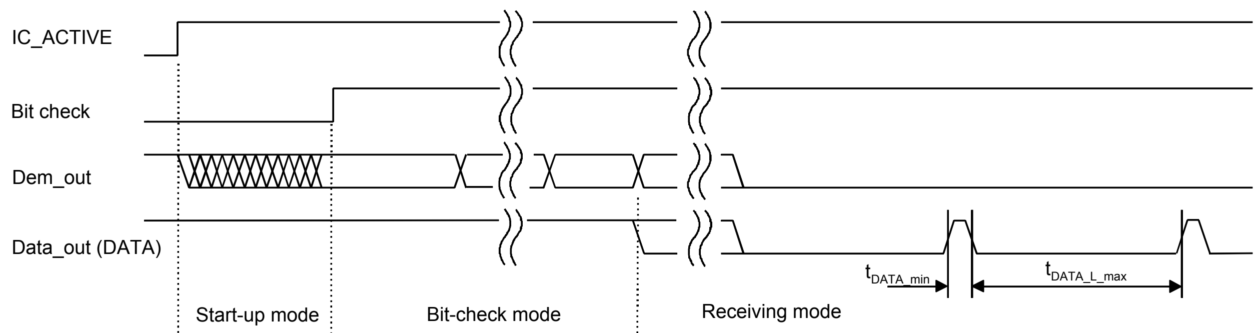


Figure 16. Steady L State Limited DATA Output Pattern After Transmission



After the end of a data transmission, the receiver remains active. Depending of the bit Noise_Disable in the OPMODE register, the output signal at Pin DATA is high or random noise pulses appear at Pin DATA (see chapter 'Digital Noise Suppression'). The edge-to-edge time period t_{ee} of the majority of these noise pulses is equal or slightly higher than T_{DATA_min}.

Switching the Receiver Back to Sleep Mode

The receiver can be set back to polling mode via Pin DATA or via Pin POLLING/_ON.

When using Pin DATA, this pin must be pulled to Low for the period t1 by the connected microcontroller. Figure 17 illustrates the timing of the OFF command (see Figure 32). The minimum value of t1 depends on BR_Range. The maximum value for t1 is not limited but it is recommended not to exceed the specified value to prevent erasing the reset marker. Note also that an internal reset for the OPMODE and the LIMIT register will be generated if t1 exceeds the specified values. This item is explained in more detail in the chapter 'Configuration of the Receiver'. Setting the receiver to sleep mode via DATA is achieved by programming bit 1 to be '1' during the register configuration. Only one sync pulse (t3) is issued.

The duration of the OFF command is determined by the sum of t1, t2 and t10. After the OFF command the sleep time T_{Sleep} elapses. Note that the capacitive load at Pin DATA is limited (see chapter 'Data Interface').

Figure 17. Timing Diagram of the OFF Command via Pin DATA

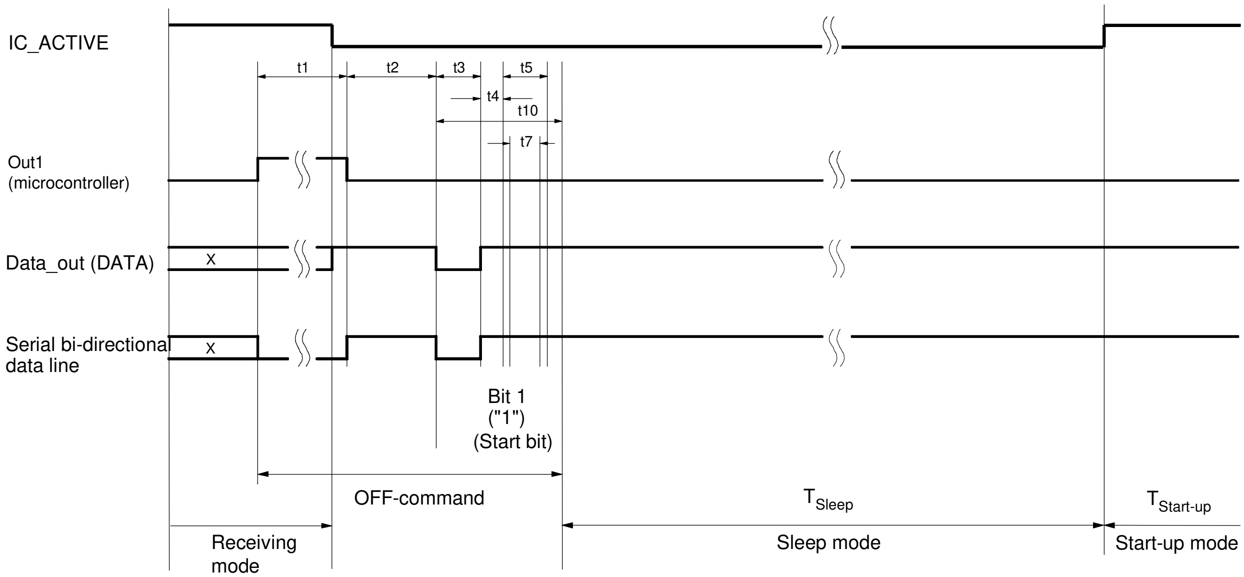


Figure 18. Timing Diagram of the OFF Command via Pin POLLING/_ON

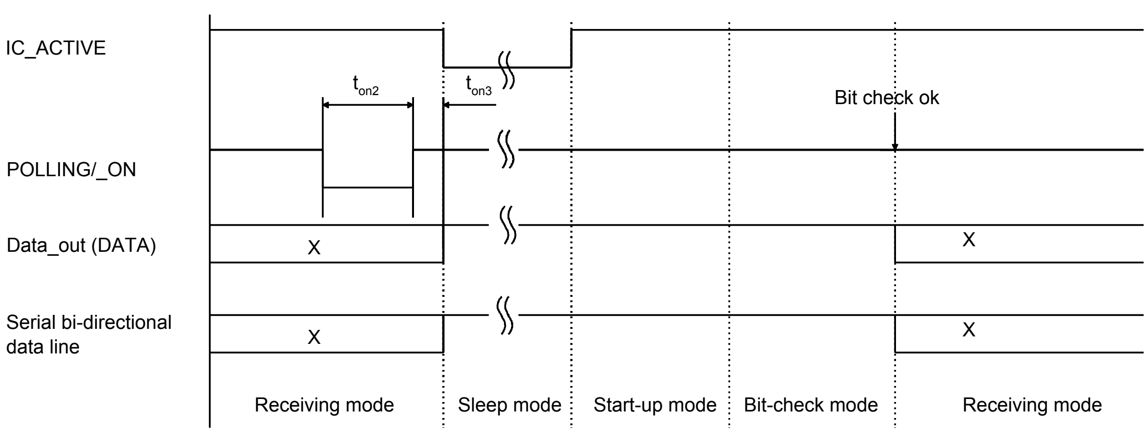


Figure 19. Activating the Receiving Mode via Pin POLLING/_ON

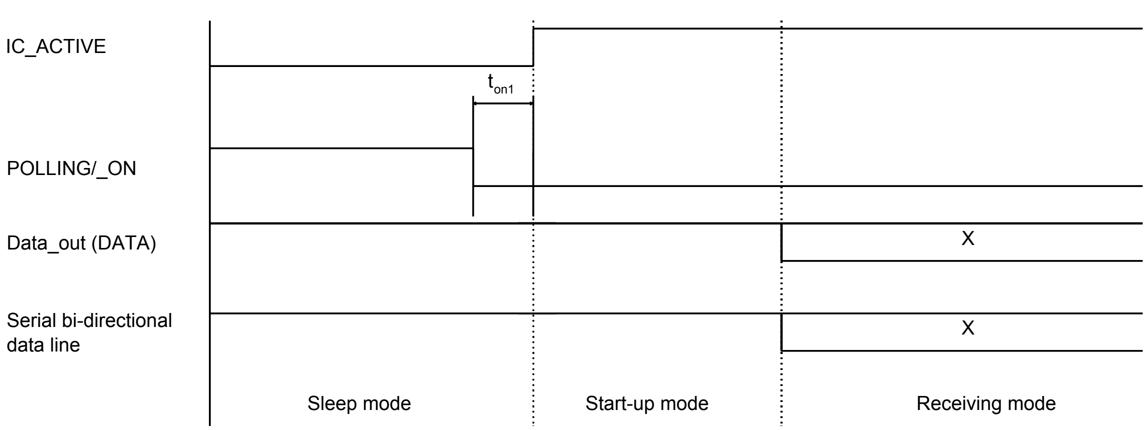


Figure 18 illustrates how to set the receiver back to polling mode via Pin POLLING/_ON. The Pin POLLING/_ON must be held to low for the time period t_{on2}. After the positive edge on Pin POLLING/_ON and the delay t_{on3}, the polling mode is active and the sleep time T_{Sleep} elapses.

This command is faster than using Pin DATA at the cost of an additional connection to the microcontroller.

Figure 19 illustrates how to set the receiver to receiving mode via the Pin POLLING/_ON. The Pin POLLING/_ON must be held to Low. After the delay t_{on1}, the receiver changes from sleep mode to start-up mode regardless the programmed values for T_{Sleep} and $N_{Bit\text{-}check}$. As long as POLLING/_ON is held to Low, the values for T_{Sleep} and $N_{Bit\text{-}check}$ will be ignored, but not deleted (see chapter 'Digital Noise Suppression').

If the receiver is polled exclusively by a microcontroller, T_{Sleep} must be programmed to 31 (permanent sleep mode). In this case the receiver remains in sleep mode as long as POLLING/_ON is held to High.

Data Clock

The Pin DATA_CLK makes a data shift clock available to sample the data stream into a shift register. Using this data clock, a microcontroller can easily synchronize the data stream. This clock can only be used for Manchester and Bi-phase coded signals.

Generation of the Data Clock

After a successful bit check, the receiver switches from polling mode to receiving mode and the data stream is available at Pin DATA. In receiving mode, the data clock control logic (Manchester/Bi-phase demodulator) is active and examines the incoming data stream. This is done, like in the bit check, by subsequent time frame checks where the distance between two edges is continuously compared to a programmable time window. As illustrated in Figure 20, only two distances between two edges in Manchester and Bi-phase coded signals are valid (T and 2T).

The limits for T are the same as used for the bit check. They can be programmed in the LIMIT-register (Lim_min and Lim_max, see Table 10 and Table 11).

The limits for 2T are calculated as follows:

Lower limit of 2T: Lim_min_2T = (Lim_min + Lim_max) - (Lim_max - Lim_min)/2

Upper limit of 2T: Lim_max_2T= (Lim_min + Lim_max) + (Lim_max - Lim_min)/2

(If the result for 'Lim_min_2T' or 'Lim_max_2T' is not an integer value, it will be round up)

The data clock is available, after the data clock control logic has detected the distance 2T (Start bit) and is issued with the delay t_{Delay} after the edge on Pin DATA (see Figure 20).

If the data clock control logic detects a timing or logical error (Manchester code violation), like illustrated in Figure 21 and Figure 22, it stops the output of the data clock. The receiver remains in receiving mode and starts with the bit check. If the bit check was successful and the start bit has been detected, the data clock control logic starts again with the generation of the data clock (see Figure 23).

It is recommended to use the function of the data clock only in conjunction with the bit check 3, 6 or 9. If the bit check is set to 0 or the receiver is set to receiving mode via the Pin POLLING/_ON, the data clock is available if the data clock control logic has detected the distance 2T (Start bit).

Note that for Bi-phase-coded signals, the data clock is issued at the end of the bit.

Figure 20. Timing Diagram of the Data Clock

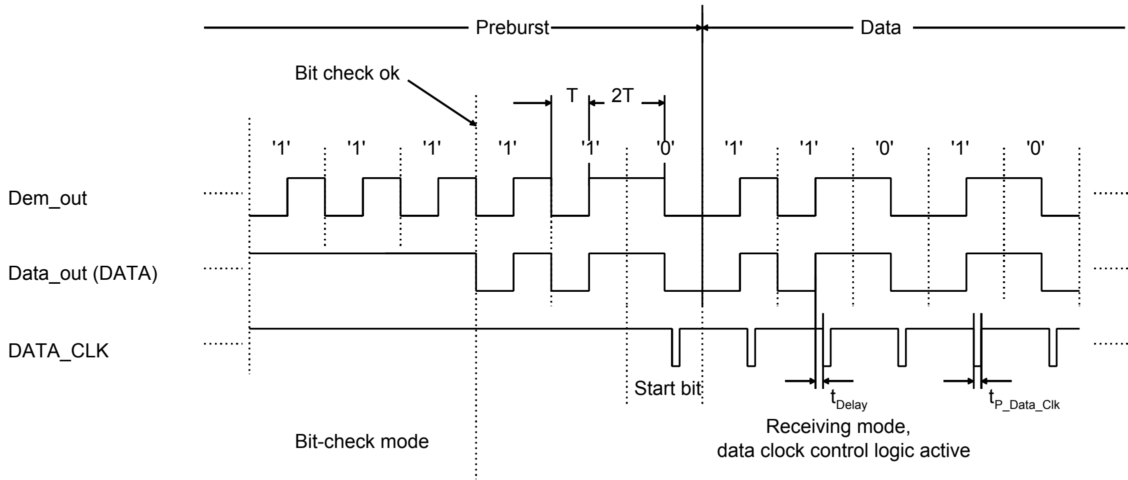


Figure 21. Data Clock Disappears Because of a Timing Error

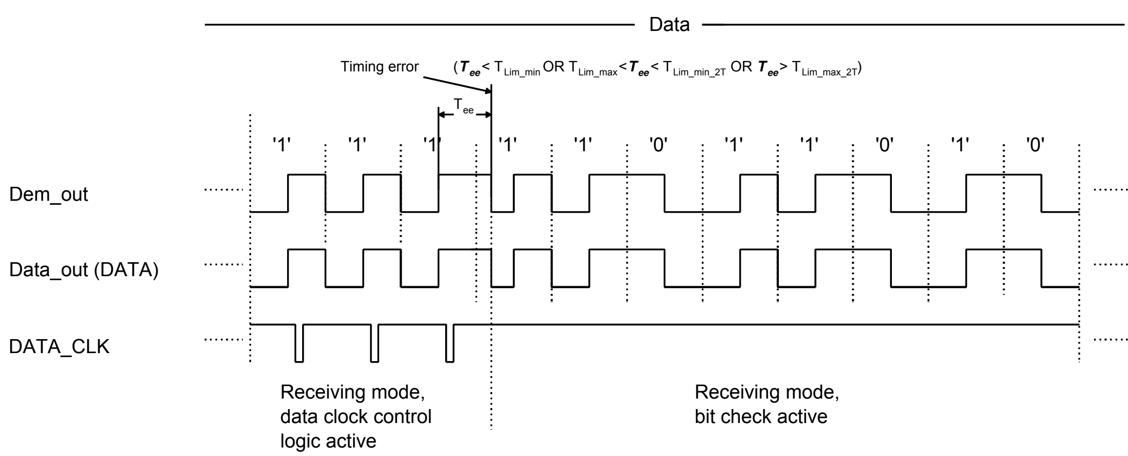


Figure 22. Data Clock Disappears Because of a Logical Error

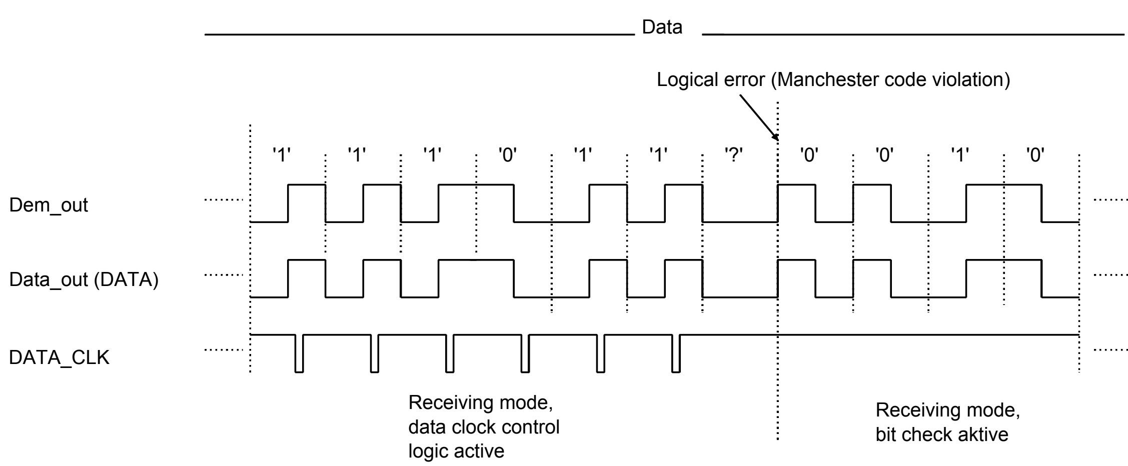
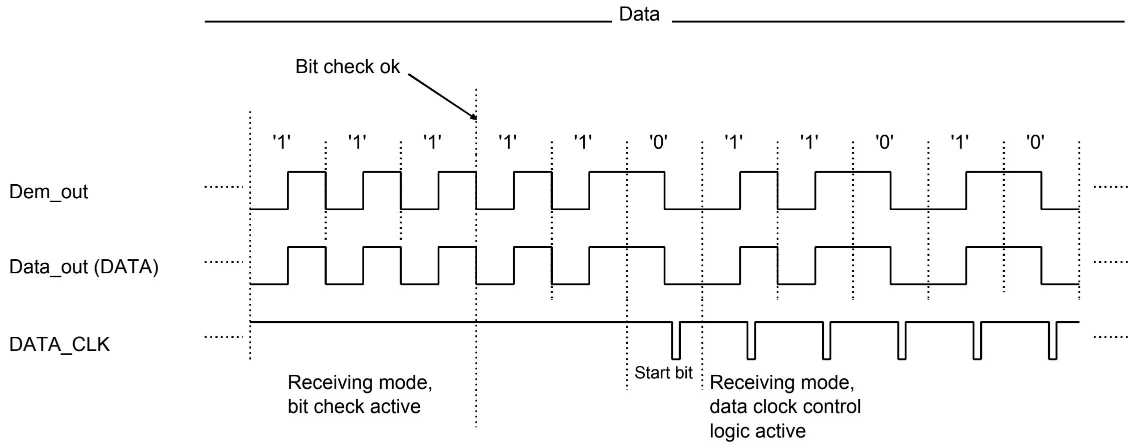


Figure 23. Output of the Data Clock After a Successful Bit Check



The delay of the data clock is calculated as follows: $t_{Delay} = t_{Delay1} + t_{Delay2}$

t_{Delay1} is the delay between the internal signals Data_Out and Data_In. For the rising edge, t_{Delay1} depends on the capacitive load C_L at Pin DATA and the external pull-up resistor R_{pup}. For the falling edge, t_{Delay1} depends additionally on the external voltage V_X (see Figure 24, Figure 25 and Figure 32). When the level of Data_In is equal to the level of Data_Out, the data clock is issued after an additional delay t_{Delay2}.

Note that the capacitive load at Pin DATA is limited. If the maximum tolerated capacitive load at Pin DATA is exceeded, the data clock disappears (see chapter 'Data Interface').

Figure 24. Timing Characteristic of the Data Clock (Rising Edge on Pin DATA)

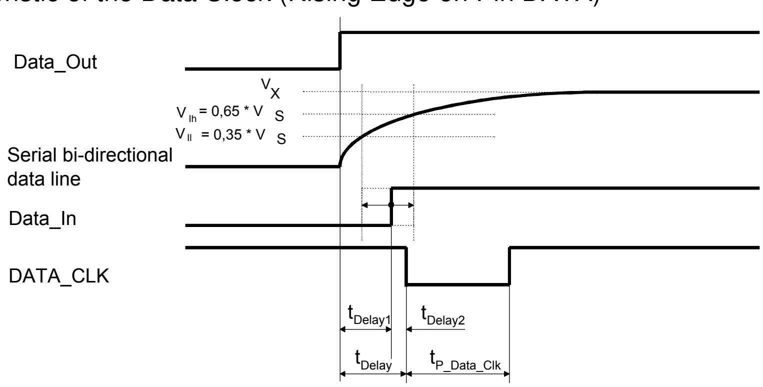
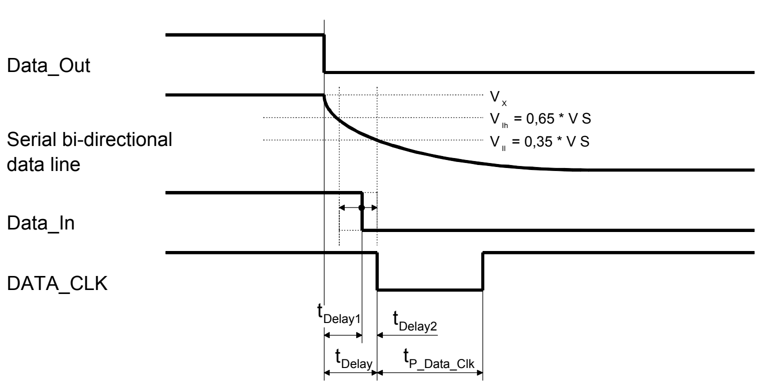


Figure 25. Timing Characteristic of the Data Clock (Falling Edge of the Pin DATA)



Digital Noise Suppression

After a data transmission, digital noise appears on the data output (see Figure 26). Preventing that digital noise keeps the connected microcontroller busy. It can be suppressed in two different ways.

Automatic Noise Suppression

If the bit Noise_Disable (Table 9) in the OPMODE register is set to 1 (default), the receiver changes to bit-check mode at the end of a valid data stream. The digital noise is suppressed and the level at Pin DATA is High in that case. The receiver changes back to receiving mode, if the bit check was successful.

This way to suppress the noise is recommended if the data stream is Manchester or Bi-phase coded and is active after power on.

Figure 28 illustrates the behavior of the data output at the end of a data stream. Note that if the last period of the data stream is a high period (rising edge to falling edge), a pulse occurs on Pin DATA. The length of the pulse depends on the selected baud-rate range.

Figure 26. Output of Digital Noise at the End of the Data Stream

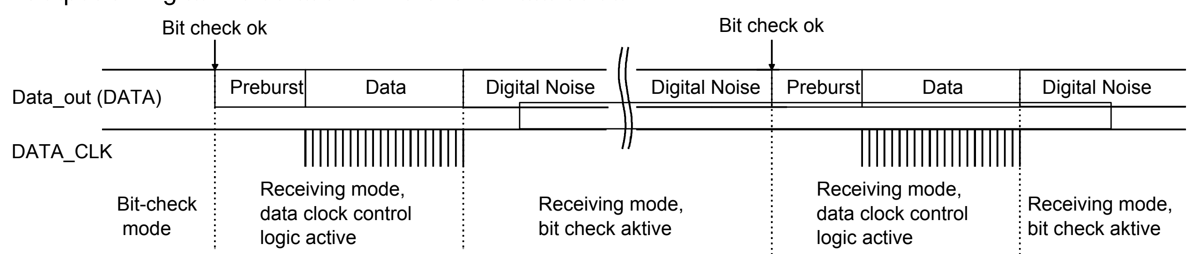


Figure 27. Automatic Noise Suppression

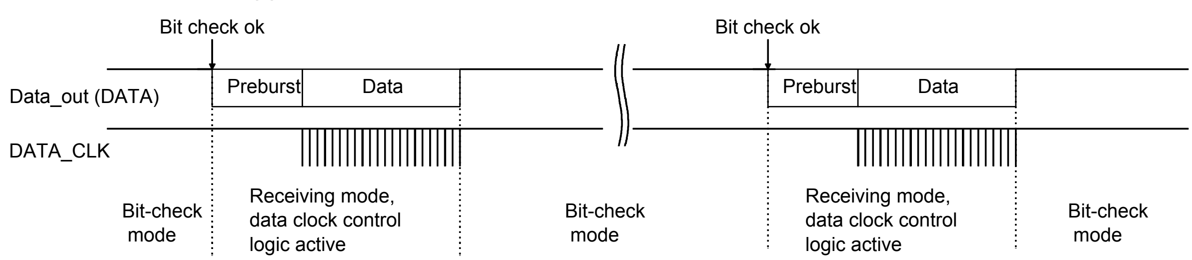
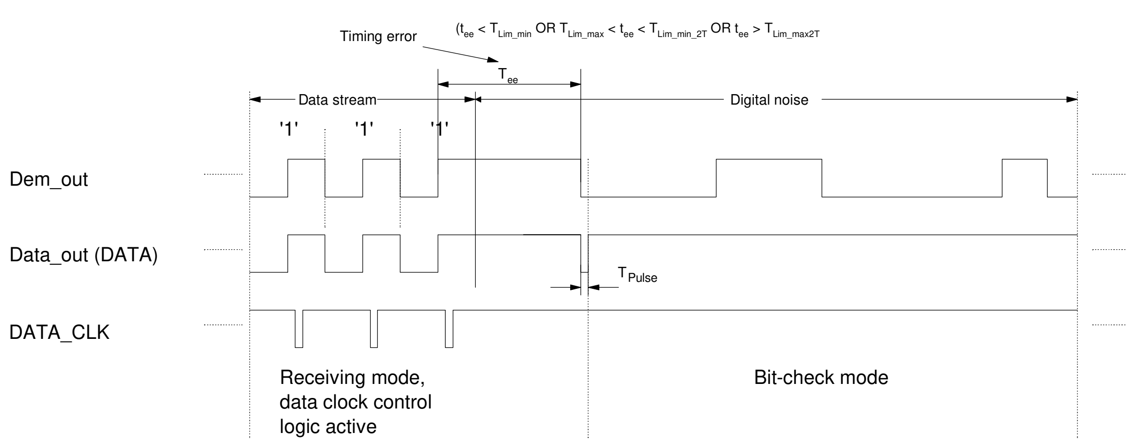
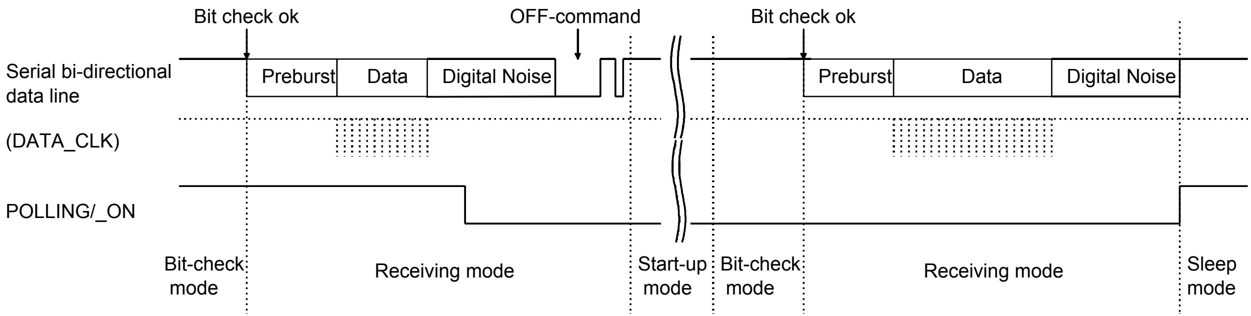


Figure 28. Occurrence of a Pulse at the End of the Data Stream



Controlled Noise Suppression by the Microcontroller

Figure 29. Controlled Noise Suppression



If the bit Noise_Disable (see Table 9) in the OPMODE register is set to 0, digital noise appears at the end of a valid data stream. To suppress the noise, the Pin POLLING/_ON must be set to Low. The receiver remains in receiving mode. Then, the OFF command causes the change to the start-up mode. The programmed sleep time (see Table 7) will not be executed because the level at Pin POLLING/_ON is low, but the bit check is active in that case. The OFF command activates the bit check also if the Pin POLLING/_ON is held to Low. The receiver changes back to receiving mode if the bit check was successful. To activate the polling mode at the end of the data transmission, the Pin POLLING/_ON must be set to High. This way of suppressing the noise is recommended if the data stream is not Manchester or Bi-phase coded.

Configuration of the Receiver

The T5760/T5761 receiver is configured via two 12-bit RAM registers called OPMODE and LIMIT. The registers can be programmed by means of the bidirectional DATA port. If the register contents have changed due to a voltage drop, this condition is indicated by a certain output pattern called reset marker (RM). The receiver must be reprogrammed in that case. After a Power-On Reset (POR), the registers are set to default mode. If the receiver is operated in default mode, there is no need to program the registers. Table 3 shows the structure of the registers. According to Table 2, bit 1 defines if the receiver is set back to polling mode via the OFF command (see chapter ’Receiving Mode’) or if it is programmed. Bit 2 represents the register address. It selects the appropriate register to be programmed. To get a high programming reliability, Bit 15 (Stop bit), at the end of the programming operation, must be set to 0.

Table 1. Effect of Bit 1 and Bit 2 on Programming the Registers

Bit 1	***Bit 2***	***Action***
1	x	The receiver is set back to polling mode (OFF command)
0	1	The OPMODE register is programmed
0	0	The LIMIT register is programmed

Table 2. Effect of Bit 15 on Programming the Register

Bit 15	***Action***
0	The values will be written into the register (OPMODE or LIMIT)
1	The values will not be written into the register

Table 3. Effect of the Configuration Words within the Registers

Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7	Bit 8	Bit 9	Bit 10	Bit 11	Bit 12	Bit 13	Bit 14	Bit 15
OFF command														
1	–	–	–	–	–	–	–	–	–	–	–	–	–	–
–		OPMODE register												–
0	1	BR_Range		$N_{Bit-check}$		Modu-lation	Sleep					X Sleep	Noise Suppres sion	0
		Baud1	Baud0	BitChk1	BitChk0	ASK/_FSK	Sleep4	Sleep3	Sleep2	Sleep1	Sleep0	$X_{Sleep Std}$	Noise_ Disable	
Default values of Bit 3...14		0	0	0	1	0	0	0	1	1	0	0	1	–
–		LIMIT register												–
0	0	Lim_min						Lim_max						–
		Lim_ min5	Lim_ min4	Lim_ min3	Lim_ min2	Lim_ min1	Lim_ min0	Lim_ max5	Lim_ max4	Lim_ max3	Lim_ max2	Lim_ max1	Lim_ max0	0
Default values of Bit 3...14		0	1	0	1	0	1	1	0	1	0	0	1	–

The following tables illustrate the effect of the individual configuration words. The default configuration is highlighted for each word.

BR_Range sets the appropriate baud-rate range and simultaneously defines XLim. XLim is used to define the bit-check limits T_{Lim_min} and T_{Lim_max} as shown in Table 10 and Table 11.

Table 4. Effect of the configuration word BR_Range

BR_Range		
Baud1	**Baud0**	**Baud-rate Range/Extension Factor for Bit-check Limits (XLim)**
0	0	BR_Range0 (application USA/Europe: BR_Range0 = 1.0 kBaud to 1.8 kBaud) XLim = 8 (default)
0	1	BR_Range1 (application USA/Europe: BR_Range1 = 1.8 kBaud to 3.2 kBaud) XLim = 4
1	0	BR_Range2 (application USA/Europe: BR_Range2 = 3.2 kBaud to 5.6 kBaud) XLim = 2
1	1	BR_Range3 (Application USA/Europe: BR_Range3 = 5.6 kBaud to 10 kBaud) XLim = 1

Table 5. Effect of the Configuration word $N_{Bit-check}$

$N_{Bit-check}$		
BitChk1	**BitChk0**	**Number of Bits to be Checked**
0	0	0
0	1	3 (default)
1	0	6
1	1	9

Table 6. Effect of the Configuration Bit Modulation

Modulation	Selected Modulation
ASK/_FSK	–
0	FSK (default)
1	ASK

Table 7. Effect of the Configuration Word Sleep

Sleep					Start Value for Sleep Counter
Sleep4	Sleep3	Sleep2	Sleep1	Sleep0	(T_{Sleep} = Sleep × Xsleep × 1024 × T_{Clk})
0	0	0	0	0	0 (Receiver is continuously polling until a valid signal occurs)
0	0	0	0	1	1 (T_{Sleep} ≈ 2.1 ms for XSleep = 1 and f_{RF} = 868.3 ms, ≈ 2.0 ms for f_{RF} = 915 MHz)
0	0	0	1	0	2
0	0	0	1	1	3
...	...	...	...	...	...
0	0	1	1	0	6 (T_{Sleep} = 12.695 ms for f_{RF} = 868.3 MHz, 12.047 ms for f_{RF} = 915 MHz) (default)
...	...	...	...	...	...
1	1	1	0	1	29
1	1	1	1	0	30
1	1	1	1	1	31 (permanent sleep mode)

Table 8. Effect of the Configuration Bit XSleep

XSleep	Extension Factor for Sleep Time
$XSleep_{Std}$	(TSleep = Sleep × Xsleep × 1024 × T_{Clk})
0	1 (default)
1	8

Table 9. Effect of the Configuration Bit Noise Suppression

Noise Suppression	
Noise_Disable	Suppression of the Digital Noise at Pin DATA
0	Noise suppression is inactive
1	Noise suppression is active (default)

Table 10. Effect of the Configuration Word Lim_min

Lim_min [1] *(Lim_min < 10 is not Applicable)*						*Lower Limit Value for Bit Check*
Lim_min5	*Lim_min4*	*Lim_min3*	*Lim_min2*	*Lim_min1*	*Lim_min0*	*(T_{Lim_min} = Lim_min × XLim × T_{Clk})*
0	0	1	0	1	0	10
0	0	1	0	1	1	11
0	0	1	1	0	0	12
..	..	..	..	..	..	
0	1	0	1	0	1	21 (default) (T_{Lim_min} = 347 µs for f_{RF} = 868.3 MHz and BR_Range0 T_{Lim_min} = 329 µs for f_{RF} = 915 MHz and BR_Range0)
..	..	..	..	..	..	
1	1	1	1	0	1	61
1	1	1	1	1	0	62
1	1	1	1	1	1	63

Note: 1. Lim_min is also used to determine the margins of the data clock control logic (see chapter 'Data Clock').

Table 11. Effect of the Configuration Word Lim_max

Lim_max [1] *(Lim_max < 12 is not applicable)*						*Upper Limit Value for Bit Check*
Lim_max5	*Lim_max4*	*Lim_max3*	*Lim_max2*	*Lim_max1*	*Lim_max0*	*(TLim_max = (Lim_max - 1) × XLim × T_{Clk})*
0	0	1	1	0	0	12
0	0	1	1	0	1	13
0	0	1	1	1	0	14
..	..	..	..	..	..	
1	0	1	0	0	1	41 (default) (TLim_max = 661 µs for f_{RF} = 868.3 MHz and BR_Range0, TLim_max = 627 µs for f_{RF} = 915 MHz and BR_Range0)
..	..	..	..	..	..	
1	1	1	1	0	1	61
1	1	1	1	1	0	62
1	1	1	1	1	1	63

Note: 1. Lim_max is also used to determine the margins of the data clock control logic (see chapter 'Data Clock').

Conservation of the Register Information

The T5760/T5761 implies an integrated power-on reset and brown-out detection circuitry to provide a mechanism to preserve the RAM register information.

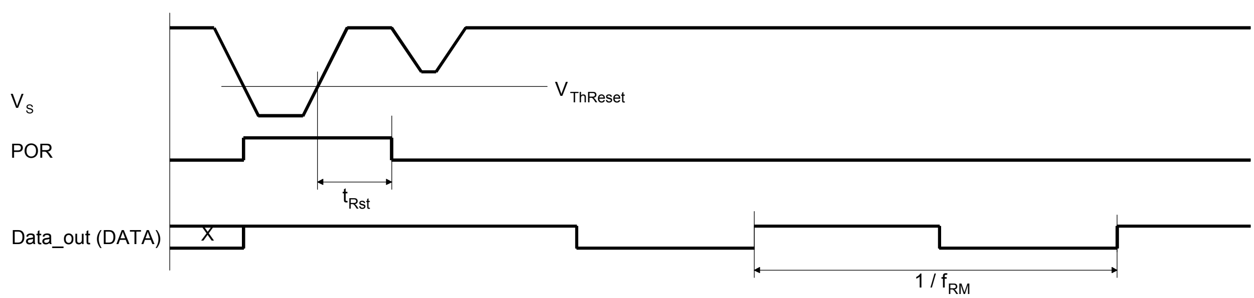
According to Figure 30, a power-on reset (POR) is generated if the supply voltage V_S drops below the threshold voltage $V_{ThReset}$. The default parameters are programmed into the configuration registers in that condition. Once V_S exceeds $V_{ThReset}$ the POR is canceled after the minimum reset period t_{Rst}. A POR is also generated when the supply voltage of the receiver is turned on.

To indicate that condition, the receiver displays a reset marker (RM) at Pin DATA after a reset. The RM is represented by the fixed frequency f_{RM} at a 50% duty-cycle. RM can be canceled via a Low pulse t1 at Pin DATA. The RM implies the following characteristics:

- f_{RM} is lower than the lowest feasible frequency of a data signal. By this means, RM cannot be misinterpreted by the connected microcontroller.
- If the receiver is set back to polling mode via Pin DATA, RM cannot be canceled by accident if t1 is applied according to the proposal in the section "Programming the Configuration Registers".

By means of that mechanism the receiver cannot lose its register information without communicating that condition via the reset marker RM.

Figure 30. Generation of the Power-on Reset



Programming the Configuration Register

Figure 31. Timing of the Register Programming

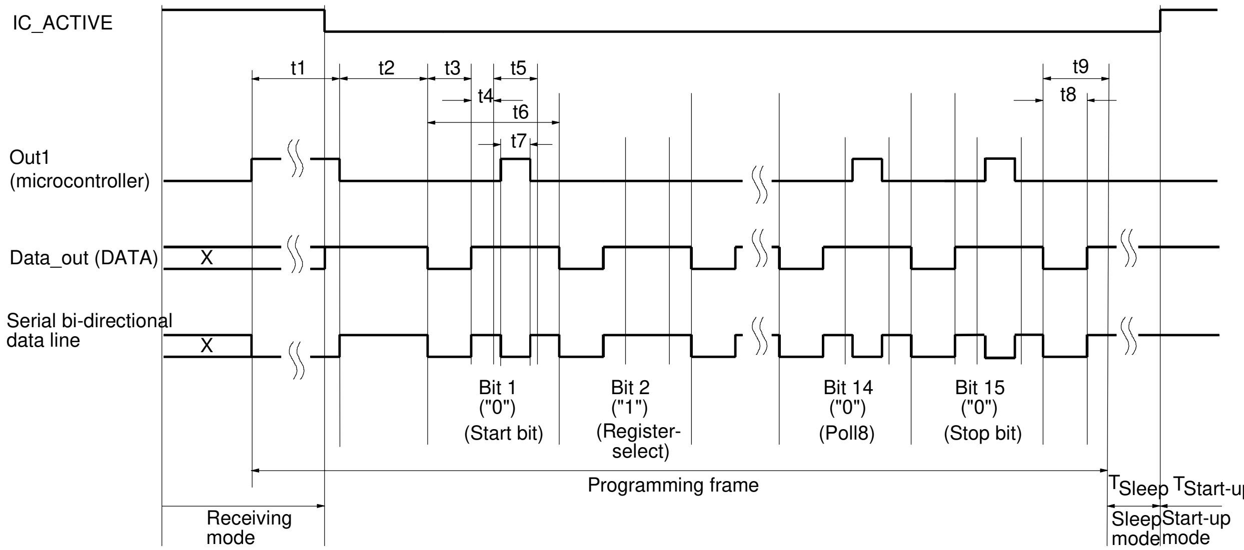
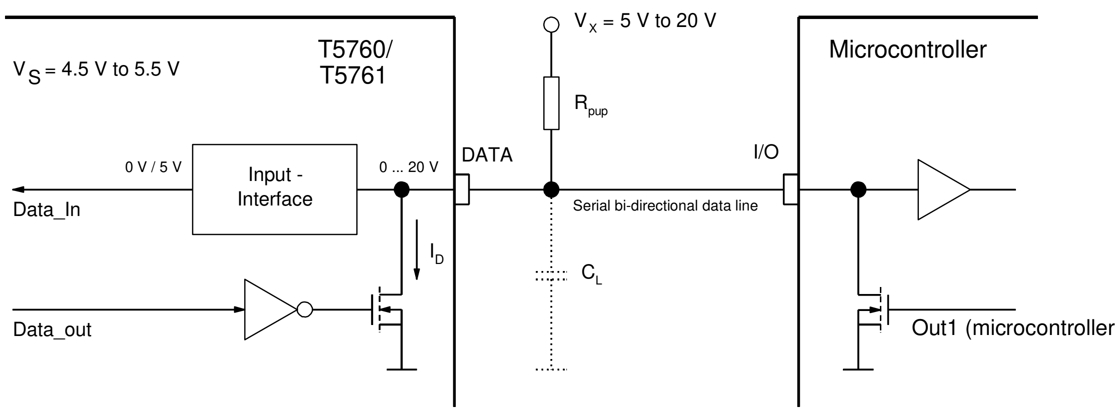


Figure 32. Data Interface



The configuration registers are programmed serially via the bi-directional data line according to Figure 31 and Figure 32.

To start programming, the serial data line DATA is pulled to Low for the time period t1 by the microcontroller. When DATA has been released, the receiver becomes the master device. When the programming delay period t2 has elapsed, it emits 15 subsequent synchronization pulses with the pulse length t3. After each of these pulses, a programming window occurs. The delay until the program window starts is determined by t4, the duration is defined by t5. Within the programming window, the individual bits are set. If the microcontroller pulls down Pin DATA for the time period t7 during t5, the according bit is set to '0'. If no programming pulse t7 is issued, this bit is set to '1'. All 15 bits are subsequently programmed this way. The time frame to program a bit is defined by t6.