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## Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email \& Skype: info@chipsmall.com Web: www.chipsmall.com Address: A1208, Overseas Decoration Building, \#122 Zhenhua RD., Futian, Shenzhen, China

## Features



- Single 3-V Supply Voltage
- High Power-added Efficient Power Amplifier ( $P_{\text {out }}$ Typically 23 dBm)
- Ramp-controlled Output Power
- Low-noise Preamplifier (NF Typically 2.1 dB)
- Biasing for External PIN Diode T/R Switch
- Current-saving Standby Mode
- Few External Components
- Packages:
- PSSO20
- QFN20 with Extended Performance

Bluetooth ${ }^{\text {TM }} /$ ISM 2.4-GHz FrontEnd IC

Electrostatic sensitive device.
Observe precautions for handling.


## Description

The T7024 is a monolithic SiGe transmit/receive front-end IC with power amplifier, low-noise amplifier and T/R switch driver. It is especially designed for operation in TDMA systems like Bluetooth ${ }^{\text {TM }}$ and WDCT.
Due to the ramp-control feature and a very low quiescent current, an external switch transistor for $\mathrm{V}_{\mathrm{S}}$ is not required.

Figure 1. Block Diagram


## Pin Configuration

Figure 2. Pinning PSSO20


Figure 3. Pinning QFN20


## Pin Description

| Pins PSSO20 | Pins QFN20 | Symbol | Function |
| :---: | :---: | :---: | :--- |
| 1 | 4 | R_SWITCH | Resistor to GND sets the PIN diode current |
| 2 | 5 | SWITCH_OUT | Switched current output for PIN diode |
| 3 | 6 | GND | Ground |
| 4 | 7 | LNA_IN | Low-noise amplifier input |
| 5 | 9 | VS_LNA | Supply voltage input for low-noise amplifier |
| 6 | 8 | GND | Ground |
| 7 | 11 | V3_PA_OUT | Inductor to power supply and matching network for power amplifier output |
| 8 | 12 | V3_PA_OUT | Inductor to power supply and matching network for power amplifier output |
| 9 | 13 | V3_PA_OUT | Inductor to power supply and matching network for power amplifier output |
| 10 | 10 | GND | Ground |
| 11 | 15 | RAMP | Power ramping control input |
| 12 | 16 | V2_PA | Inductor to power supply for power amplifier |
| 13 | 17 | V2_PA | Inductor to power supply for power amplifier |
| 14 | 14 | GND | Ground |
| 15 | 19 | V1_PA | Supply voltage for power amplifier |
| 16 | 20 | PA_IN | Power amplifier input |
| 17 | 18 | GND | Ground |
| 18 | 1 | LNA_OUT | Low-noise amplifier output |
| 19 | 2 | RX_ON | RX active high |
| 20 | 3 | PU | Power-up active high |
| Slug | Slug | GND | Ground |

## Absolute Maximum Ratings

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

| Parameters | Symbol | Value | Unit |
| :--- | :---: | :---: | :---: |
| Supply voltage <br> Pins VS_LNA, V1_PA, V2_PA, V3_PA_OUT | $\mathrm{V}_{\mathrm{S}}$ | 6 | V |
| Junction temperature | $\mathrm{T}_{\mathrm{j}}$ | 150 | ${ }^{\circ} \mathrm{C}$ |
| Storage temperature | $\mathrm{T}_{\text {stg }}$ | -40 to +125 | ${ }^{\circ} \mathrm{C}$ |
| RF input power LNA | $\mathrm{P}_{\text {inLNA }}$ | 5 | dBm |
| RF input power PA | $\mathrm{P}_{\text {inPA }}$ | 10 | dBm |

## Thermal Resistance

| Parameters | Symbol | Value | Unit |
| :--- | :---: | :---: | :---: |
| Junction ambient PSSOP20, slug soldered on PCB | $\mathrm{R}_{\mathrm{thJA}}$ | 19 | $\mathrm{~K} / \mathrm{W}$ |
| Junction ambient QFN20, slug soldered on PCB | $\mathrm{R}_{\mathrm{thJA}}$ | 27 | $\mathrm{~K} / \mathrm{W}$ |

Do not operate this part near strong electrostatic fields. This IC meets class 1 ESD test requirement (HBM in accordance to EIA/JESD22-A114-A (October 97) and class A ESD test requirement (MM) in accordance to EIA/JESD22-A115A.

## Operating Range

All voltages are referred to ground (pins GND and slug). Power supply points are VS_LNA, V1_PA, V2_PA, V3_PA_OUT. The table represents the sum of all supply currents depending on the TX/RX mode.

| Parameters | Symbol | Min. | Typ. | Max. | Unit |
| :--- | :---: | :---: | :---: | :---: | :---: |
| Supply voltage <br> Pins V1_PA, V2_PA and V3_PA_OUT | $\mathrm{V}_{\mathrm{S}}$ | 2.7 | 3.0 | 4.6 | V |
| Supply voltage, pin VS_LNA | $\mathrm{V}_{\mathrm{S}}$ | 2.7 | 3.0 | 5.5 | V |
| Supply current TX, PSSO20 |  |  | 190 |  | mA |
| SFN20 | $\mathrm{I}_{\mathrm{S}}$ |  | 165 | mA |  |
| Supply current RX | $\mathrm{I}_{\mathrm{S}}$ |  | 8 | mA |  |
| Standby current, PU =0 | $\mathrm{I}_{\mathrm{S}}$ |  | 10 | $\mu \mathrm{~A}$ |  |
| Ambient temperature | $\mathrm{I}_{\text {S_standby }}$ |  |  | ${ }^{\circ} \mathrm{C}$ |  |

Electrical Characteristics
Test conditions (unless otherwise specified): $\mathrm{V}_{\mathrm{S}}=3.0 \mathrm{~V}, \mathrm{~T}_{\mathrm{amb}}=25^{\circ} \mathrm{C}$

| Parameters | Test Conditions | Symbol | Min. | Typ. | Max. | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Power Amplifier ${ }^{(1)}$ |  |  |  |  |  |  |
| Supply voltage | Pins V1_PA, V2_PA, V3_PA_OUT | $\mathrm{V}_{\mathrm{S}}$ | 2.7 | 3.0 | 4.6 | V |
| Supply current | TX PSSO20 <br> TX QFN20 | $\begin{aligned} & \mathrm{I}_{\mathrm{S}_{-} T \mathrm{X}} \\ & \mathrm{I}_{\mathrm{S}_{-}} \end{aligned}$ |  | $\begin{aligned} & 190 \\ & 165 \end{aligned}$ |  | $\begin{aligned} & \mathrm{mA} \\ & \mathrm{~mA} \end{aligned}$ |
|  | RX (PA off), $\mathrm{V}_{\text {RAMP }} \leq 0.1 \mathrm{~V}$ | $\mathrm{I}_{\text {S_RX }}$ |  |  | 10 | $\mu \mathrm{A}$ |
| Standby current | Standby | $\mathrm{I}_{\text {S_standby }}$ |  |  | 10 | $\mu \mathrm{A}$ |
| Frequency range | TX | f | 2.4 |  | 2.5 | GHz |
| Gain-control range | TX | $\Delta \mathrm{Gp}$ | 60 | 42 |  | dB |
| Power gain maximum | TX, pin PA_IN to V3_PA_OUT | Gp | 28 | 30 | 33 | dB |
| Power gain minimum | TX, pin PA_IN to V3_PA_OUT | Gp | -40 |  | -17 | dB |
| Ramping voltage maximum | TX, power gain (maximum) Pin RAMP | $V_{\text {RAMP max }}$ | 1.7 | 1.75 | 1.83 | V |
| Ramping voltage minimum | TX, power gain (minimum) Pin RAMP | $\mathrm{V}_{\text {RAMP min }}$ |  | 0.1 |  | V |
| Ramping current maximum | TX, $\mathrm{V}_{\text {RAMP }}=1.75 \mathrm{~V}$, pin RAMP | $I_{\text {RAMP max }}$ |  |  | 0.5 | mA |
| Power-added efficiency | TX PSSO20 <br> TX QFN20 | $\begin{aligned} & \text { PAE } \\ & \text { PAE } \end{aligned}$ | $\begin{aligned} & 30 \\ & 35 \end{aligned}$ | $\begin{aligned} & 35 \\ & 40 \end{aligned}$ |  | $\begin{aligned} & \hline \% \\ & \% \end{aligned}$ |
| Saturated output power | TX, input power $=0 \mathrm{dBm}$ referred to pins V3_PA_OUT | $\mathrm{P}_{\text {sat }}$ | 22 | 23 | 24 | dBm |
| Input matching ${ }^{(2)}$ | TX, pin PA_IN | Load VSWR |  | < 1.5:1 |  |  |
| Output matching ${ }^{(2)}$ | TX, pins V3_PA_OUT | Load VSWR |  | < 1.5:1 |  |  |
| Harmonics at $\mathrm{P}_{\text {sat }}=23 \mathrm{dBm}$ | TX, pins V3_PA_OUT | 2 fo |  |  | -30 | dBc |
|  | TX, pins V3_PA_OUT | 3 fo |  |  | -30 | dBc |
| T/R Switch Driver (Current Programming by External Resistor from R_SWITCH to GND) |  |  |  |  |  |  |
| Switch-out current output | Standby, pin SWITCH_OUT | $\mathrm{I}_{\text {S_O_standby }}$ |  |  | 1 | $\mu \mathrm{A}$ |
|  | RX | $\mathrm{IS}_{\text {_O_RX }}$ |  |  | 1 | $\mu \mathrm{A}$ |
|  | TX at $100 \Omega$ | $\mathrm{I}_{\text {S_O_100 }}$ |  | 1.7 |  | mA |
|  | TX at $1.2 \mathrm{k} \Omega$ | $\mathrm{l}_{\text {S_O_1k2 }}$ |  | 7 |  | mA |
|  | TX at $33 \mathrm{k} \Omega$ | $\mathrm{l}_{\text {S_O_33k }}$ |  | 17 |  | mA |
|  | TX at $\infty$ | IS _O_R |  | 19 |  | mA |
| Low-noise Amplifier ${ }^{(3)}$ |  |  |  |  |  |  |
| Supply voltage | All, pin VS_LNA | $\mathrm{V}_{\text {S }}$ | 2.7 | 3.0 | 5.5 | V |
| Supply current | RX | $\mathrm{I}_{\mathrm{s}}$ |  | 8 | 9 | mA |

Notes: 1. Power amplifier shall be unconditionally stable, maximum duty cycle $100 \%$, true CW operation, maximum load mismatch and duration: load VSWR $=10: 1$ (all phases) $10 \mathrm{~s}, \mathrm{Z}_{\mathrm{G}}=50 \Omega$
2. With external matching network, load impedance $50 \Omega$
3. Low-noise amplifier shall be unconditionally stable.
4. With external matching components.
5. LNA gain can be adjusted with RX_ON voltage according to Figure 19 on page 11. Please note, that for RX_ON below 1.4 V the T/R switch driver switches to TX mode.

## Electrical Characteristics (Continued)

Test conditions (unless otherwise specified): $\mathrm{V}_{\mathrm{S}}=3.0 \mathrm{~V}, \mathrm{~T}_{\mathrm{amb}}=25^{\circ} \mathrm{C}$

| Parameters | Test Conditions | Symbol | Min. | Typ. | Max. | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Supply current (LNA and control logic) | TX (control logic active) Pin VS_LNA | $\mathrm{I}_{\text {S }}$ |  |  | 0.5 | mA |
| Standby current | Standby, pin VS_LNA | $\mathrm{IS}_{\text {_standby }}$ |  | 1 | 10 | $\mu \mathrm{A}$ |
| Frequency range | RX | f | 2.4 |  | 2.5 | GHz |
| Power gain ${ }^{(5)}$ | RX, pin LNA_IN to LNA_OUT | Gp | 15 | 16 | 19 | dB |
| Noise figure | RX PSSO20 <br> RX QFN20 | $\begin{aligned} & \text { NF } \\ & \text { NF } \end{aligned}$ |  | $\begin{aligned} & 2.5 \\ & 2.1 \end{aligned}$ | $\begin{aligned} & 2.8 \\ & 2.3 \end{aligned}$ | $\begin{aligned} & \mathrm{dB} \\ & \mathrm{~dB} \end{aligned}$ |
| Gain compression | RX, referred to pin LNA_OUT | O1dB | -9 | -7 | -6 | dBm |
| $3{ }^{\text {rd }}$-order input interception point | RX | IIP3 | -16 | -14 | -13 | dBm |
| Input matching ${ }^{(4)}$ | RX, pin LNA_IN | VSWRin |  |  | 2:1 |  |
| Output matching ${ }^{(4)}$ | RX, pin LNA_OUT | VSWRout |  |  | 2:1 |  |
| Logic Input Levels (RX_ON, PU) ${ }^{(5)}$ |  |  |  |  |  |  |
| High input level | = '1' pins RX_ON and PU | $\mathrm{V}_{\mathrm{iH}}$ | 2.4 |  | $\mathrm{V}_{\mathrm{S}, \text { LNA }}$ | V |
| Low input level | = '0' | $\mathrm{V}_{\mathrm{iL}}$ | 0 |  | 0.5 | V |
| High input current | $={ }^{\prime} 1^{\prime} \mathrm{V}_{\mathrm{iH}}=2.4 \mathrm{~V}$ | $\mathrm{I}_{\mathrm{iH}}$ |  | 40 | 60 | $\mu \mathrm{A}$ |
| Low input current | = '0' | $\mathrm{I}_{\mathrm{iL}}$ |  |  | 0.2 | $\mu \mathrm{A}$ |

Notes: 1. Power amplifier shall be unconditionally stable, maximum duty cycle $100 \%$, true CW operation, maximum load mismatch and duration: load VSWR $=10: 1$ (all phases) $10 \mathrm{~s}, \mathrm{Z}_{\mathrm{G}}=50 \Omega$
2. With external matching network, load impedance $50 \Omega$
3. Low-noise amplifier shall be unconditionally stable.
4. With external matching components.
5. LNA gain can be adjusted with RX_ON voltage according to Figure 19 on page 11. Please note, that for RX_ON below 1.4 V the T/R switch driver switches to TX mode.

## Control Logic PA and LNA/Antenna Switch Driver

| PU | RX_ON | Ramp $^{(1)}$ | PA | LNA | Antenna Switch Driver | Operation Mode |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| 0 | 0 | 0 | off | off | off | standby |
| 0 | 0 | 1 | on | off | off | $(2)$ |
| 0 | 1 | 0 | off | on | off | $(3)$ |
| 0 | 1 | 1 | on | on | off | $(4)$ |
| 1 | 0 | 0 | off | off | on | $(4)$ |
| 1 | 0 | 1 | on | off | on | TX |
| 1 | 1 | 0 | off | on | off | RX |
| 1 | 1 | on | on | off | $(5)$ |  |

Notes: 1. " 0 " $=\mathrm{V}_{\text {RAMP }} \leq 0.1 \mathrm{~V}$, " 1 " $=\mathrm{V}_{\text {RAMP }}$ typically $1.75 \mathrm{~V}, 1.3 \mathrm{~V}<\mathrm{V}_{\text {RAMP }}<1.83 \mathrm{~V}$ controls gain and output power, compare Figure 9 on page 7 and Figure 13 on page 9
2. Only for special operation, e.g. only PA operation, no LNA/switch driver operation
3. Only for special operation, e.g. no switch driver operation
4. Only for special operation
5. Only for special operation, e.g. separate $T X / R X$ antennas, $T X$ and $R X$ operation at the same time

Typical Operating Characteristics

Figure 4. LNA (PSSO20): Gain and Noise Figure versus Frequency


Figure 5. LNA (N20): Gain and Noise Figure versus Frequency


Figure 6. LNA: NF and Gain versus Temperature


Figure 7. LNA: Typical Switch-out Current versus $\mathrm{R}_{\text {switch }}$


Figure 8. PA (PSSO20): Output Power and PAE versus Supply


Figure 9. PA (PSSO20): Output Power and PAE versus Ramp Voltage


Figure 10. PA (PSSO20): Output Power and PAE versus Input Power


Figure 11. PA (PSSO20): Output Power and PAE versus Frequency


Figure 12. PA (QFN20): Output Power and PAE versus Supply Voltage


Figure 13. PA (QFN20) Output Power and PAE versus Ramp Voltage


Figure 14. PA (QFN20): Output Power and PAE versus Input Power


Figure 15. PA (QFN20): Output Power and PAE versus Frequency


Figure 16. LNA: Supply Current versus Temperature


Figure 17. PA (PSSO20): Supply Current versus $\mathrm{I}_{\text {ramp }}$ and Temperature


Figure 18. PA (PSSO20, QFN20): $P_{\text {out }}$ versus $V_{\text {RAMP }}$ and Temperature


Figure 19. (PSSO20, QFN20): LNA Gain (dB) versus RX_ON (V)


Figure 20. Input Circuit PA_IN/V1_PA


Figure 21. Input Circuit RAMP/V1_PA


Figure 22．Input Circuit V2＿PA


Figure 23．Input／Output Circuit V3＿PA＿OUT


Figure 24．Input Circuit SWITCH＿OUT／R＿SWITCH


Figure 25. Input Circuit LNA_IN/VS_LNA


Figure 26. Input Circuit PU/RX_ON


Figure 27. Output Circuit LNA_OUT


Figure 28. Typical Application T7024 (PSSO20 Package)


Figure 29. Typical Application T7024 (QFN20 Package)
LNA OUT
 LED on application-board

Switch Out
PA OUT
blocking capacitors depending on application

## Ordering Information

| Extended Type Number | Package | Remarks | MOQ |
| :--- | :---: | :--- | :--- |
| T7024-TRS | PSSO20 | Tube | 830 pcs. |
| T7024-TRQ | PSSO20 | Taped and reeled | 4000 pcs. |
| T7024-PGP | QFN20 | Taped and reeled | 1500 pcs. |
| T7024-PGQ | QFN20 | Taped and reeled | 6000 pcs. |
| T7024-PGPM | QFN20 | Taped and reeled <br> Pb free, halogen free | 1500 pcs. |
| T7024-PGQM | Taped and reeled <br> Pb free, halogen free | 6000 pcs. |  |
| Demoboard-T7024-PG | QFN20 | Evaluation board QFN | 1 |
| Demoboard-T7024-TR | PSSO20 | Evaluation board PSSO | 1 |

## Package Information

Package: QFN 20-5x5
Exposed pad $3.1 \times 3.1$
(acc. JEDEC OUTLIN: N№. MO-220)
Dimensions in mm


Drawing-No: 6.543-5069.02-4
Issue: 3; 24.01.03


Drawing-No.:6.543-5078.01-4
Issue: 1: 05.06.01

Package Information PB Free

Package: QFN 20LD 5x5
Exposed pad $3.1 \times 3.1$


Drawing-No: 6.543-5094.01-4
Issue: 1 ; 19.12.02


technical drawings according to DIN specifications

## Recommended PCB Land Pattern

Figure 30. Recommended PCB Land Pattern


Table 1. Recommended PCB Land Pattern Signs

| Sign | Description | Size |
| :---: | :--- | :--- |
| A | Distance of vias | 1.6 mm |
| B | Size of slug pattern | 3.1 mm |
| C | Distance slug to pins | 0.33 mm |
| D | Diameter of vias | 1 mm |
| E | Width of pin pattern | 0.3 mm |
| F | Distance of pin pattern | 0.33 mm |

## Atmel Corporation

2325 Orchard Parkway
San Jose, CA 95131, USA
Tel: 1(408) 441-0311
Fax: 1(408) 487-2600

## Regional Headquarters

Europe<br>Atmel Sarl<br>Route des Arsenaux 41<br>Case Postale 80<br>CH-1705 Fribourg<br>Switzerland<br>Tel: (41) 26-426-5555<br>Fax: (41) 26-426-5500<br>Asia<br>Room 1219<br>Chinachem Golden Plaza<br>77 Mody Road Tsimshatsui<br>East Kowloon<br>Hong Kong<br>Tel: (852) 2721-9778<br>Fax: (852) 2722-1369<br>\section*{Japan}<br>9F, Tonetsu Shinkawa Bldg.<br>1-24-8 Shinkawa<br>Chuo-ku, Tokyo 104-0033<br>Japan<br>Tel: (81) 3-3523-3551<br>Fax: (81) 3-3523-7581

## Atmel Operations

Memory<br>2325 Orchard Parkway<br>San Jose, CA 95131, USA<br>Tel: 1(408) 441-0311<br>Fax: 1(408) 436-4314

## Microcontrollers

2325 Orchard Parkway
San Jose, CA 95131, USA
Tel: 1(408) 441-0311
Fax: 1(408) 436-4314
La Chantrerie
BP 70602
44306 Nantes Cedex 3, France
Tel: (33) 2-40-18-18-18
Fax: (33) 2-40-18-19-60
ASIC/ASSP/Smart Cards
Zone Industrielle
13106 Rousset Cedex, France
Tel: (33) 4-42-53-60-00
Fax: (33) 4-42-53-60-01
1150 East Cheyenne Mtn. Blvd.
Colorado Springs, CO 80906, USA
Tel: 1(719) 576-3300
Fax: 1(719) 540-1759
Scottish Enterprise Technology Park
Maxwell Building
East Kilbride G75 0QR, Scotland
Tel: (44) 1355-803-000
Fax: (44) 1355-242-743

## RF/Automotive

## Theresienstrasse 2

Postfach 3535
74025 Heilbronn, Germany
Tel: (49) 71-31-67-0
Fax: (49) 71-31-67-2340
1150 East Cheyenne Mtn. Blvd.
Colorado Springs, CO 80906, USA
Tel: 1(719) 576-3300
Fax: 1(719) 540-1759

## Biometrics/Imaging/Hi-Rel MPU/

High Speed Converters/RF Datacom
Avenue de Rochepleine
BP 123
38521 Saint-Egreve Cedex, France
Tel: (33) 4-76-58-30-00
Fax: (33) 4-76-58-34-80

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