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Features

- Single 3-V Supply Voltage
- High-power-added Efficient Power Amplifier (P_{out} Typically 28 dBm)
- Ramp-controlled Output Power
- Low-noise Preamplifier (NF Typically 2.1 dB)
- Biasing for External PIN Diode T/R Switch
- Current-saving Standby Mode
- Few External Components
- Package: QFN20



ISM 2.4 GHz Front End IC

1. Description

The T7026 is a monolithic SiGe transmit/receive front-end IC with power amplifier, low-noise amplifier and T/R switch driver. It is especially designed for operation in TDMA systems like DECT, IEEE 802.11 FHSS WLAN, home RF and ISM proprietary radios. Due to the ramp-control feature and a very low quiescent current, an external switch transistor for V_S is not required.

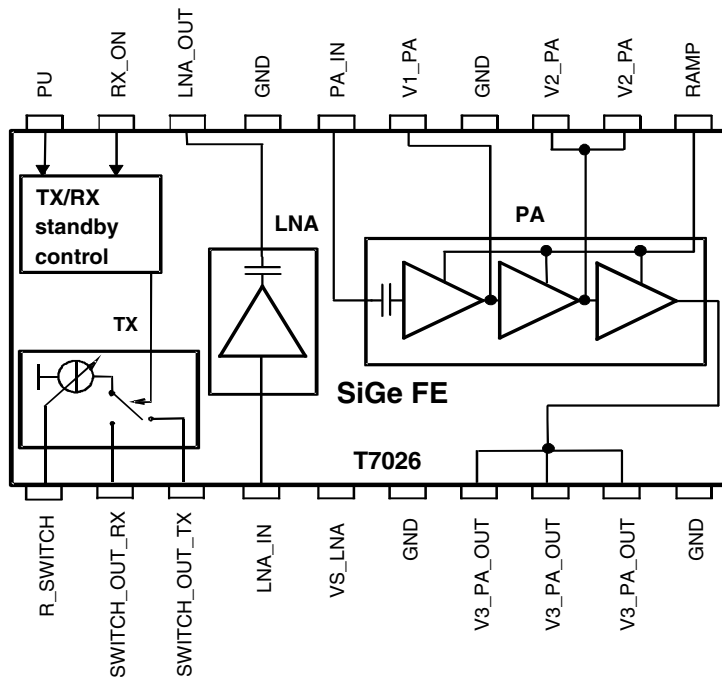
Electrostatic sensitive device.

Observe precautions for handling.



T7026

Figure 1-1. Block Diagram



2. Pin Configuration

Figure 2-1. Pinning QFN20

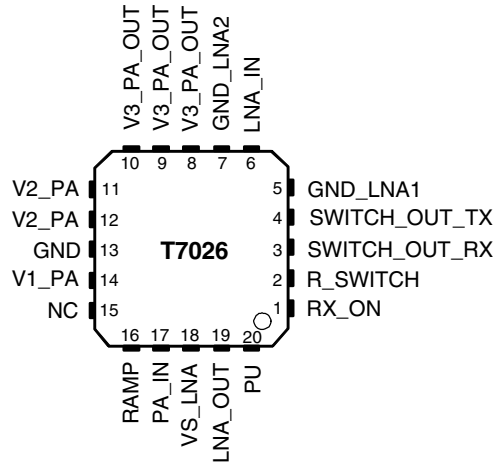


Figure 2-2. Pin Description

| Pin | Symbol | Function |
|------|---------------|--|
| 1 | RX_ON | RX active high |
| 2 | R_SWITCH | Resistor to GND sets the PIN diode current |
| 3 | SWITCH_OUT_RX | Switched current output for PIN diode (active in RX mode) |
| 4 | SWITCH_OUT_TX | Switched current output for PIN diode (active in TX mode) |
| 5 | GND_LNA1 | Ground |
| 6 | LNA_IN | Low-noise amplifier input |
| 7 | GND_LNA2 | Ground |
| 8 | V3_PA_OUT | Inductor to power supply and matching network for power amplifier output |
| 9 | V3_PA_OUT | Inductor to power supply and matching network for power amplifier output |
| 10 | V3_PA_OUT | Inductor to power supply and matching network for power amplifier output |
| 11 | V2_PA | Inductor to power supply for power amplifier |
| 12 | V2_PA | Inductor to power supply for power amplifier |
| 13 | GND | Ground |
| 14 | V1_PA | Supply voltage for power amplifier |
| 15 | NC | Not connected |
| 16 | RAMP | Power ramping control input |
| 17 | PA_IN | Power amplifier input |
| 18 | VS_LNA | Supply voltage input for low-noise amplifier |
| 19 | LNA_OUT | Low-noise amplifier output |
| 20 | PU | Power-up active high |
| Slug | GND | Ground |

3. Absolute Maximum Ratings

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

All voltages are referred to ground (pins GND and slug)

| Parameters | Symbol | Value | Unit |
|---|-------------|-------------|------|
| Supply voltage Pins VS_LNA, V1_PA, V2_PA and V3_PA_OUT, no RF | V_S | 5 | V |
| Junction temperature | T_j | 150 | °C |
| Storage temperature | T_{stg} | -40 to +125 | °C |
| RF input power LNA | P_{inLNA} | 5 | dBm |
| RF input power PA | P_{inPA} | 10 | dBm |

4. Thermal Resistance

| Parameters | Symbol | Value | Unit |
|---|------------|-------|------|
| Junction ambient QFN20, slug soldered on PCB | R_{thJA} | 27 | K/W |

5. Operating Range

All voltages are referred to ground (pins GND and slug). Power supply points are VS_LNA, V1_PA, V2_PA, V3_PA_OUT. The following table represents the sum of all supply currents depending on the TX/RX mode.

| Parameters | Symbol | Min. | Typ. | Max. | Unit |
|---|-----------|------|------|------|------|
| Supply voltage Pins V1_PA, V2_PA and V3_PA_OUT | V_S | 2.7 | 3.6 | 4.6 | V |
| Supply voltage Pin VS_LNA | V_S | 2.7 | 3.0 | 5.5 | V |
| Supply current TX | I_S | | 470 | | mA |
| RX | I_S | | 8 | | mA |
| Standby current PU = 0 | I_S | | 10 | | μA |
| Ambient temperature | T_{amb} | -25 | +25 | +70 | °C |

6. Electrical Characteristics

Test conditions (unless otherwise specified): $V_S = 3.6\text{ V}$, $T_{amb} = 25^\circ\text{C}$

| Parameters | Test Conditions | Symbol | Min. | Typ. | Max. | Unit |
|--|--|---------------------|------|---------|------|---------------|
| Power Amplifier⁽¹⁾ | | | | | | |
| Supply voltage | Pins V1_PA, V2_PA and V3_PA_OUT | V_S | 2.7 | 3.6 | 4.6 | V |
| Supply current | TX | I_{S_TX} | | 470 | | mA |
| | RX (PA off), $V_{RAMP} \leq 0.1\text{ V}$ | I_{S_RX} | | | 10 | μA |
| Standby current | Standby for $V_{RAMP} \leq 0.1\text{ V}$ | $I_{S_standby}$ | | | 10 | μA |
| Frequency range | TX | f | 2.4 | | 2.5 | GHz |
| Gain-control range | TX | ΔG_p | 60 | 42 | | dB |
| Power gain maximum | TX | G_p | 28 | 33 | 34 | dB |
| Power gain minimum | Pin PA_IN to V3_PA_OUT | G_p | -40 | | -17 | dB |
| Ramping voltage maximum | TX, power gain (max), pin RAMP | $V_{RAMP\ max}$ | 1.6 | 1.65 | 1.7 | V |
| Ramping voltage minimum | TX, power gain (min), pin RAMP | $V_{RAMP\ min}$ | | 1 | | V |
| Ramping current maximum | TX, $V_{RAMP} = 1.75\text{ V}$, pin RAMP | $I_{RAMP\ max}$ | | | 0.1 | mA |
| Power-added efficiency | TX | PAE | 33 | 37 | | % |
| Saturated output power | TX, input power = 0 dBm referred to pins V3_PA_OUT | P_{sat} | 27 | 28 | 29 | dBm |
| Input matching ⁽²⁾ | TX pin PA_IN | Load VSWR | | < 1.5:1 | | |
| Output matching ⁽²⁾ | TX pins V3_PA_OUT | Load VSWR | | < 1.5:1 | | |
| Harmonics at P 1dBCP | TX pins V3_PA_OUT | 2 fo | | -30 | | dBc |
| Harmonics at P 1dBCP | TX pins V3_PA_OUT | 3 fo | | -30 | | dBc |
| T/R-switch Driver (Current Programming by External Resistor from R_SWITCH to GND) | | | | | | |
| Switch-out current output | Standby, pin SWITCH_OUT | $I_{S_O_standby}$ | | | 1 | μA |
| | RX | $I_{S_O_RX}$ | | | 1 | μA |
| | TX at 100 Ω | $I_{S_O_100}$ | | 1.7 | | mA |
| | TX at 1.2 k Ω | $I_{S_O_1k2}$ | | 7 | | mA |
| | TX at 33 k Ω | $I_{S_O_33k}$ | | 17 | | mA |
| | TX at R switch open | $I_{S_O_R}$ | | 19 | | mA |
| $I_{Switch_Out_RX}$ maximum | | | | | 7 | mA |
| Low-noise Amplifier⁽³⁾ | | | | | | |
| Supply voltage | All, pin VS_LNA | V_S | 2.7 | 3.0 | 5 | V |
| Supply current | RX | I_S | | 8 | 10 | mA |
| Supply current (LNA and control logic) | TX (control logic active) pin VS_LNA | I_S | | | 0.5 | mA |
| Standby current | Standby, pin VS_LNA | $I_{S_standby}$ | | 1 | 10 | μA |
| Frequency range | RX | f | 2.4 | | 2.5 | GHz |

Notes: 1. Power amplifier shall be unconditionally stable, maximum duty cycle 100%, true cw operation, maximum load mismatch and duration: VSWR = 8:1 (all phases) 10 s, ZG = 50 Ω , $V_S = 3.6\text{ V}$.

2. With external matching network, load impedance 50 Ω

3. Low-noise amplifier shall be unconditionally stable.

4. With external matching components.

6. Electrical Characteristics (Continued)

Test conditions (unless otherwise specified): $V_S = 3.6\text{ V}$, $T_{\text{amb}} = 25^\circ\text{C}$

| Parameters | Test Conditions | Symbol | Min. | Typ. | Max. | Unit |
|--------------------------------------|------------------------------|----------|------|-------|--------------|---------------|
| Power gain | RX, pin LNA_IN to LNA_OUT | Gp | 15 | 16 | 19 | dB |
| Noise figure | RX | NF | | 2.1 | 2.3 | dB |
| Gain compression | RX, referred to pin LNA_OUT | O1dB | -9 | -7 | -6 | dBm |
| Third-order input interception point | RX | IIP3 | -16 | -14 | -13 | dBm |
| Input matching ⁽⁴⁾ | RX, pin LNA_IN | VSWRin | | < 2:1 | | |
| Output matching ⁽⁴⁾ | RX, pin LNA_OUT | VSWRout | | < 2:1 | | |
| Logic Input Levels (RX_ON, PU) | | | | | | |
| High input level | = 1, pins RX_ON and PU | V_{iH} | 2.4 | | $V_{S, LNA}$ | V |
| Low input level | = 0 | V_{iL} | 0 | | 0.5 | V |
| High input current | = 1, $V_{iH} = 2.4\text{ V}$ | I_{iH} | | 40 | 60 | μA |
| Low input current | = 0 | I_{iL} | | | 0.2 | μA |

- Notes:
1. Power amplifier shall be unconditionally stable, maximum duty cycle 100%, true cw operation, maximum load mismatch and duration: VSWR = 8:1 (all phases) 10 s, ZG = 50 Ω , $V_S = 3.6\text{ V}$.
 2. With external matching network, load impedance 50 Ω .
 3. Low-noise amplifier shall be unconditionally stable.
 4. With external matching components.

7. Control Logic for LNA and T/R-switch Driver

| Operation Mode | PU | RX_ON |
|----------------|----|-------|
| Standby | 0 | 0 |
| TX | 1 | 0 |
| RX | 1 | 1 |

8. Input/Output Circuits

Figure 8-1. Internal Circuitry; PA_IN, V1_PA

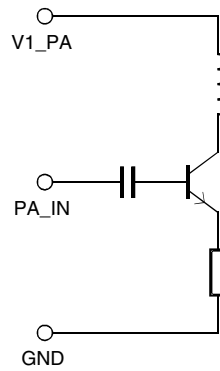


Figure 8-2. Internal Circuitry; RAMP, V1_PA

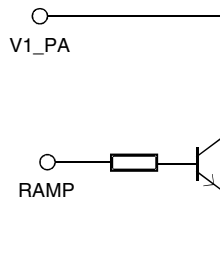


Figure 8-3. Internal Circuitry V2_PA

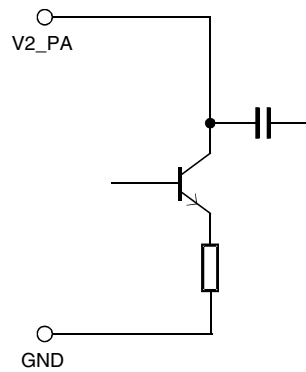


Figure 8-4. Internal Circuitry V3_PA_OUT

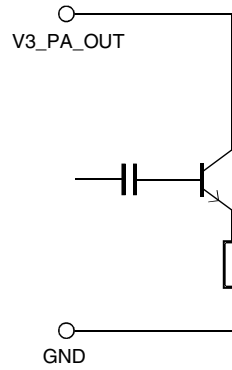


Figure 8-5. Internal Circuitry SWITCH_OUT_RX, SWITCH_OUT_TX, R_SWITCH, V1_PA

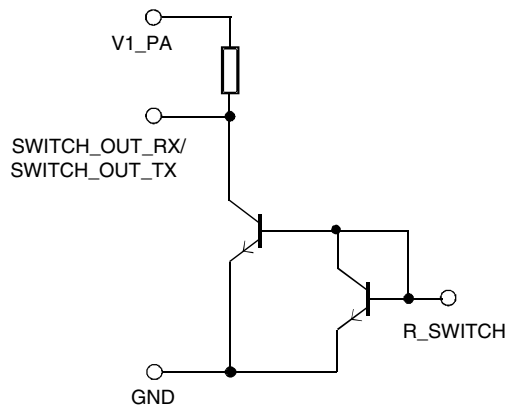


Figure 8-6. Internal Circuitry LNA_IN, VS_LNA

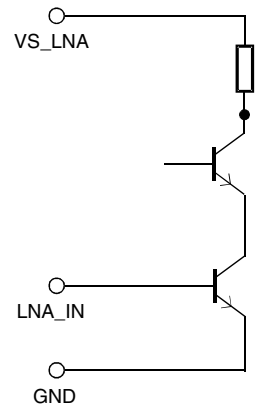


Figure 8-7. Internal Circuitry PU, RX_ON, VS_LNA

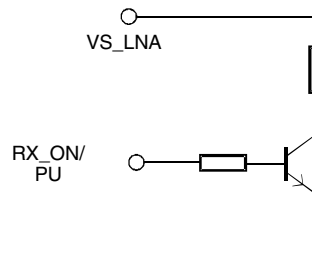
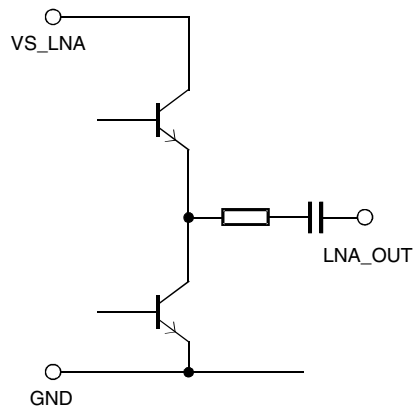


Figure 8-8. Internal Circuitry LNA_OUT, VS_LNA



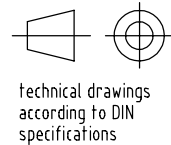
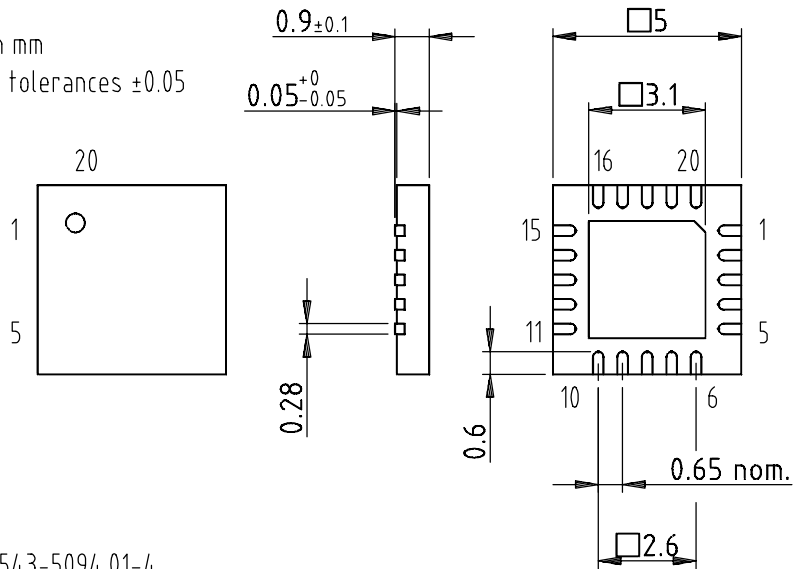
9. Ordering Information

| Extended Type Number | Package | Remarks | MOQ |
|----------------------|------------------------------|------------------|-------|
| T7026-PGQ | QFN20 | Taped and reeled | 6,000 |
| T7026-PGP | QFN20 | Taped and reeled | 1,500 |
| T7026-PGQW | QFN20, Pb-free, halogen-free | Taped and reeled | 6,000 |
| T7026-PGPW | QFN20, Pb-free, halogen-free | Taped and reeled | 1,500 |

10. Package Information

Package: QFN 20LD 5x5
Exposed pad 3.1 x 3.1

Dimensions in mm
Not indicated tolerances ±0.05



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