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## Features

- 80C51 Core Architecture
- 256 Bytes of On-chip RAM
- 1K Bytes of On-chip XRAM
- 32K Bytes of On-chip Flash Memory
  - Data Retention: 10 Years at 85°C
  - Erase/Write Cycle: 100K
- Boot Code Section with Independent Lock Bits
- 2K Bytes of On-chip Flash for Bootloader
- In-System Programming by On-Chip Boot Program (CAN, UART) and IAP Capability
- 2K Bytes of On-chip EEPROM
  - Erase/Write Cycle: 100K
- 14-sources 4-level Interrupts
- Three 16-bit Timers/Counters
- Full Duplex UART Compatible 80C51
- Maximum Crystal Frequency 40 MHz, in X2 Mode, 20 MHz (CPU Core, 20 MHz)
- Five Ports: 32 + 2 Digital I/O Lines
- Five-channel 16-bit PCA with:
  - PWM (8-bit)
  - High-speed Output
  - Timer and Edge Capture
- Double Data Pointer
- 21-bit Watchdog Timer (7 Programmable Bits)
- A 10-bit Resolution Analog to Digital Converter (ADC) with 8 Multiplexed Inputs
- Full CAN Controller:
  - Fully Compliant with CAN Rev2.0A and 2.0B
  - Optimized Structure for Communication Management (Via SFR)
  - 15 Independent Message Objects:
    - Each Message Object Programmable on Transmission or Reception
    - Individual Tag and Mask Filters up to 29-bit Identifier/Channel
    - 8-byte Cyclic Data Register (FIFO)/Message Object
    - 16-bit Status and Control Register/Message Object
    - 16-bit Time-Stamping Register/Message Object
    - CAN Specification 2.0 Part A or 2.0 Part B Programmable for Each Message Object
    - Access to Message Object Control and Data Registers Via SFR
    - Programmable Reception Buffer Length Up To 15 Message Objects
    - Priority Management of Reception of Hits on Several Message Objects at the Same Time (Basic CAN Feature)
    - Priority Management for Transmission
    - Message Object Overrun Interrupt
  - Supports:
    - Time Triggered Communication
    - Autobaud and Listening Mode
    - Programmable Automatic Reply Mode
  - 1-Mbit/s Maximum Transfer Rate at 8 MHz<sup>(1)</sup> Crystal Frequency in X2 Mode
  - Readable Error Counters
  - Programmable Link to On-chip Timer for Time Stamping and Network Synchronization
  - Independent Baud Rate Prescaler
  - Data, Remote, Error and Overload Frame Handling
- On-chip Emulation Logic (Enhanced Hook System)
- Power Saving Modes:
  - Idle Mode
  - Power-down Mode

1. At BRP = 1 sampling point will be fixed.



## Enhanced 8-bit Microcontroller with CAN Controller and Flash Memory

**T89C51CC01**  
**AT89C51CC01**



- Power Supply: 3V to 5.5V
- Temperature Range: Industrial (-40° to +85°C)
- Packages: VQFP44, PLCC44

## Description

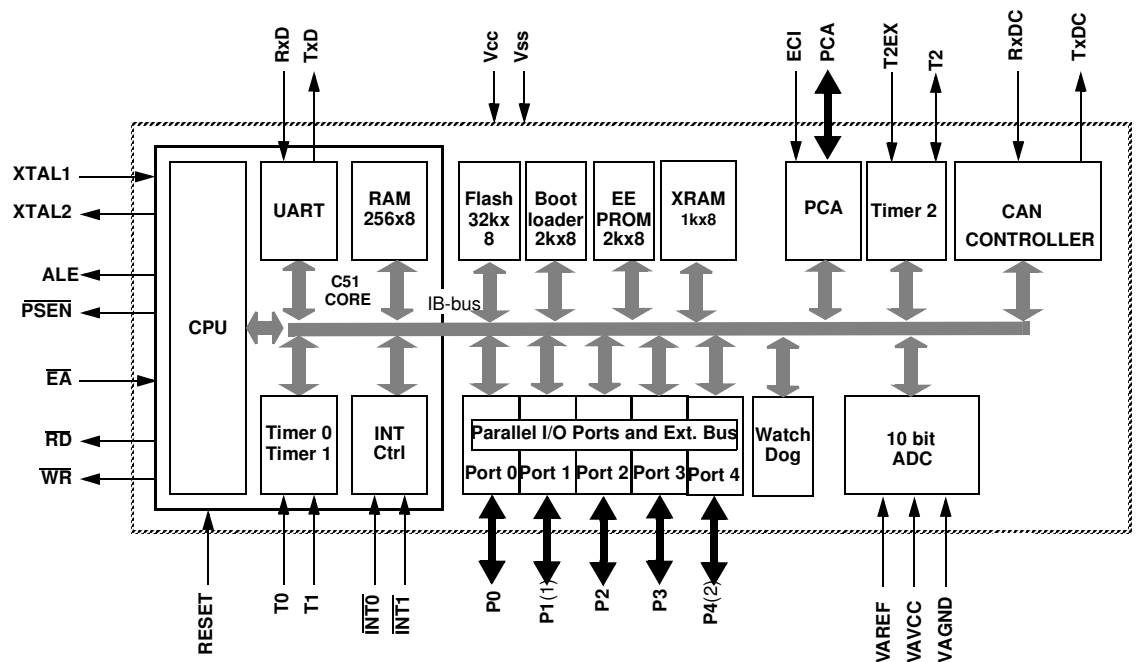
The T89C51CC01 is the first member of the CANary™ family of 8-bit microcontrollers dedicated to CAN network applications.

In X2 mode a maximum external clock rate of 20 MHz reaches a 300 ns cycle time.

Besides the full CAN controller T89C51CC01 provides 32K Bytes of Flash memory including In-System-Programming (ISP), 2K Bytes Boot Flash Memory, 2K Bytes EEPROM and 1.2-Kbyte RAM.

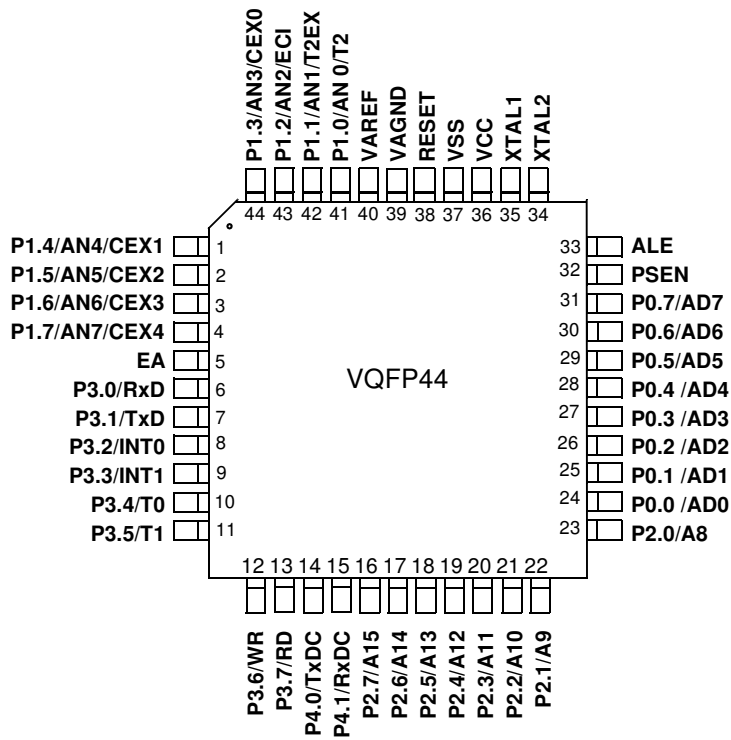
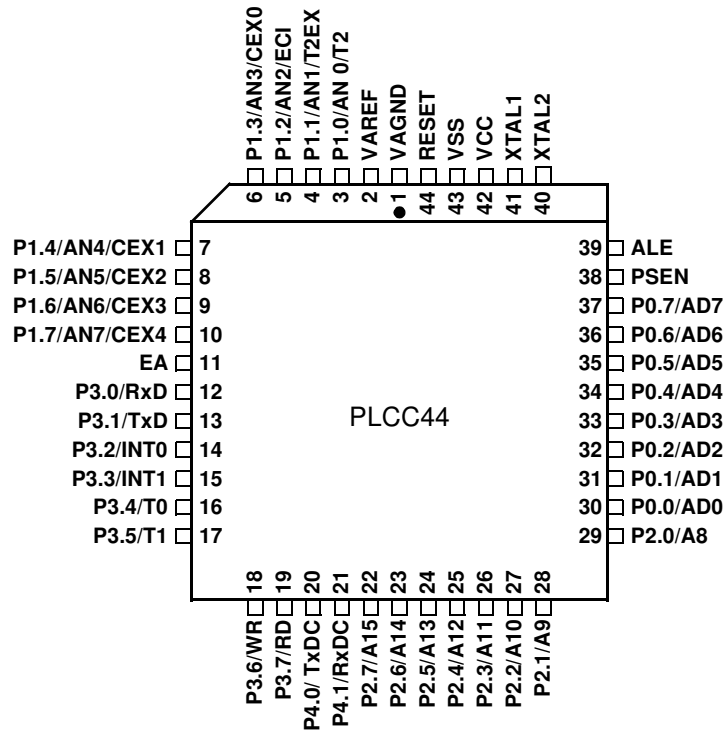
Special attention is paid to the reduction of the electro-magnetic emission of T89C51CC01.

## Block Diagram



- Notes:
1. 8 analog Inputs/8 Digital I/O
  2. 2-Bit I/O Port

Pin Configuration





## I/O Configurations

Each Port SFR operates via type-D latches, as illustrated in Figure 1 for Ports 3 and 4. A CPU "write to latch" signal initiates transfer of internal bus data into the type-D latch. A CPU "read latch" signal transfers the latched Q output onto the internal bus. Similarly, a "read pin" signal transfers the logical level of the Port pin. Some Port data instructions activate the "read latch" signal while others activate the "read pin" signal. Latch instructions are referred to as Read-Modify-Write instructions. Each I/O line may be independently programmed as input or output.

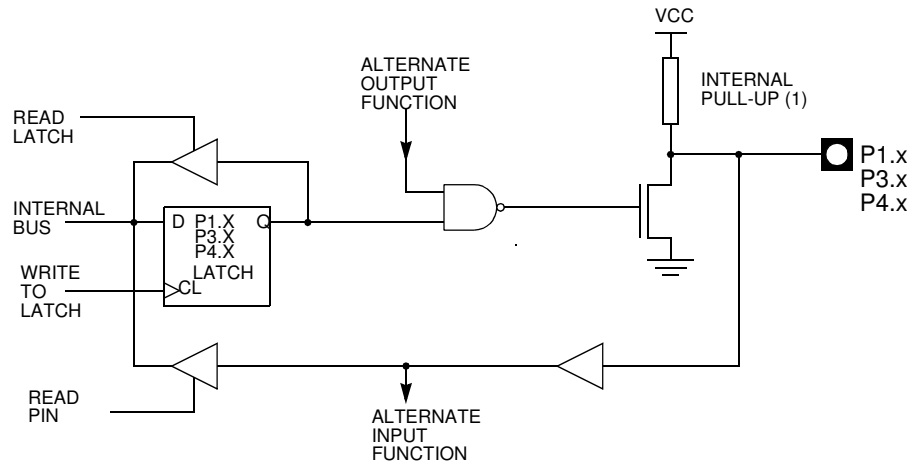
### Port 1, Port 3 and Port 4

Figure 1 shows the structure of Ports 1 and 3, which have internal pull-ups. An external source can pull the pin low. Each Port pin can be configured either for general-purpose I/O or for its alternate input output function.

To use a pin for general-purpose output, set or clear the corresponding bit in the Px register (x = 1,3 or 4). To use a pin for general-purpose input, set the bit in the Px register. This turns off the output FET drive.

To configure a pin for its alternate function, set the bit in the Px register. When the latch is set, the "alternate output function" signal controls the output level (see Figure 1). The operation of Ports 1, 3 and 4 is discussed further in the "quasi-Bidirectional Port Operation" section.

**Figure 1.** Port 1, Port 3 and Port 4 Structure



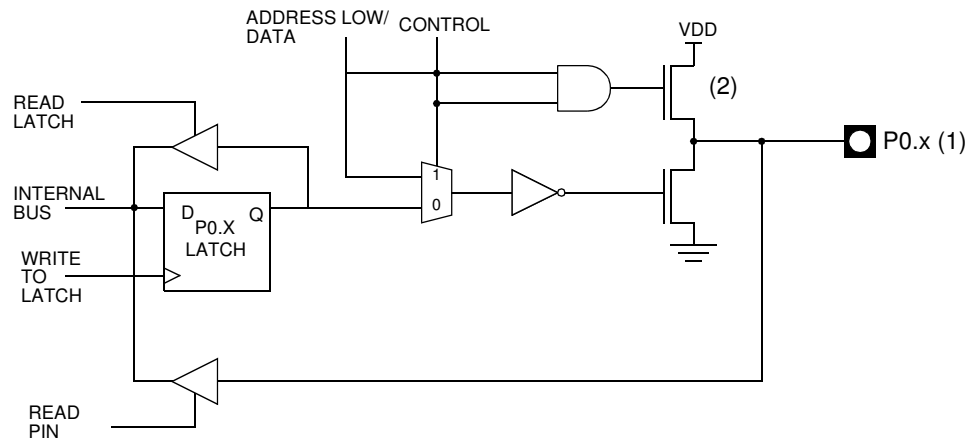
Note: The internal pull-up can be disabled on P1 when analog function is selected.

### Port 0 and Port 2

Ports 0 and 2 are used for general-purpose I/O or as the external address/data bus. Port 0, shown in Figure 3, differs from the other Ports in not having internal pull-ups. Figure 3 shows the structure of Port 2. An external source can pull a Port 2 pin low.

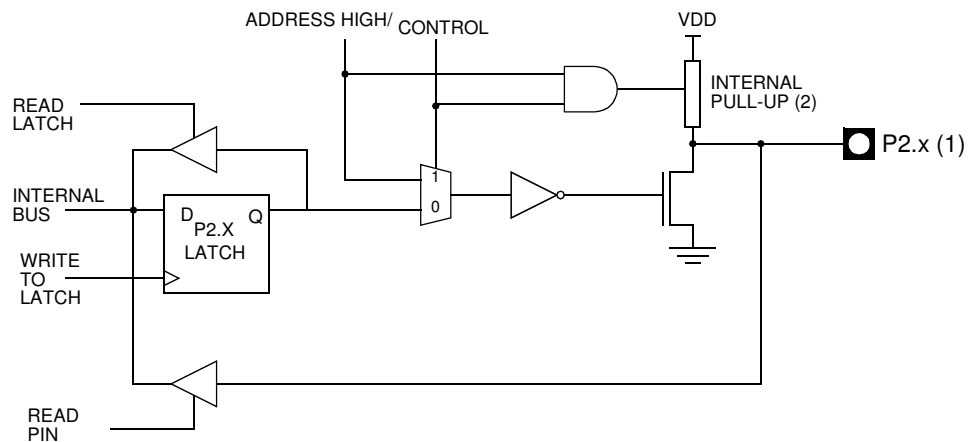
To use a pin for general-purpose output, set or clear the corresponding bit in the Px register (x = 0 or 2). To use a pin for general-purpose input, set the bit in the Px register to turn off the output driver FET.

**Figure 2. Port 0 Structure**



- Notes:
1. Port 0 is precluded from use as general-purpose I/O Ports when used as address/data bus drivers.
  2. Port 0 internal strong pull-ups assist the logic-one output for memory bus cycles only. Except for these bus cycles, the pull-up FET is off, Port 0 outputs are open-drain.

**Figure 3. Port 2 Structure**



- Notes:
1. Port 2 is precluded from use as general-purpose I/O Ports when as address/data bus drivers.
  2. Port 2 internal strong pull-ups FET (P1 in FIGURE) assist the logic-one output for memory bus cycle.

When Port 0 and Port 2 are used for an external memory cycle, an internal control signal switches the output-driver input from the latch output to the internal address/data line.

## Read-Modify-Write Instructions

Some instructions read the latch data rather than the pin data. The latch based instructions read the data, modify the data and then rewrite the latch. These are called "Read-Modify-Write" instructions. Below is a complete list of these special instructions (see Table ). When the destination operand is a Port or a Port bit, these instructions read the latch rather than the pin:

**Table 1.** Read-Modify-Write Instructions

Instruction	Description	Example
ANL	logical AND	ANL P1, A
ORL	logical OR	ORL P2, A
XRL	logical EX-OR	XRL P3, A
JBC	jump if bit = 1 and clear bit	JBC P1.1, LABEL
CPL	complement bit	CPL P3.0
INC	increment	INC P2
DEC	decrement	DEC P2
DJNZ	decrement and jump if not zero	DJNZ P3, LABEL
MOV Px.y, C	move carry bit to bit y of Port x	MOV P1.5, C
CLR Px.y	clear bit y of Port x	CLR P2.4
SET Px.y	set bit y of Port x	SET P3.3

It is not obvious the last three instructions in this list are Read-Modify-Write instructions. These instructions read the port (all 8 bits), modify the specifically addressed bit and write the new byte back to the latch. These Read-Modify-Write instructions are directed to the latch rather than the pin in order to avoid possible misinterpretation of voltage (and therefore, logic) levels at the pin. For example, a Port bit used to drive the base of an external bipolar transistor can not rise above the transistor's base-emitter junction voltage (a value lower than VIL). With a logic one written to the bit, attempts by the CPU to read the Port at the pin are misinterpreted as logic zero. A read of the latch rather than the pins returns the correct logic-one value.

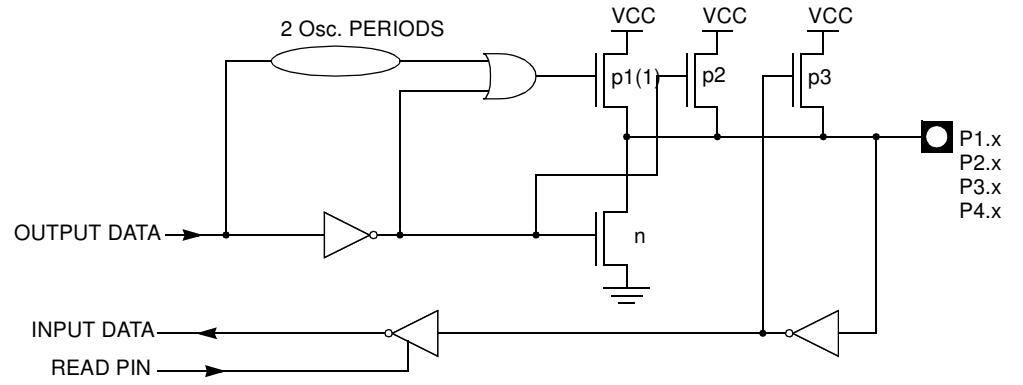
## Quasi-Bidirectional Port Operation

Port 1, Port 2, Port 3 and Port 4 have fixed internal pull-ups and are referred to as "quasi-bidirectional" Ports. When configured as an input, the pin impedance appears as logic one and sources current in response to an external logic zero condition. Port 0 is a "true bidirectional" pin. The pins float when configured as input. Resets write logic one to all Port latches. If logical zero is subsequently written to a Port latch, it can be returned to input conditions by a logical one written to the latch.

Note: Port latch values change near the end of Read-Modify-Write instruction cycles. Output buffers (and therefore the pin state) update early in the instruction after Read-Modify-Write instruction cycle.

Logical zero-to-one transitions in Port 1, Port 2, Port 3 and Port 4 use an additional pull-up (p1) to aid this logic transition (see Figure 4.). This increases switch speed. This extra pull-up sources 100 times normal internal circuit current during 2 oscillator clock periods. The internal pull-ups are field-effect transistors rather than linear resistors. Pull-ups consist of three p-channel FET (pFET) devices. A pFET is on when the gate senses logical zero and off when the gate senses logical one. pFET #1 is turned on for two oscillator periods immediately after a zero-to-one transition in the Port latch. A logical one at the Port pin turns on pFET #3 (a weak pull-up) through the inverter. This inverter and pFET pair form a latch to drive logical one. pFET #2 is a very weak pull-up switched on whenever the associated nFET is switched off. This is traditional CMOS switch convention. Current strengths are 1/10 that of pFET #3.

**Figure 4.** Internal Pull-Up Configurations



Note: Port 2 p1 assists the logic-one output for memory bus cycles.



## SFR Mapping

The Special Function Registers (SFRs) of the T89C51CC01 fall into the following categories:

**Table 2. C51 Core SFRs**

Mnemonic	Add	Name	7	6	5	4	3	2	1	0
ACC	E0h	Accumulator	–	–	–	–	–	–	–	–
B	F0h	B Register	–	–	–	–	–	–	–	–
PSW	D0h	Program Status Word	CY	AC	F0	RS1	RS0	OV	F1	P
SP	81h	Stack Pointer	–	–	–	–	–	–	–	–
DPL	82h	Data Pointer Low byte LSB of DPTR	–	–	–	–	–	–	–	–
DPH	83h	Data Pointer High byte MSB of DPTR	–	–	–	–	–	–	–	–

**Table 3. I/O Port SFRs**

Mnemonic	Add	Name	7	6	5	4	3	2	1	0
P0	80h	Port 0	–	–	–	–	–	–	–	–
P1	90h	Port 1	–	–	–	–	–	–	–	–
P2	A0h	Port 2	–	–	–	–	–	–	–	–
P3	B0h	Port 3	–	–	–	–	–	–	–	–
P4	C0h	Port 4 (x2)	–	–	–	–	–	–	–	–

**Table 4. Timers SFRs**

Mnemonic	Add	Name	7	6	5	4	3	2	1	0
TH0	8Ch	Timer/Counter 0 High byte	–	–	–	–	–	–	–	–
TL0	8Ah	Timer/Counter 0 Low byte	–	–	–	–	–	–	–	–
TH1	8Dh	Timer/Counter 1 High byte	–	–	–	–	–	–	–	–
TL1	8Bh	Timer/Counter 1 Low byte	–	–	–	–	–	–	–	–
TH2	CDh	Timer/Counter 2 High byte	–	–	–	–	–	–	–	–
TL2	CCh	Timer/Counter 2 Low byte	–	–	–	–	–	–	–	–
TCON	88h	Timer/Counter 0 and 1 control	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0
TMOD	89h	Timer/Counter 0 and 1 Modes	GATE1	C/T1#	M11	M01	GATE0	C/T0#	M10	M00

**Table 4. Timers SFRs (Continued)**

Mnemonic	Add	Name	7	6	5	4	3	2	1	0
T2CON	C8h	Timer/Counter 2 control	TF2	EXF2	RCLK	TCLK	EXEN2	TR2	C/T2#	CP/RL2#
T2MOD	C9h	Timer/Counter 2 Mode	-	-	-	-	-	-	T2OE	DCEN
RCAP2H	CBh	Timer/Counter 2 Reload/Capture High byte	-	-	-	-	-	-	-	-
RCAP2L	CAh	Timer/Counter 2 Reload/Capture Low byte	-	-	-	-	-	-	-	-
WDTRST	A6h	Watchdog Timer Reset	-	-	-	-	-	-	-	-
WDTPRG	A7h	Watchdog Timer Program	-	-	-	-	-	S2	S1	S0

**Table 5. Serial I/O Port SFRs**

Mnemonic	Add	Name	7	6	5	4	3	2	1	0
SCON	98h	Serial Control	FE/SM0	SM1	SM2	REN	TB8	RB8	TI	RI
SBUF	99h	Serial Data Buffer	-	-	-	-	-	-	-	-
SADEN	B9h	Slave Address Mask	-	-	-	-	-	-	-	-
SADDR	A9h	Slave Address	-	-	-	-	-	-	-	-

**Table 6. PCA SFRs**

Mnemonic	Add	Name	7	6	5	4	3	2	1	0
CCON	D8h	PCA Timer/Counter Control	CF	CR	-	CCF4	CCF3	CCF2	CCF1	CCF0
CMOD	D9h	PCA Timer/Counter Mode	CIDL	WDTE	-	-	-	CPS1	CPS0	ECF
CL	E9h	PCA Timer/Counter Low byte	-	-	-	-	-	-	-	-
CH	F9h	PCA Timer/Counter High byte	-	-	-	-	-	-	-	-
CCAPM0	DAh	PCA Timer/Counter Mode 0	-	ECOM0	CAPP0	CAPN0	MAT0	TOG0	PWM0	ECCF0
CCAPM1	DBh	PCA Timer/Counter Mode 1	-	ECOM1	CAPP1	CAPN1	MAT1	TOG1	PWM1	ECCF1
CCAPM2	DCh	PCA Timer/Counter Mode 2	-	ECOM2	CAPP2	CAPN2	MAT2	TOG2	PWM2	ECCF2
CCAPM3	DDh	PCA Timer/Counter Mode 3	-	ECOM3	CAPP3	CAPN3	MAT3	TOG3	PWM3	ECCF3
CCAPM4	DEh	PCA Timer/Counter Mode 4	-	ECOM4	CAPP4	CAPN4	MAT4	TOG4	PWM4	ECCF4
CCAP0H	FAh	PCA Compare Capture Module 0 H	CCAP0H7	CCAP0H6	CCAP0H5	CCAP0H4	CCAP0H3	CCAP0H2	CCAP0H1	CCAP0H0
CCAP1H	FBh	PCA Compare Capture Module 1 H	CCAP1H7	CCAP1H6	CCAP1H5	CCAP1H4	CCAP1H3	CCAP1H2	CCAP1H1	CCAP1H0
CCAP2H	FCh	PCA Compare Capture Module 2 H	CCAP2H7	CCAP2H6	CCAP2H5	CCAP2H4	CCAP2H3	CCAP2H2	CCAP2H1	CCAP2H0
CCAP3H	FDh	PCA Compare Capture Module 3 H	CCAP3H7	CCAP3H6	CCAP3H5	CCAP3H4	CCAP3H3	CCAP3H2	CCAP3H1	CCAP3H0
CCAP4H	FEh	PCA Compare Capture Module 4 H	CCAP4H7	CCAP4H6	CCAP4H5	CCAP4H4	CCAP4H3	CCAP4H2	CCAP4H1	CCAP4H0

**Table 6. PCA SFRs (Continued)**

Mnemonic	Add	Name	7	6	5	4	3	2	1	0
CCAP0L	EAh	PCA Compare Capture Module 0 L	CCAP0L7	CCAP0L6	CCAP0L5	CCAP0L4	CCAP0L3	CCAP0L2	CCAP0L1	CCAP0L0
CCAP1L	EBh	PCA Compare Capture Module 1 L	CCAP1L7	CCAP1L6	CCAP1L5	CCAP1L4	CCAP1L3	CCAP1L2	CCAP1L1	CCAP1L0
CCAP2L	ECh	PCA Compare Capture Module 2 L	CCAP2L7	CCAP2L6	CCAP2L5	CCAP2L4	CCAP2L3	CCAP2L2	CCAP2L1	CCAP2L0
CCAP3L	EDh	PCA Compare Capture Module 3 L	CCAP3L7	CCAP3L6	CCAP3L5	CCAP3L4	CCAP3L3	CCAP3L2	CCAP3L1	CCAP3L0
CCAP4L	EEh	PCA Compare Capture Module 4 L	CCAP4L7	CCAP4L6	CCAP4L5	CCAP4L4	CCAP4L3	CCAP4L2	CCAP4L1	CCAP4L0

**Table 7. Interrupt SFRs**

Mnemonic	Add	Name	7	6	5	4	3	2	1	0
IEN0	A8h	Interrupt Enable Control 0	EA	EC	ET2	ES	ET1	EX1	ET0	EX0
IEN1	E8h	Interrupt Enable Control 1	–	–	–	–	–	ETIM	EADC	ECAN
IPL0	B8h	Interrupt Priority Control Low 0	–	PPC	PT2	PS	PT1	PX1	PT0	PX0
IPH0	B7h	Interrupt Priority Control High 0	–	PPCH	PT2H	PSH	PT1H	PX1H	PT0H	PX0H
IPL1	F8h	Interrupt Priority Control Low 1	–	–	–	–	–	POVRL	PADCL	PCANL
IPH1	F7h	Interrupt Priority Control High 1	–	–	–	–	–	POVRH	PADCH	PCANH

**Table 8. ADC SFRs**

Mnemonic	Add	Name	7	6	5	4	3	2	1	0
ADCON	F3h	ADC Control	–	PSIDLE	ADEN	ADEOC	ADSST	SCH2	SCH1	SCH0
ADCF	F6h	ADC Configuration	CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0
ADCLK	F2h	ADC Clock	–	–	–	PRS4	PRS3	PRS2	PRS1	PRS0
ADDH	F5h	ADC Data High byte	ADAT9	ADAT8	ADAT7	ADAT6	ADAT5	ADAT4	ADAT3	ADAT2
ADDL	F4h	ADC Data Low byte	–	–	–	–	–	–	ADAT1	ADAT0

**Table 9. CAN SFRs**

Mnemonic	Add	Name	7	6	5	4	3	2	1	0
CANGCON	ABh	CAN General Control	ABRQ	OVRQ	TTC	SYNCTTC	AUT-BAUD	TEST	ENA	GRES
CANGSTA	AAh	CAN General Status	–	OVFG	–	TBSY	RBSY	ENFG	BOFF	ERRP
CANGIT	9Bh	CAN General Interrupt	CANIT	–	OVRTIM	OVRBUF	SERG	CERG	FERG	AERG
CANBT1	B4h	CAN Bit Timing 1	–	BRP5	BRP4	BRP3	BRP2	BRP1	BRP0	–
CANBT2	B5h	CAN Bit Timing 2	–	SJW1	SJW0	–	PRS2	PRS1	PRS0	–
CANBT3	B6h	CAN Bit Timing 3	–	PHS22	PHS21	PHS20	PHS12	PHS11	PHS10	SMP

**Table 9. CAN SFRs (Continued)**

Mnemonic	Add	Name	7	6	5	4	3	2	1	0
CANEN1	CEh	CAN Enable Channel byte 1	–	ENCH14	ENCH13	ENCH12	ENCH11	ENCH10	ENCH9	ENCH8
CANEN2	CFh	CAN Enable Channel byte 2	ENCH7	ENCH6	ENCH5	ENCH4	ENCH3	ENCH2	ENCH1	ENCH0
CANGIE	C1h	CAN General Interrupt Enable	–	–	ENRX	ENTX	ENERCH	ENBUF	ENERG	–
CANIE1	C2h	CAN Interrupt Enable Channel byte 1	–	IECH14	IECH13	IECH12	IECH11	IECH10	IECH9	IECH8
CANIE2	C3h	CAN Interrupt Enable Channel byte 2	IECH7	IECH6	IECH5	IECH4	IECH3	IECH2	IECH1	IECH0
CANSIT1	BAh	CAN Status Interrupt Channel byte1	–	SIT14	SIT13	SIT12	SIT11	SIT10	SIT9	SIT8
CANSIT2	BBh	CAN Status Interrupt Channel byte2	SIT7	SIT6	SIT5	SIT4	SIT3	SIT2	SIT1	SIT0
CANTCON	A1h	CAN Timer Control	TPRESC 7	TPRESC 6	TPRESC 5	TPRESC 4	TPRESC 3	TPRESC 2	TPRESC 1	TPRESC 0
CANTIMH	ADh	CAN Timer high	CANTIM 15	CANTIM 14	CANTIM 13	CANTIM 12	CANTIM 11	CANTIM 10	CANTIM 9	CANTIM 8
CANTIML	ACh	CAN Timer low	CANTIM 7	CANTIM 6	CANTIM 5	CANTIM 4	CANTIM 3	CANTIM 2	CANTIM 1	CANTIM 0
CANSTMH	AFh	CAN Timer Stamp high	TIMSTMP 15	TIMSTMP 14	TIMSTMP 13	TIMSTMP 12	TIMSTMP 11	TIMSTMP 10	TIMSTMP 9	TIMSTMP 8
CANSTML	AEh	CAN Timer Stamp low	TIMSTMP 7	TIMSTMP 6	TIMSTMP 5	TIMSTMP 4	TIMSTMP 3	TIMSTMP 2	TIMSTMP 1	TIMSTMP 0
CANTTCH	A5h	CAN Timer TTC high	TIMTTC 15	TIMTTC 14	TIMTTC 13	TIMTTC 12	TIMTTC 11	TIMTTC 10	TIMTTC 9	TIMTTC 8
CANTTCL	A4h	CAN Timer TTC low	TIMTTC 7	TIMTTC 6	TIMTTC 5	TIMTTC 4	TIMTTC 3	TIMTTC 2	TIMTTC 1	TIMTTC 0
CANTEC	9Ch	CAN Transmit Error Counter	TEC7	TEC6	TEC5	TEC4	TEC3	TEC2	TEC1	TEC0
CANREC	9Dh	CAN Receive Error Counter	REC7	REC6	REC5	REC4	REC3	REC2	REC1	REC0
CANPAGE	B1h	CAN Page	CHNB3	CHNB2	CHNB1	CHNB0	AINC	INDX2	INDX1	INDX0
CANSTCH	B2h	CAN Status Channel	DLCW	TXOK	RXOK	BERR	SERR	CERR	FERR	AERR
CANCONH	B3h	CAN Control Channel	CONCH1	CONCH0	RPLV	IDE	DLC3	DLC2	DLC1	DLC0
CANMSG	A3h	CAN Message Data	MSG7	MSG6	MSG5	MSG4	MSG3	MSG2	MSG1	MSG0

**Table 9. CAN SFRs (Continued)**

Mnemonic	Add	Name	7	6	5	4	3	2	1	0
CANIDT1	BCh	CAN Identifier Tag byte 1(Part A)	IDT10	IDT9	IDT8	IDT7	IDT6	IDT5	IDT4	IDT3
		CAN Identifier Tag byte 1(PartB)	IDT28	IDT27	IDT26	IDT25	IDT24	IDT23	IDT22	IDT21
CANIDT2	BDh	CAN Identifier Tag byte 2 (PartA)	IDT2	IDT1	IDT0	–	–	–	–	–
		CAN Identifier Tag byte 2 (PartB)	IDT20	IDT19	IDT18	IDT17	IDT16	IDT15	IDT14	IDT13
CANIDT3	BEh	CAN Identifier Tag byte 3(PartA)	–	–	–	–	–	–	–	–
		CAN Identifier Tag byte 3(PartB)	IDT12	IDT11	IDT10	IDT9	IDT8	IDT7	IDT6	IDT5
CANIDT4	BFh	CAN Identifier Tag byte 4(PartA)	–	–	–	–	–	RTRTAG	–	RB0TAG
		CAN Identifier Tag byte 4(PartB)	IDT4	IDT3	IDT2	IDT1	IDT0	–	RB1TAG	–
CANIDM1	C4h	CAN Identifier Mask byte 1(PartA)	IDMSK10	IDMSK9	IDMSK8	IDMSK7	IDMSK6	IDMSK5	IDMSK4	IDMSK3
		CAN Identifier Mask byte 1(PartB)	IDMSK28	IDMSK27	IDMSK26	IDMSK25	IDMSK24	IDMSK23	IDMSK22	IDMSK21
CANIDM2	C5h	CAN Identifier Mask byte 2(PartA)	IDMSK2	IDMSK1	IDMSK0	–	–	–	–	–
		CAN Identifier Mask byte 2(PartB)	IDMSK20	IDMSK19	IDMSK18	IDMSK17	IDMSK16	IDMSK15	IDMSK14	IDMSK13
CANIDM3	C6h	CAN Identifier Mask byte 3(PartA)	–	–	–	–	–	–	–	–
		CAN Identifier Mask byte 3(PartB)	IDMSK12	IDMSK11	IDMSK10	IDMSK9	IDMSK8	IDMSK7	IDMSK6	IDMSK5
CANIDM4	C7h	CAN Identifier Mask byte 4(PartA)	–	–	–	–	–	RTRMSK	–	IDEMSK
		CAN Identifier Mask byte 4(PartB)	IDMSK4	IDMSK3	IDMSK2	IDMSK1	IDMSK0	–	–	–

**Table 10. Other SFRs**

Mnemonic	Add	Name	7	6	5	4	3	2	1	0
PCON	87h	Power Control	SMOD1	SMOD0	–	POF	GF1	GF0	PD	IDL
AUXR	8Eh	Auxiliary Register 0	–	–	M0	–	XRS1	XRS2	EXTRAM	A0
AUXR1	A2h	Auxiliary Register 1	–	–	ENBOOT	–	GF3	0	–	DPS
CKCON	8Fh	Clock Control	CANX2	WDX2	PCAX2	SIX2	T2X2	T1X2	T0X2	X2

**Table 10. Other SFRs**

Mnemonic	Add	Name	7	6	5	4	3	2	1	0
FCON	D1h	Flash Control	FPL3	FPL2	FPL1	FPL0	FPS	FMOD1	FMOD0	FBUSY
EECON	D2h	EEPROM Contol	EEPL3	EEPL2	EEPL1	EEPL0	–	–	EEE	EEBUSY

**Table 11. SFR Mapping**

	0/8 <sup>(1)</sup>	1/9	2/A	3/B	4/C	5/D	6/E	7/F	
F8h	IPL1 xxxx x000	CH 0000 0000	CCAP0H 0000 0000	CCAP1H 0000 0000	CCAP2H 0000 0000	CCAP3H 0000 0000	CCAP4H 0000 0000		FFh
F0h	B 0000 0000		ADCLK xxx0 0000	ADCON x000 0000	ADDL 0000 0000	ADDH 0000 0000	ADCF 0000 0000	IPH1 xxxx x000	F7h
E8h	IEN1 xxxx x000	CL 0000 0000	CCAP0L 0000 0000	CCAP1L 0000 0000	CCAP2L 0000 0000	CCAP3L 0000 0000	CCAP4L 0000 0000		EFh
E0h	ACC 0000 0000								E7h
D8h	CCON 00x0 0000	CMOD 00xx x000	CCAPM0 x000 0000	CCAPM1 x000 0000	CCAPM2 x000 0000	CCAPM3 x000 0000	CCAPM4 x000 0000		DFh
D0h	PSW 0000 0000	FCON 0000 0000	EECON xxxx xx00						D7h
C8h	T2CON 0000 0000	T2MOD xxxx xx00	RCAP2L 0000 0000	RCAP2H 0000 0000	TL2 0000 0000	TH2 0000 0000	CANEN1 x000 0000	CANEN2 0000 0000	CFh
C0h	P4 xxxx xx11	CANGIE 1100 0000	CANIE1 x000 0000	CANIE2 0000 0000	CANIDM1 xxxx xxxx	CANIDM2 xxxx xxxx	CANIDM3 xxxx xxxx	CANIDM4 xxxx xxxx	C7h
B8h	IPL0 x000 0000	SADEN 0000 0000	CANSIT1 x000 0000	CANSIT2 0000 0000	CANIDT1 xxxx xxxx	CANIDT2 xxxx xxxx	CANIDT3 xxxx xxxx	CANIDT4 xxxx xxxx	BFh
B0h	P3 1111 1111	CANPAGE 0000 0000	CANSTCH xxxx xxxx	CANCONCH xxxx xxxx	CANBT1 xxxx xxxx	CANBT2 xxxx xxxx	CANBT3 xxxx xxxx	IPH0 x000 0000	B7h
A8h	IEN0 0000 0000	SADDR 0000 0000	CANGSTA 1010 0000	CANGCON 0000 0000	CANTIML 0000 0000	CANTIMH 0000 0000	CANSTMPL xxxx xxxx	CANSTMPH xxxx xxxx	AFh
A0h	P2 1111 1111	CANTCON 0000 0000	AUXR1 xxxx 00x0	CANMSG xxxx xxxx	CANTTCL 0000 0000	CANTTCH 0000 0000	WDTRST 1111 1111	WDTPRG xxxx x000	A7h
98h	SCON 0000 0000	SBUF 0000 0000		CANGIT 0x00 0000	CANTEC 0000 0000	CANREC 0000 0000			9Fh
90h	P1 1111 1111								97h
88h	TCON 0000 0000	TMOD 0000 0000	TL0 0000 0000	TL1 0000 0000	TH0 0000 0000	TH1 0000 0000	AUXR x00x 1100	CKCON 0000 0000	8Fh
80h	P0 1111 1111	SP 0000 0111	DPL 0000 0000	DPH 0000 0000				PCON 00x1 0000	87h
	0/8 <sup>(1)</sup>	1/9	2/A	3/B	4/C	5/D	6/E	7/F	

 Reserved 

Note: 1. These registers are bit-addressable.  
 Sixteen addresses in the SFR space are both byte-addressable and bit-addressable. The bit-addressable SFR's are those whose address ends in 0 and 8. The bit addresses, in this area, are 0x80 through to 0xFF.



## Clock

The T89C51CC01 core needs only 6 clock periods per machine cycle. This feature, called "X2", provides the following advantages:

- Divides frequency crystals by 2 (cheaper crystals) while keeping the same CPU power.
- Saves power consumption while keeping the same CPU power (oscillator power saving).
- Saves power consumption by dividing dynamic operating frequency by 2 in operating and idle modes.
- Increases CPU power by 2 while keeping the same crystal frequency.

In order to keep the original C51 compatibility, a divider-by-2 is inserted between the XTAL1 signal and the main clock input of the core (phase generator). This divider may be disabled by the software.

An extra feature is available to start after Reset in the X2 mode. This feature can be enabled by a bit X2B in the Hardware Security Byte. This bit is described in the section "In-System-Programming".

## Description

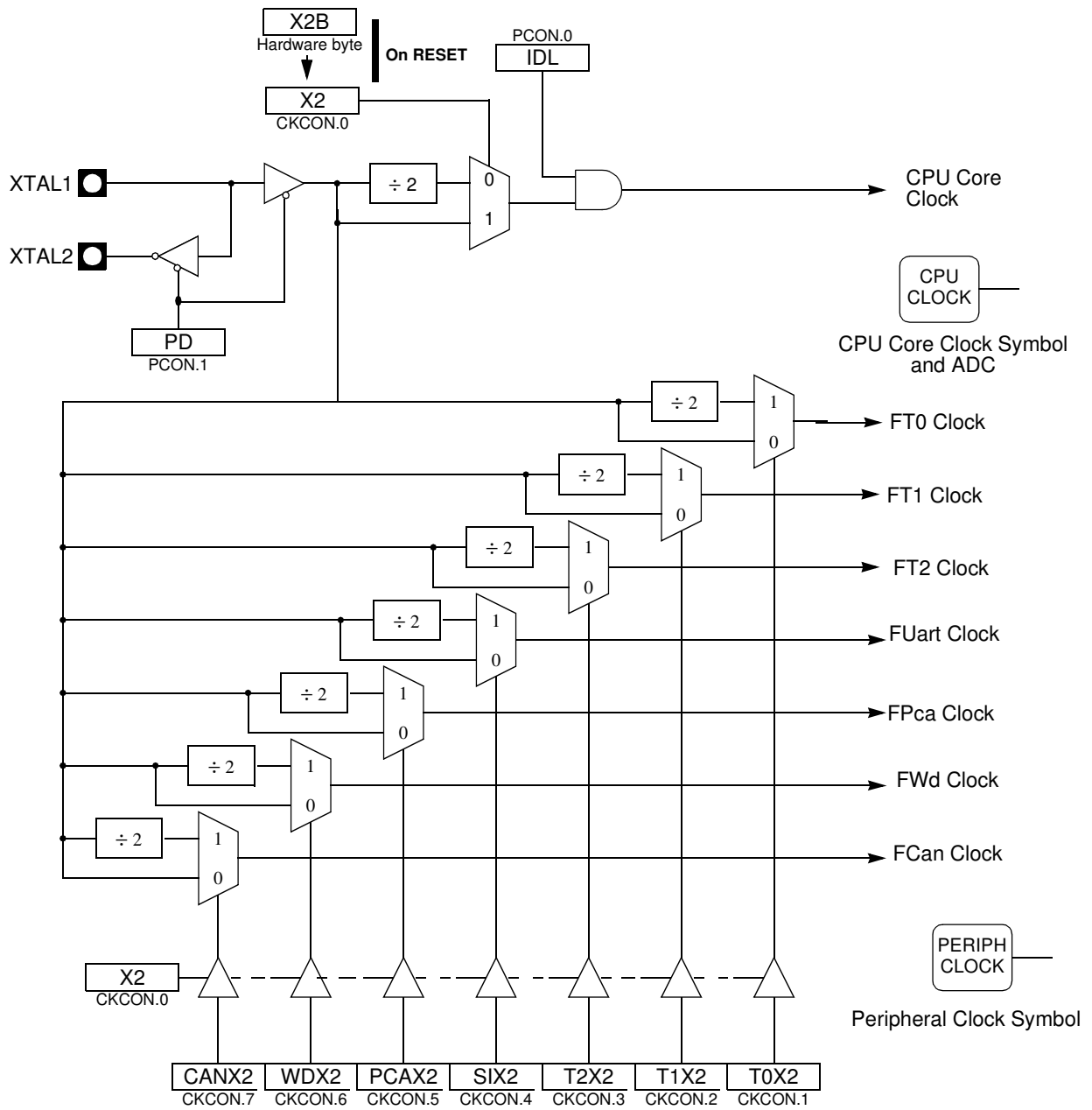
The X2 bit in the CKCON register (see Table 12) allows switching from 12 clock cycles per instruction to 6 clock cycles and vice versa. At reset, the standard speed is activated (STD mode).

Setting this bit activates the X2 feature (X2 mode) for the CPU Clock only (see Figure 5.).

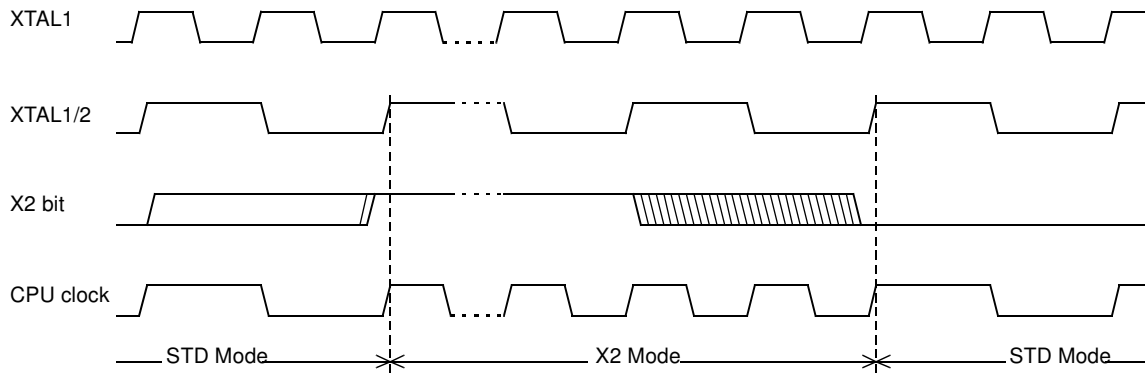
The Timers 0, 1 and 2, Uart, PCA, Watchdog or CAN switch in X2 mode only if the corresponding bit is cleared in the CKCON register.

The clock for the whole circuit and peripheral is first divided by two before being used by the CPU core and peripherals. This allows any cyclic ratio to be accepted on the XTAL1 input. In X2 mode, as this divider is bypassed, the signals on XTAL1 must have a cyclic ratio between 40 to 60%. Figure 5. shows the clock generation block diagram. The X2 bit is validated on the XTAL1÷2 rising edge to avoid glitches when switching from the X2 to the STD mode. Figure 6 shows the mode switching waveforms.

Figure 5. Clock CPU Generation Diagram



**Figure 6. Mode Switching Waveforms**



**Note:** In order to prevent any incorrect operation while operating in the X2 mode, users must be aware that all peripherals using the clock frequency as a time reference (UART, timers...) will have their time reference divided by two. For example a free running timer generating an interrupt every 20 ms will then generate an interrupt every 10 ms. A UART with a 4800 baud rate will have a 9600 baud rate.

## Register

Table 12. CKCON Register

CKCON (S:8Fh)  
Clock Control Register

7	6	5	4	3	2	1	0
CANX2	WDX2	PCAX2	SIX2	T2X2	T1X2	T0X2	X2
Bit Number	Bit Mnemonic	Description					
7	CANX2	<b>CAN clock</b> <sup>(1)</sup> Clear to select 6 clock periods per peripheral clock cycle. Set to select 12 clock periods per peripheral clock cycle.					
6	WDX2	<b>Watchdog clock</b> <sup>(1)</sup> Clear to select 6 clock periods per peripheral clock cycle. Set to select 12 clock periods per peripheral clock cycle.					
5	PCAX2	<b>Programmable Counter Array clock</b> <sup>(1)</sup> Clear to select 6 clock periods per peripheral clock cycle. Set to select 12 clock periods per peripheral clock cycle.					
4	SIX2	<b>Enhanced UART clock (MODE 0 and 2)</b> <sup>(1)</sup> Clear to select 6 clock periods per peripheral clock cycle. Set to select 12 clock periods per peripheral clock cycle.					
3	T2X2	<b>Timer 2 clock</b> <sup>(1)</sup> Clear to select 6 clock periods per peripheral clock cycle. Set to select 12 clock periods per peripheral clock cycle.					
2	T1X2	<b>Timer 1 clock</b> <sup>(1)</sup> Clear to select 6 clock periods per peripheral clock cycle. Set to select 12 clock periods per peripheral clock cycle.					
1	T0X2	<b>Timer 0 clock</b> <sup>(1)</sup> Clear to select 6 clock periods per peripheral clock cycle. Set to select 12 clock periods per peripheral clock cycle.					
0	X2	<b>CPU clock</b> Clear to select 12 clock periods per machine cycle (STD mode) for CPU and all the peripherals. Set to select 6 clock periods per machine cycle (X2 mode) and to enable the individual peripherals "X2"bits.					

Note: 1. This control bit is validated when the CPU clock bit X2 is set; when X2 is low, this bit has no effect.

Reset Value = 0000 0000b

## Power Management

Two power reduction modes are implemented in the T89C51CC01: the Idle mode and the Power-down mode. These modes are detailed in the following sections. In addition to these power reduction modes, the clocks of the core and peripherals can be dynamically divided by 2 using the X2 Mode detailed in Section “Clock”.

## Reset Pin

In order to start-up (cold reset) or to restart (warm reset) properly the microcontroller, a high level has to be applied on the RST pin. A bad level leads to a wrong initialisation of the internal registers like SFRs, PC, etc. and to unpredictable behavior of the microcontroller. A warm reset can be applied either directly on the RST pin or indirectly by an internal reset source such as a watchdog, PCA, timer, etc.

## At Power-up (Cold Reset)

Two conditions are required before enabling a CPU start-up:

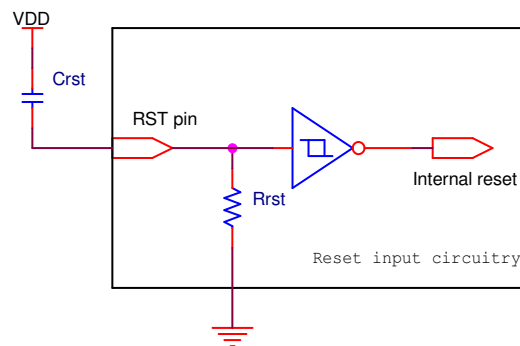
- VDD must reach the specified VDD range,
- The level on xtal1 input must be outside the specification (VIH, VIL).

If one of these two conditions are not met, the microcontroller does not start correctly and can execute an instruction fetch from anywhere in the program space. An active level applied on the RST pin must be maintained until both of the above conditions are met. A reset is active when the level VIH1 is reached and when the pulse width covers the period of time where VDD and the oscillator are not stabilized. Two parameters have to be taken into account to determine the reset pulse width:

- VDD rise time (vddrst),
- Oscillator startup time (oscrst).

To determine the capacitor the highest value of these two parameters has to be chosen. The reset circuitry is shown in Figure 7.

**Figure 7.** Reset Circuitry



0

Table 13 and Table 15 give some typical examples for three values of VDD rise times, two values of oscillator start-up time and two pull-down resistor values.

**Table 13.** Minimum Reset Capacitor for a 15k Pull-down Resistor

oscrst/vddrst	1ms	10ms	100ms
5ms	2.7 $\mu$ F	4.7 $\mu$ F	47 $\mu$ F
20ms	10 $\mu$ F	15 $\mu$ F	47 $\mu$ F

Note: These values assume VDD starts from 0v to the nominal value. If the time between two on/off sequences is too fast, the power-supply decoupling capacitors may not be fully discharged, leading to a bad reset sequence.

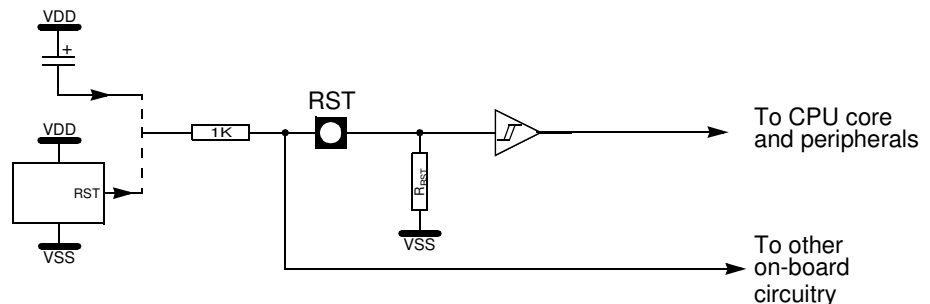
**Warm Reset**

To achieve a valid reset, the reset signal must be maintained for at least 2 machine cycles (24 oscillator clock periods) while the oscillator is running. The number of clock periods is mode independent (X2 or X1).

**Watchdog Reset**

As detailed in Section “PCA Watchdog Timer”, page 123, the WDT generates a 96-clock period pulse on the RST pin. In order to properly propagate this pulse to the rest of the application in case of external capacitor or power-supply supervisor circuit, a 1K $\Omega$  resistor must be added as shown Figure 8.

**Figure 8.** Reset Circuitry for WDT reset out usage



### Reset Recommendation to Prevent Flash Corruption

An example of bad initialization situation may occur in an instance where the bit ENBOOT in AUXR1 register is initialized from the hardware bit BLJB upon reset. Since this bit allows mapping of the bootloader in the code area, a reset failure can be critical.

If one wants the ENBOOT cleared in order to unmap the boot from the code area (yet due to a bad reset) the bit ENBOOT in SFRs may be set. If the value of Program Counter is accidentally in the range of the boot memory addresses then a flash access (write or erase) may corrupt the Flash on-chip memory.

It is recommended to use an external reset circuitry featuring power supply monitoring to prevent system malfunction during periods of insufficient power supply voltage (power supply failure, power supply switched off).

**Idle Mode**

Idle mode is a power reduction mode that reduces the power consumption. In this mode, program execution halts. Idle mode freezes the clock to the CPU at known states while the peripherals continue to be clocked. The CPU status before entering Idle mode is preserved, i.e., the program counter and program status word register retain their data for the duration of Idle mode. The contents of the SFRs and RAM are also retained. The status of the Port pins during Idle mode is detailed in Table 14.

**Entering Idle Mode**

To enter Idle mode, you must set the IDL bit in PCON register (see Table 15). The T89C51CC01 enters Idle mode upon execution of the instruction that sets IDL bit. The instruction that sets IDL bit is the last instruction executed.

Note: If IDL bit and PD bit are set simultaneously, the T89C51CC01 enters Power-down mode. Then it does not go in Idle mode when exiting Power-down mode.

**Exiting Idle Mode**

There are two ways to exit Idle mode:

1. Generate an enabled interrupt.
  - Hardware clears IDL bit in PCON register which restores the clock to the CPU. Execution resumes with the interrupt service routine. Upon completion



of the interrupt service routine, program execution resumes with the instruction immediately following the instruction that activated Idle mode. The general-purpose flags (GF1 and GF0 in PCON register) may be used to indicate whether an interrupt occurred during normal operation or during Idle mode. When Idle mode is exited by an interrupt, the interrupt service routine may examine GF1 and GF0.

2. Generate a reset.

- A logic high on the RST pin clears IDL bit in PCON register directly and asynchronously. This restores the clock to the CPU. Program execution momentarily resumes with the instruction immediately following the instruction that activated the Idle mode and may continue for a number of clock cycles before the internal reset algorithm takes control. Reset initializes the T89C51CC01 and vectors the CPU to address C:0000h.

- Note:
1. During the time that execution resumes, the internal RAM cannot be accessed; however, it is possible for the Port pins to be accessed. To avoid unexpected outputs at the Port pins, the instruction immediately following the instruction that activated Idle mode should not write to a Port pin or to the external RAM.
  2. If Idle mode is invoked by ADC Idle, the ADC conversion completion will exit Idle.

## Power-down Mode

The Power-down mode places the T89C51CC01 in a very low power state. Power-down mode stops the oscillator and freezes all clocks at known states. The CPU status prior to entering Power-down mode is preserved, i.e., the program counter, program status word register retain their data for the duration of Power-down mode. In addition, the SFRs and RAM contents are preserved. The status of the Port pins during Power-down mode is detailed in Table 14.

## Entering Power-down Mode

To enter Power-down mode, set PD bit in PCON register. The T89C51CC01 enters the Power-down mode upon execution of the instruction that sets PD bit. The instruction that sets PD bit is the last instruction executed.

## Exiting Power-down Mode

If VDD was reduced during the Power-down mode, do not exit Power-down mode until VDD is restored to the normal operating level.

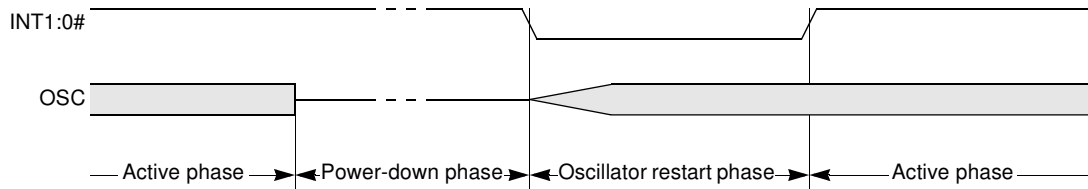
There are two ways to exit the Power-down mode:

1. Generate an enabled external interrupt.
  - The T89C51CC01 provides capability to exit from Power-down using INT0#, INT1#.

Hardware clears PD bit in PCON register which starts the oscillator and restores the clocks to the CPU and peripherals. Using INTx# input, execution resumes when the input is released (see Figure 9) while using KINx input, execution resumes after counting 1024 clock ensuring the oscillator is restarted properly (see Figure 8). Execution resumes with the interrupt service routine. Upon completion of the interrupt service routine, program execution resumes with the instruction immediately following the instruction that activated Power-down mode.

- Note:
1. The external interrupt used to exit Power-down mode must be configured as level sensitive (INT0# and INT1#) and must be assigned the highest priority. In addition, the duration of the interrupt must be long enough to allow the oscillator to stabilize. The execution will only resume when the interrupt is deasserted.
  2. Exit from power-down by external interrupt does not affect the SFRs nor the internal RAM content.

Figure 9. Power-down Exit Waveform Using INT1:0#



2. Generate a reset.

- A logic high on the RST pin clears PD bit in PCON register directly and asynchronously. This starts the oscillator and restores the clock to the CPU and peripherals. Program execution momentarily resumes with the instruction immediately following the instruction that activated Power-down mode and may continue for a number of clock cycles before the internal reset algorithm takes control. Reset initializes the T89C51CC01 and vectors the CPU to address 0000h.

- Notes:
1. During the time that execution resumes, the internal RAM cannot be accessed; however, it is possible for the Port pins to be accessed. To avoid unexpected outputs at the Port pins, the instruction immediately following the instruction that activated the Power-down mode should not write to a Port pin or to the external RAM.
  2. Exit from power-down by reset redefines all the SFRs, but does not affect the internal RAM content.

Table 14. Pin Conditions in Special Operating Modes

Mode	Port 0	Port 1	Port 2	Port 3	Port 4	ALE	PSEN#
Reset	Floating	High	High	High	High	High	High
Idle (internal code)	Data	Data	Data	Data	Data	High	High
Idle (external code)	Floating	Data	Data	Data	Data	High	High
Power-Down(internal code)	Data	Data	Data	Data	Data	Low	Low
Power-Down (external code)	Floating	Data	Data	Data	Data	Low	Low

3.

## Registers

**Table 15.** PCON Register

PCON (S:87h) – Power configuration Register

7	6	5	4	3	2	1	0
SMOD1	SMOD0	-	POF	GF1	GF0	PD	IDL
Bit Number	Bit Mnemonic	Description					
7	SMOD1	<b>Serial port Mode bit 1</b> Set to select double baud rate in mode 1, 2 or 3					
6	SMOD0	<b>Serial port Mode bit 0</b> Clear to select SM0 bit in SCON register. Set to select FE bit in SCON register.					
5	-	<b>Reserved</b> The value read from this bit is indeterminate. Do not set this bit.					
4	POF	<b>Power-Off Flag</b> Clear to recognize next reset type. Set by hardware when $V_{cc}$ rises from 0 to its nominal voltage. Can also be set by software.					
3	GF1	<b>General-purpose flag 1</b> One use is to indicate whether an interrupt occurred during normal operation or during Idle mode.					
2	GF0	<b>General-purpose flag 0</b> One use is to indicate whether an interrupt occurred during normal operation or during Idle mode.					
1	PD	<b>Power-down Mode bit</b> Cleared by hardware when an interrupt or reset occurs. Set to activate the Power-down mode. If IDL and PD are both set, PD takes precedence.					
0	IDL	<b>Idle Mode bit</b> Cleared by hardware when an interrupt or reset occurs. Set to activate the Idle mode. If IDL and PD are both set, PD takes precedence.					

Reset Value = 00X1 0000b

## Data Memory

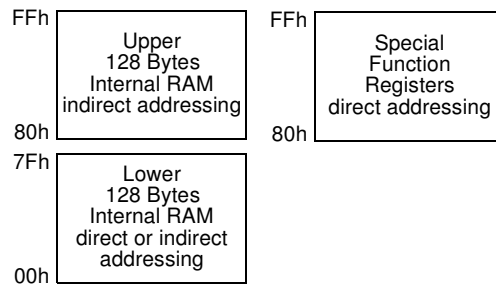
The T89C51CC01 provides data memory access in two different spaces:

1. The internal space mapped in three separate segments:
  - the lower 128 Bytes RAM segment.
  - the upper 128 Bytes RAM segment.
  - the expanded 1024 Bytes RAM segment (XRAM).
2. The external space.

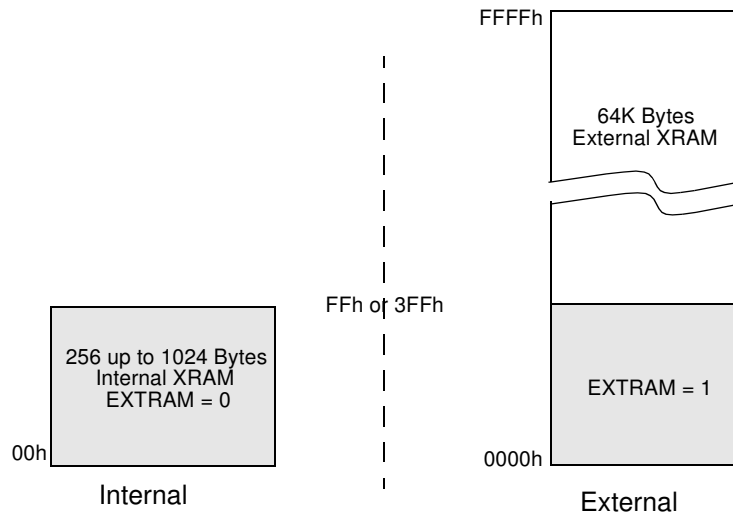
A fourth internal segment is available but dedicated to Special Function Registers, SFRs, (addresses 80h to FFh) accessible by direct addressing mode.

Figure 11 shows the internal and external data memory spaces organization.

**Figure 10.** Internal Memory - RAM



**Figure 11.** Internal and External Data Memory Organization XRAM-XRAM



## Internal Space

### Lower 128 Bytes RAM

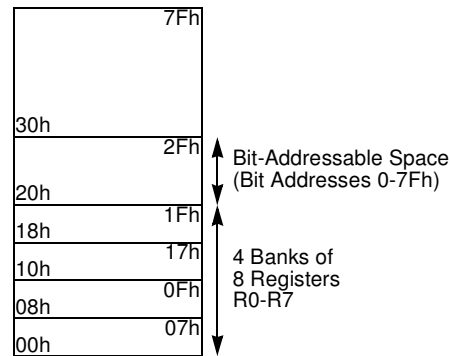
The lower 128 Bytes of RAM (see Figure 11) are accessible from address 00h to 7Fh using direct or indirect addressing modes. The lowest 32 Bytes are grouped into 4 banks of 8 registers (R0 to R7). Two bits RS0 and RS1 in PSW register (see Figure 18) select which bank is in use according to Table 16. This allows more efficient use of code space, since register instructions are shorter than instructions that use direct addressing, and can be used for context switching in interrupt service routines.

**Table 16.** Register Bank Selection

RS1	RS0	Description
0	0	Register bank 0 from 00h to 07h
0	1	Register bank 0 from 08h to 0Fh
1	0	Register bank 0 from 10h to 17h
1	1	Register bank 0 from 18h to 1Fh

The next 16 Bytes above the register banks form a block of bit-addressable memory space. The C51 instruction set includes a wide selection of single-bit instructions, and the 128 bits in this area can be directly addressed by these instructions. The bit addresses in this area are 00h to 7Fh.

**Figure 12.** Lower 128 Bytes Internal RAM Organization



### Upper 128 Bytes RAM

The upper 128 Bytes of RAM are accessible from address 80h to FFh using only indirect addressing mode.

### Expanded RAM

The on-chip 1024 Bytes of expanded RAM (XRAM) are accessible from address 0000h to 03FFh using indirect addressing mode through MOVX instructions. In this address range, the bit EXTRAM in AUXR register is used to select the XRAM (default) or the XRAM. As shown in Figure 11 when EXTRAM = 0, the XRAM is selected and when EXTRAM = 1, the XRAM is selected.

The size of XRAM can be configured by XRS1-0 bit in AUXR register (default size is 1024 Bytes).

Note: Lower 128 Bytes RAM, Upper 128 Bytes RAM, and expanded RAM are made of volatile memory cells. This means that the RAM content is indeterminate after power-up and must then be initialized properly.

External Space

Memory Interface

The external memory interface comprises the external bus (port 0 and port 2) as well as the bus control signals (RD, WR, and ALE).

Figure 13 shows the structure of the external address bus. P0 carries address A7:0 while P2 carries address A15:8. Data D7:0 is multiplexed with A7:0 on P0. Table 17 describes the external memory interface signals.

Figure 13. External Data Memory Interface Structure

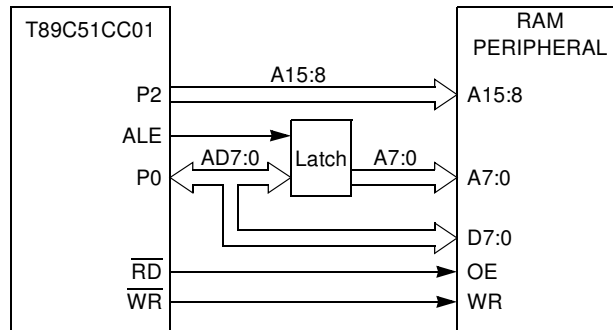


Table 17. External Data Memory Interface Signals

Signal Name	Type	Description	Alternative Function
A15:8	O	<b>Address Lines</b> Upper address lines for the external bus.	P2.7:0
AD7:0	I/O	<b>Address/Data Lines</b> Multiplexed lower address lines and data for the external memory.	P0.7:0
ALE	O	<b>Address Latch Enable</b> ALE signals indicates that valid address information are available on lines AD7:0.	-
$\overline{RD}$	O	<b>Read</b> Read signal output to external data memory.	P3.7
$\overline{WR}$	O	<b>Write</b> Write signal output to external memory.	P3.6

External Bus Cycles

This section describes the bus cycles the T89C51CC01 executes to read (see Figure 14), and write data (see Figure 15) in the external data memory. External memory cycle takes 6 CPU clock periods. This is equivalent to 12 oscillator clock period in standard mode or 6 oscillator clock periods in X2 mode. For further information on X2 mode.

Slow peripherals can be accessed by stretching the read and write cycles. This is done using the M0 bit in AUXR register. Setting this bit changes the width of the  $\overline{RD}$  and  $\overline{WR}$  signals from 3 to 15 CPU clock periods.

For simplicity, the accompanying figures depict the bus cycle waveforms in idealized form and do not provide precise timing information. For bus cycle timing parameters refer to the Section “AC Characteristics”.