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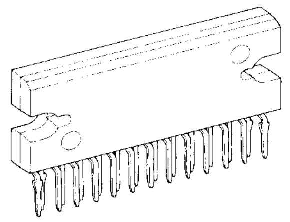
TOSHIBA BiCD Integrated Circuit Silicon Monolithic

TB6560AHQ, TB6560AFG

PWM Chopper-Type Bipolar Driver IC for Stepping Motor Control

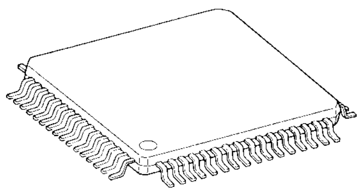
The TB6560AHQ/AFG is a PWM chopper-type stepping motor driver IC designed for sinusoidal-input microstep control of bipolar stepping motors. The TB6560AHQ/AFG can be used in applications that require 2-phase, 1-2-phase, 2W1-2-phase and 4W1-2-phase excitation modes. The TB6560AHQ/AFG is capable of low-vibration, high-performance forward and reverse driving of a two-phase bipolar stepping motor using only a clock signal.

TB6560AHQ



HZIP25-P-1.27

TB6560AFG



HQFP64-P-1010-0.50

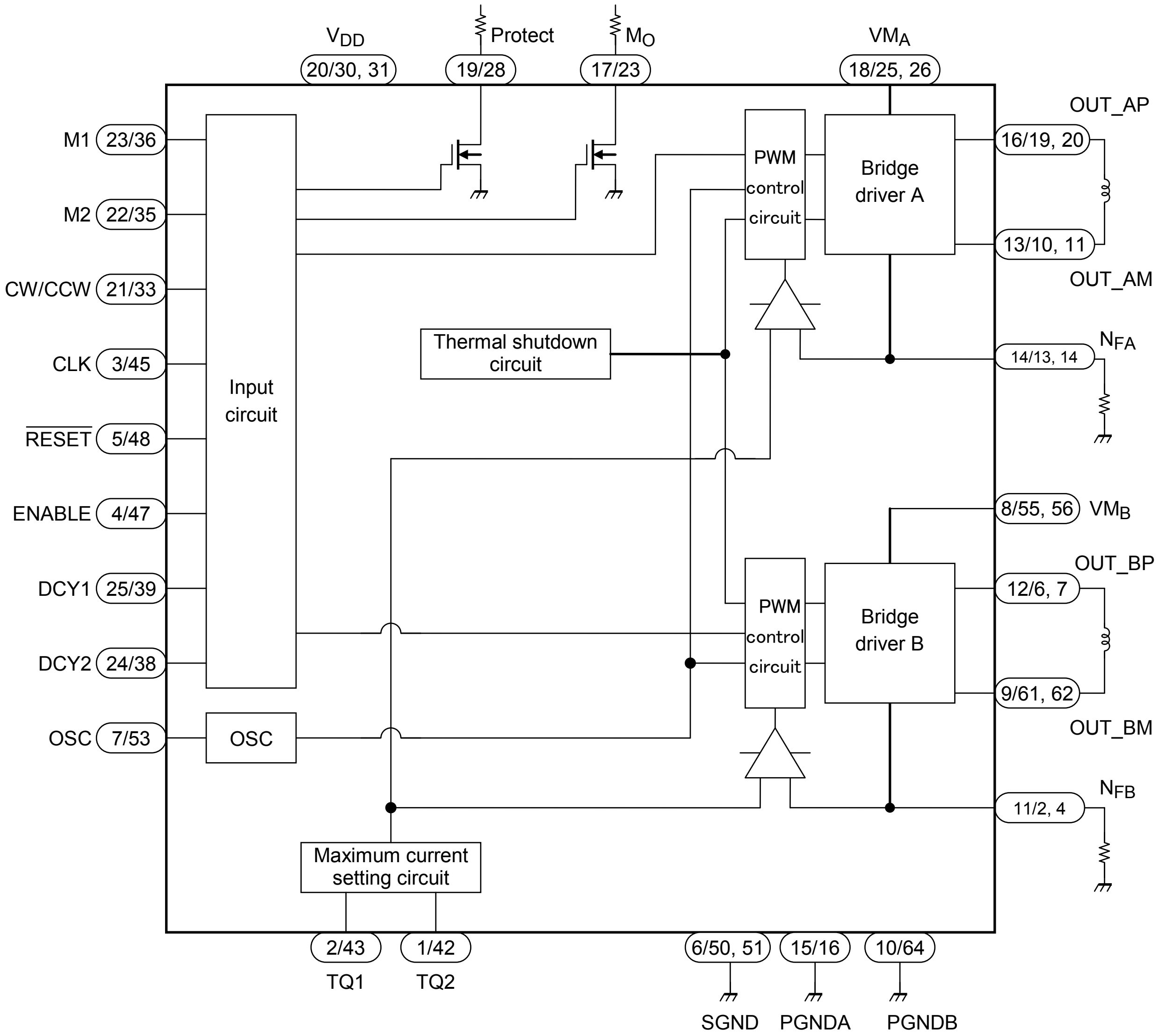
Weight
HZIP25-P-1.27: 9.86 g (typ.)
HQFP64-P-1010-0.50: 0.26 g (typ.)

Features

- Single-chip motor driver for sinusoidal microstep control of stepping motors
- High output withstand voltage due to the use of BiCD process: Ron (upper and lower sum) =
  TB6560AHQ: 0.6 Ω (typ.)
  TB6560AFG: 0.7 Ω (typ.)
- Forward and reverse rotation
- Selectable phase excitation modes (2, 1-2, 2W1-2 and 4W1-2)
- High output withstand voltage: V_{DSS} = 40 V
- High output current: I_{OUT} = TB6560AHQ: 3.5 A (peak)
  TB6560AFG: 2.5 A (peak)
- Packages: HZIP25-P-1.27
  HQFP64-P-1010-0.50
- Internal pull-down resistors on inputs: 100 kΩ (typ.)
- Output monitor pin: M_O current (I_{MO} (max) = 1 mA)
- Reset and enable pins
- Thermal shutdown (TSD)

*: These ICs are highly sensitive to electrostatic discharge. When handling them, ensure that the environment is protected against electrostatic discharge. Ensure also that the ambient temperature and relative humidity are maintained at reasonable level.

Block Diagram



TB6560AHQ/TB6560AFG

Pin Functions

Pin No.		I/O	Symbol	Functional Description	Remarks
TB6560 AHQ	TB6560 AFG				
1	42	Input	TQ2	Torque setting input (current setting)	Internal pull-down resistor
2	43	Input	TQ1	Torque setting input (current setting)	Internal pull-down resistor
3	45	Input	CLK	Clock input for microstepping	Internal pull-down resistor
4	47	Input	ENABLE	H: Enable; L: All outputs OFF	Internal pull-down resistor
5	48	Input	$\overline{\text{RESET}}$	L: Reset (The outputs are reset to their initial states.)	Internal pull-down resistor
6	50/51	—	SGND	Signal ground (for control block)	(Note 1)
7	53	—	OSC	A CR oscillation circuit is connected to this pin. Performs output chopping.	
8	55/56	Input	VM_B	Motor power supply pin (for phase-B driver)	(Note 1)
9	61/62	Output	OUT_BM	OUT_B output	(Note 1)
10	64 (*)	—	PGNDB	Power ground	
11	2/4 (*)	—	N_{FB}	Connection pin for a B-channel current sensing resistor Two pins of the TB6560AFG should be short-circuited.	(Note 1)
12	6/7	Output	OUT_BP	OUT_B output	(Note 1)
13	10/11	Output	OUT_AM	OUT_A output	(Note 1)
14	13/14 (*)	—	N_{FA}	Connection pin for an A-channel current sensing resistor Two pins of the TB6560AFG should be short-circuited.	(Note 1)
15	16	—	PGNDA	Power ground	
16	19/20	Output	OUT_AP	OUT_A output	(Note 1)
17	23	Output	M_O	Initial state sensing output. This pin is enabled in the initial state.	Open drain
18	25/26	Input	VM_A	Motor power supply pin (for phase-A driver)	(Note 1)
19	28	Output	Protect	When TSD is activated: High; when in normal state: High-Z.	Open drain
20	30/31	Input	V_{DD}	Power supply pin for control block	(Note 1)
21	33	Input	CW/CCW	Rotation direction select input. L: Clockwise; H: Counterclockwise	Internal pull-down resistor
22	35	Input	M2	Excitation mode setting input	Internal pull-down resistor
23	36	Input	M1	Excitation mode setting input	Internal pull-down resistor
24	38	Input	DCY2	Current decay mode setting input	Internal pull-down resistor
25	39	Input	DCY1	Current decay mode setting input	Internal pull-down resistor

(*): The pin assignment of the TB6560AFG is different from that of the TB6560FG.

TB6560AHQ: There is no no-connect (NC) pin.

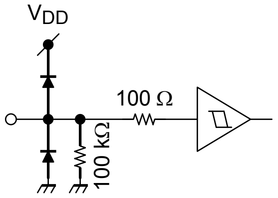
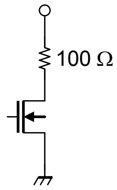
TB6560AFG: Except the above pins, all pins are NC. The pin numbers of NC pins are: 1, 3, 5, 8, 9, 12, 15, 17, 18, 21, 22, 24, 27, 29, 32, 34, 37, 40, 41, 44, 46, 49, 52, 54, 57, 58, 59, 60, and 63.

Applying a voltage to NC pins does not cause any problem since they are not connected inside the IC.

All control input pins have an internal pull-down resistor of 100 kΩ (typ.)

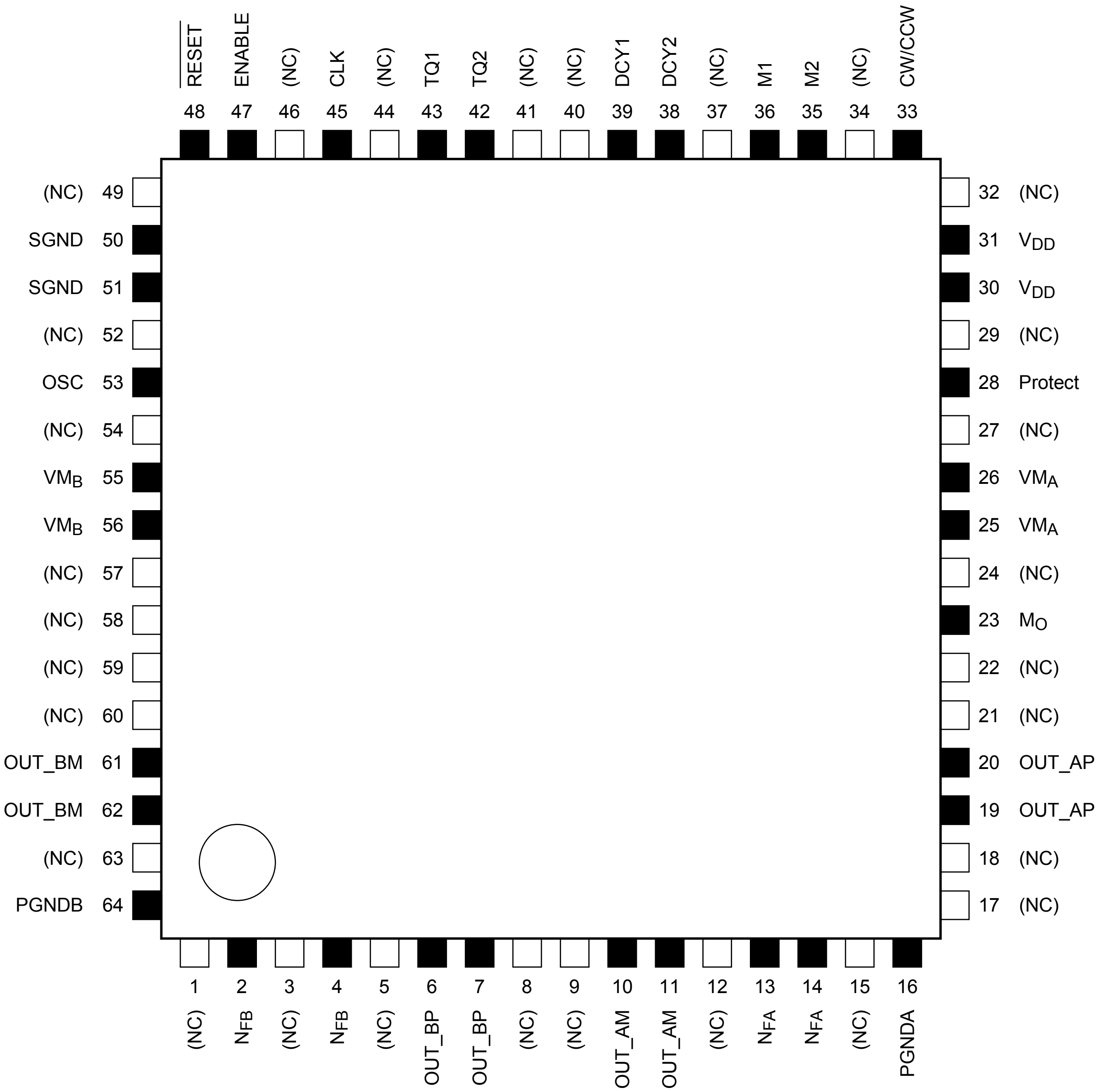
Note 1: As for the TB6560AFG, two pins that have the same functionality should be short-circuited at a location as close to the TB6560AFG as possible.
(The electrical characteristics provided in this document are measured when those pins are handled in this manner.)

Equivalent Circuits

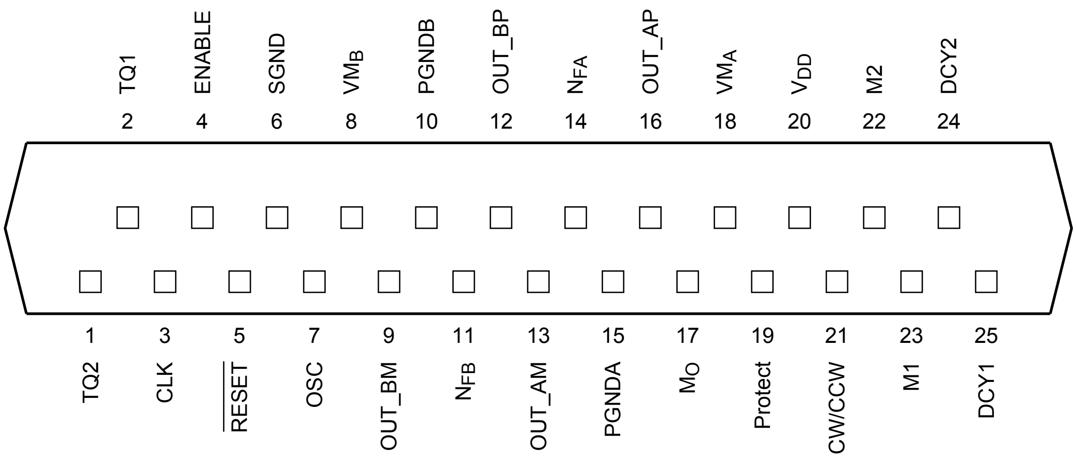
Input Pins (M1, M2, CLK, CW/CCW, TQ1,TQ2,ENABLE, $\overline{RESET}$,DCY1, DCY2)	Output Pins (M_O, Protect)
 	

Pin Assignment (top view)

TB6560AFG



TB6560AHQ



Absolute Maximum Ratings (T_a = 25°C)

Characteristics			Symbol	Rating	Unit
Power supply voltage			V_{DD}	6	V
			$VM_{A/B}$	40	
Output current (per phase)	Peak	TB6560AHQ	$I_{O\ (PEAK)}$	3.5	A
		TB6560AFG		2.5	
M_O drain current			$I_{(Mo)}$	1	mA
Protect drain current			$I_{(Protect)}$	1	mA
Input voltage			V_{IN}	V_{DD}	V
Power dissipation		TB6560AHQ	P_D	5 (Note 1)	W
				43 (Note 2)	
		TB6560AFG		1.7 (Note 3)	
				4.2 (Note 4)	
Operating temperature			T_{opr}	–30 to 85	°C
Storage temperature			T_{stg}	–55 to 150	°C

Note 1: T_a = 25°C, without heatsink.

Note 2: T_a = 25°C, with infinite heatsink (HZIP25).

Note 3: T_a = 25°C, with soldered leads.

Note 4: T_a = 25°C, when mounted on a board (4-layer board).

Operating Range (T_a = –30 to 85°C)

Characteristics		Symbol	Test Condition	Min	Typ.	Max	Unit
Power supply voltage		V_{DD}	—	4.5	5.0	5.5	V
		$VM_{A/B}$	$VM_{A/B} \geq V_{DD}$	4.5	—	34	V
Output current	TB6560AHQ	I_{OUT}	—	—	—	3	A
	TB6560AFG		—	—	—	1.5	
Input voltage		V_{IN}	—	0	—	5.5	V
Clock frequency		f_{CLK}	—	—	—	15	kHz
OSC frequency		f_{OSC}	—	—	—	600	kHz

Electrical Characteristics (T_a = 25°C, V_{DD} = 5 V, VM = 24 V)

Characteristics		Symbol	Test Condition	Min	Typ.	Max	Unit
Input voltage	High	$V_{IN\ (H)}$	M1, M2, CW/CCW, CLK, $\overline{RESET}$, ENABLE, DCY1, DCY2, TQ1, TQ2	2.0	—	V_{DD}	V
	Low	$V_{IN\ (L)}$		−0.2	—	0.8	
Input hysteresis voltage (Note)		V_{INhys}		—	400	—	mV
Input current		$I_{IN\ (H)}$	M1, M2, CW/CCW, CLK, $\overline{RESET}$, ENABLE, DCY1, DCY2, TQ1, TQ2 V_{IN} = 5.0 V Internal pull-down resistor	30	55	80	μA
		$I_{IN\ (L)}$	V_{IN} = 0 V	—	—	1	
V_{DD} supply current		I_{DD1}	Outputs: Open, $\overline{RESET}$: H, ENABLE: H (2, 1-2 phase excitation)	—	3	5	mA
		I_{DD2}	Outputs: Open, $\overline{RESET}$: H, ENABLE: H (4W1−2, 2W1-2 phase excitation)	—	3	5	
		I_{DD3}	$\overline{RESET}$: L, ENABLE: L	—	2	5	
		I_{DD4}	$\overline{RESET}$: H, ENABLE: L	—	2	5	
VM supply current		I_{M1}	$\overline{RESET}$: H/L, ENABLE: L	—	0.5	1	mA
		I_{M2}	$\overline{RESET}$: H/L, ENABLE: H	—	0.7	2	
Channel-to-channel voltage differential		ΔV_O	B/A, C_{OSC} = 330 μF	−5	—	5	%
V_{NF} voltage change according to the torque settings		V_{NFHH}	TQ1 = H, TQ2 = H	10	20	30	%
		V_{NFHL}	TQ1 = L, TQ2 = H	45	50	55	
		V_{NFLH}	TQ1 = H, TQ2 = L	70	75	80	
		V_{NFLL}	TQ1 = L, TQ2 = L	—	—	100	
Minimum clock pulse width		$t_{W\ (CLK)}$	C_{OSC}= 330 pF	30	—	—	μs
M_O output residual voltage		V_{OL} M_O	I_{OL} = 1 mA	—	—	0.5	V
Protect output rest voltage (Note)		V_{OL} Protect	I_{OL} = 1 mA	—	—	0.5	V
TSD threshold (Note)		TSD	—	—	170	—	°C
TSD hysteresis (Note)		TSDhys	—	—	20	—	°C
Oscillating frequency		f_{OSC}	C_{OSC} = 330 pF	60	130	200	kHz

Note: Not tested in production

Electrical Characteristics (T_a = 25°C, V_{DD} = 5 V, VM = 24 V)

Characteristics				Symbol	Test Condition		Min	Typ.	Max	Unit
Output ON-resistance			TB6560AHQ	Ron $_{U1H}$	I_{OUT} = 1.5 A		—	0.3	0.4	Ω
				Ron $_{L1H}$			—	0.3	0.4	
			TB6560AFG	Ron $_{U1F}$	I_{OUT} = 1.5 A		—	0.35	0.5	
				Ron $_{L1F}$			—	0.35	0.5	
A-/B-phase chopping current (Note 1)	4W1-2-phase excitation	2W1-2-phase excitation	1-2-phase excitation	Vector	θ = 0	TQ1 = L, TQ2 = L	—	100	—	%
		—	—		θ = 1/16		—	100	—	
		2W1-2-phase excitation	—		θ = 2/16		93	98	100	
		—	—		θ = 3/16		91	96	100	
		2W1-2-phase excitation	—		θ = 4/16		87	92	97	
		—	—		θ = 5/16		83	88	93	
		2W1-2-phase excitation	—		θ = 6/16		78	83	88	
		—	—		θ = 7/16		72	77	82	
		2W1-2-phase excitation	1-2-phase excitation		θ = 8/16		66	71	76	
		—	—		θ = 9/16		58	63	68	
		2W1-2-phase excitation	—		θ = 10/16		51	56	61	
		—	—		θ = 11/16		42	47	52	
		2W1-2-phase excitation	—		θ = 12/16		33	38	43	
		—	—		θ = 13/16		24	29	34	
		2W1-2-phase excitation	—		θ = 14/16		15	20	25	
		—	—		θ = 15/16		5	10	15	
	2-phase excitation				—		—	100	—	
Reference voltage				V_{NF}	TQ1, TQ2 = L (100 %) OSC = 100 kHz		450	500	550	mV
Output transistor switching characteristics (Note 2)				t_r	R_L = 10 Ω, V_{NF} = 0.5 V		—	1	—	μs
				t_f			—	1	—	
Delay time (Note 2)				t_{pLH}	$\overline{\text{RESET}}$ to output		—	1	—	
				t_{pLH}	ENABLE to output		—	3	—	
				t_{pHL}			—	2	—	
Output leakage current			Upper side	I_{LH}	VM = 40 V		—	—	1	μA
			Lower side	I_{LL}			—	—	1	

Note 1: Relative to the peak current at θ = 0.

Note 2: Not tested in production.

Functional Descriptions

1. Excitation Mode Settings

The excitation mode can be selected from the following four modes using the M1 and M2 inputs. (The 2-phase excitation mode is selected by default since both M1 and M2 have internal pull-down resistors.)

Inputs		Mode (Excitation)
M2	M1	
L	L	2-phase
L	H	1-2-phase
H	L	4W1-2-phase
H	H	2W1-2-phase

2. Function Table (Relationship Between Inputs and Output Modes)

When the ENABLE pin is Low, outputs are off. When the $\overline{\text{RESET}}$ pin is Low, the outputs are put in the Initial mode as shown in the table below. In this mode, the states of the CLK and CW/CCW pins are don't-cares.

Inputs				Output Mode
CLK	CW/CCW	$\overline{\text{RESET}}$	ENABLE	
↑	L	H	H	CW
↑	H	H	H	CCW
X	X	L	H	Initial mode
X	X	X	L	Z

X: Don't care

3. Initial Mode

When $\overline{\text{RESET}}$ is asserted, phase currents in each excitation mode are as follows. At this time, the MO pin goes Low (open-drain connection).

Excitation Mode	A-Phase Current	B-Phase Current
2-phase	100 %	−100 %
1-2-phase	100 %	0 %
2W1-2-phase	100 %	0 %
4W1-2-phase	100 %	0 %

4. Decay Mode Settings

It takes approximately four OSC cycles for discharging a current in PWM mode. The 25 % decay mode is created by inducing decay during the last cycle in Fast Decay mode; the 50 % Decay mode is created by inducing decay during the last two cycles in Fast Decay mode; and the 100 % Decay mode is created by inducing decay during all four cycles in Fast Decay mode.
Since the DCY1 and DCY2 pins have internal pull-down resistors, the Normal mode is selected when DCY1 and DCY2 are undriven.

DCY2	DCY1	Current Decay Setting
L	L	Normal 0 %
L	H	25 % Decay
H	L	50 % Decay
H	H	100 % Decay

5. Torque Settings (Current Value)

The ratio of the current necessary for actual operations to the predefined current adjusted by an external resistor can be selected as follows. The Weak Excitation mode should be selected to set a torque extremely low like when the motor is at a fixed position.
Since the TQ2 and TQ1 pins have pull-down resistors, the 100 % torque setting is selected when TQ2 and TQ1 are undriven.

TQ2	TQ1	Current Ratio
L	L	100 %
L	H	75 %
H	L	50 %
H	H	20 % (Weak excitation)

6. Calculation of the Predefined Output Current

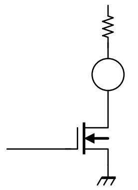
To perform a constant current drive, the reference current should be adjusted by an external resistor. Charging stops when the N_{FA} (N_{FB}) voltage reaches 0.5 V (when the torque setting is 100 %) so that a current does not exceed the predefined level.
I_{OUT} (A) = 0.5 (V) / R_{NF} (Ω)
Example: To set the peak current to 1 A, the value of an external resistor should be 0.5 Ω.

7. Protect and M_O Output Pins

These are open-drain outputs. An external pull-up resistor should be added to these pins when in use. If the TSD circuit is activated, Protect is driven Low. When the IC enters the Initial state, M_O is driven Low.

Pin State	Protect	M_O
Low	Thermal shutdown	Initial state
High-Z	Normal operation	Other than the initial state

Open-drain connection



Rest voltage of output terminal Mo and output terminal Protect reach 0.5 V (max) when I_O is 1 mA.

8. Adjusting the External Capacitor Value (C_{OSC}) and Minimum Clock Pulse Width ($t_{W(CLK)}$)

A triangular-wave is generated internally by CR oscillation. The capacitor is externally connected to the OSC pin. The recommended capacitor value is between 100 pF and 1000 pF.

Approximate equation: $f_{OSC} = 1/\{ C_{OSC} \times 1.5 \times (10/ C_{OSC} + 1)/66\} \times 1000$ kHz
(Since this is an approximation formula, the calculation result may not be exactly equal to the actual value.)

The approximate values are shown below.
The minimum clock pulse width ($t_{W(CLK)}$) corresponds to the external capacitor (C_{OSC}) as follows:

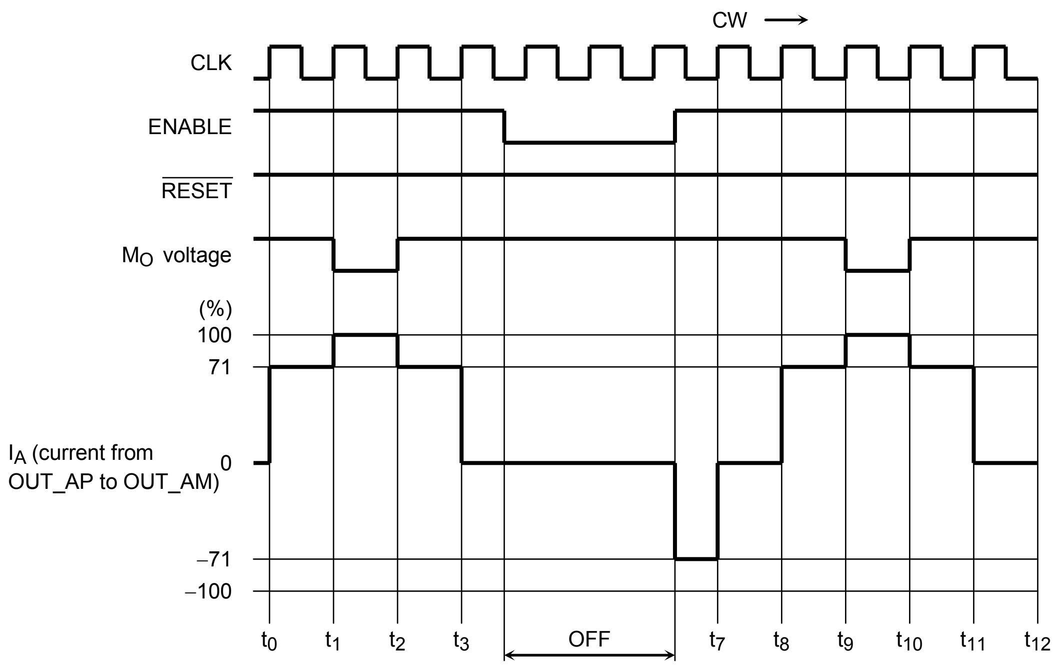
Capacitor	Oscillating Frequency	Minimum Clock Pulse Width $t_{W(CLK)}$ (Note 1)
1000 pF	44 kHz	90 μs (Note 2)
330 pF	130 kHz	30 μs
100 pF	400 kHz	10 μs (Note 2)

Note 1: When the frequency of an input clock signal is high, the C_{OSC} value should be small so that the duty cycle of an input clock pulse does not become extremely high (should be around 50 % or lower).

Note 2: Not tested in production.

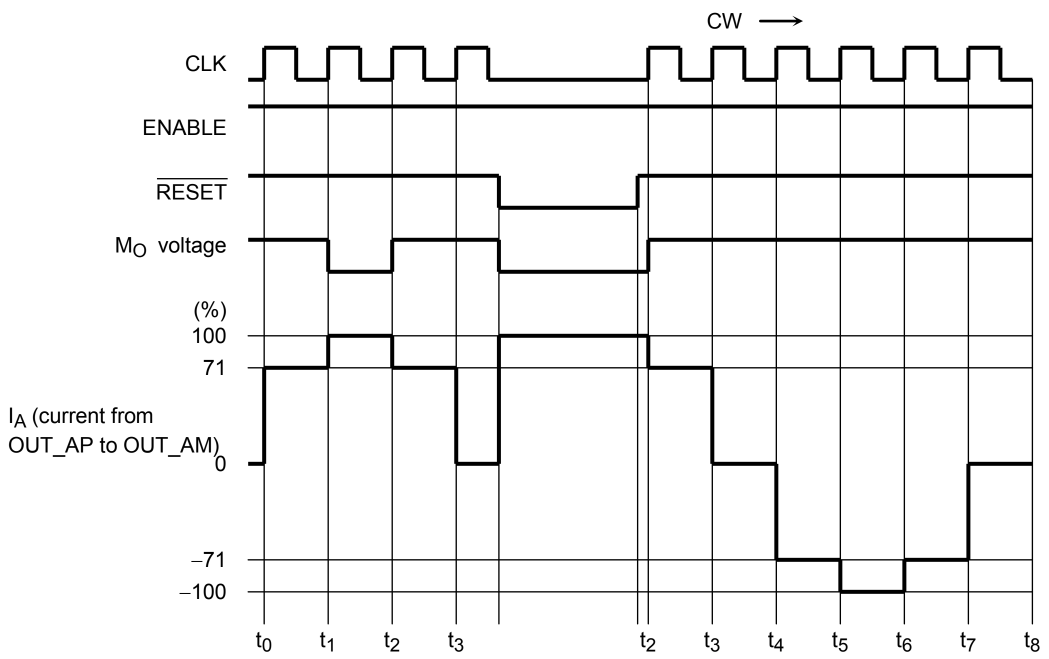
Relationship between the Enable and $\overline{\text{RESET}}$ and Output Signals

Example 1: ENABLE input in 1-2-phase excitation mode (M1: H, M2: L)



Setting the ENABLE signal Low disables only the output signals, while internal circuitry other than the output block continues to operate in accordance with the CLK input. Therefore, when the ENABLE signal goes High again, the output current generation is restarted as if phases proceeded with the CLK signal.

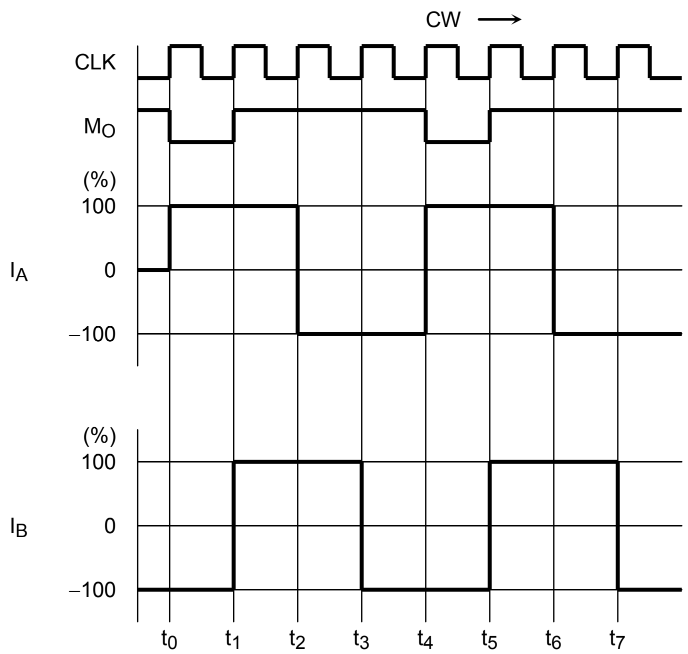
Example 2: $\overline{\text{RESET}}$ input in 1-2-phase excitation mode (M1: H, M2: L)



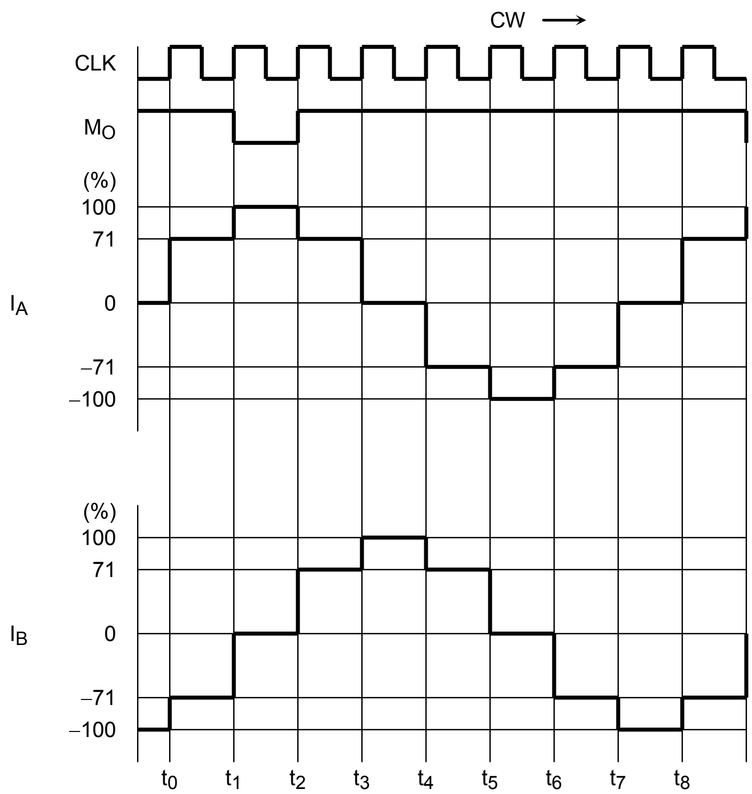
Setting the $\overline{\text{RESET}}$ signal Low causes the outputs to be put in the Initial state and the M_O output to be driven Low (Initial state: A-channel output current is at its peak (100 %)).

When the $\overline{\text{RESET}}$ signal goes High again, the output current generation is restarted at the next rising edge of CLK with the state following the Initial state.

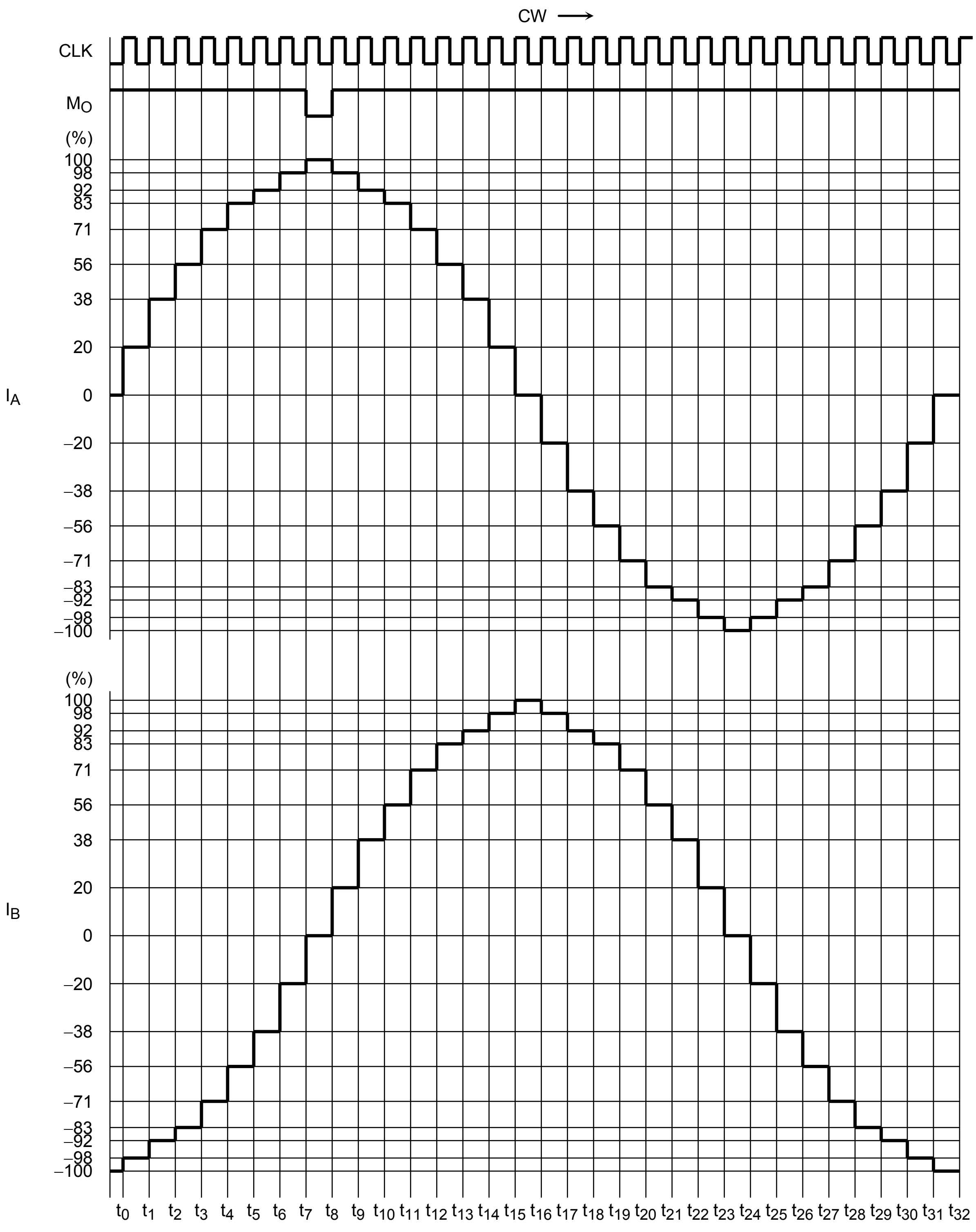
2-Phase Excitation (M1: L, M2: L, CW Mode)



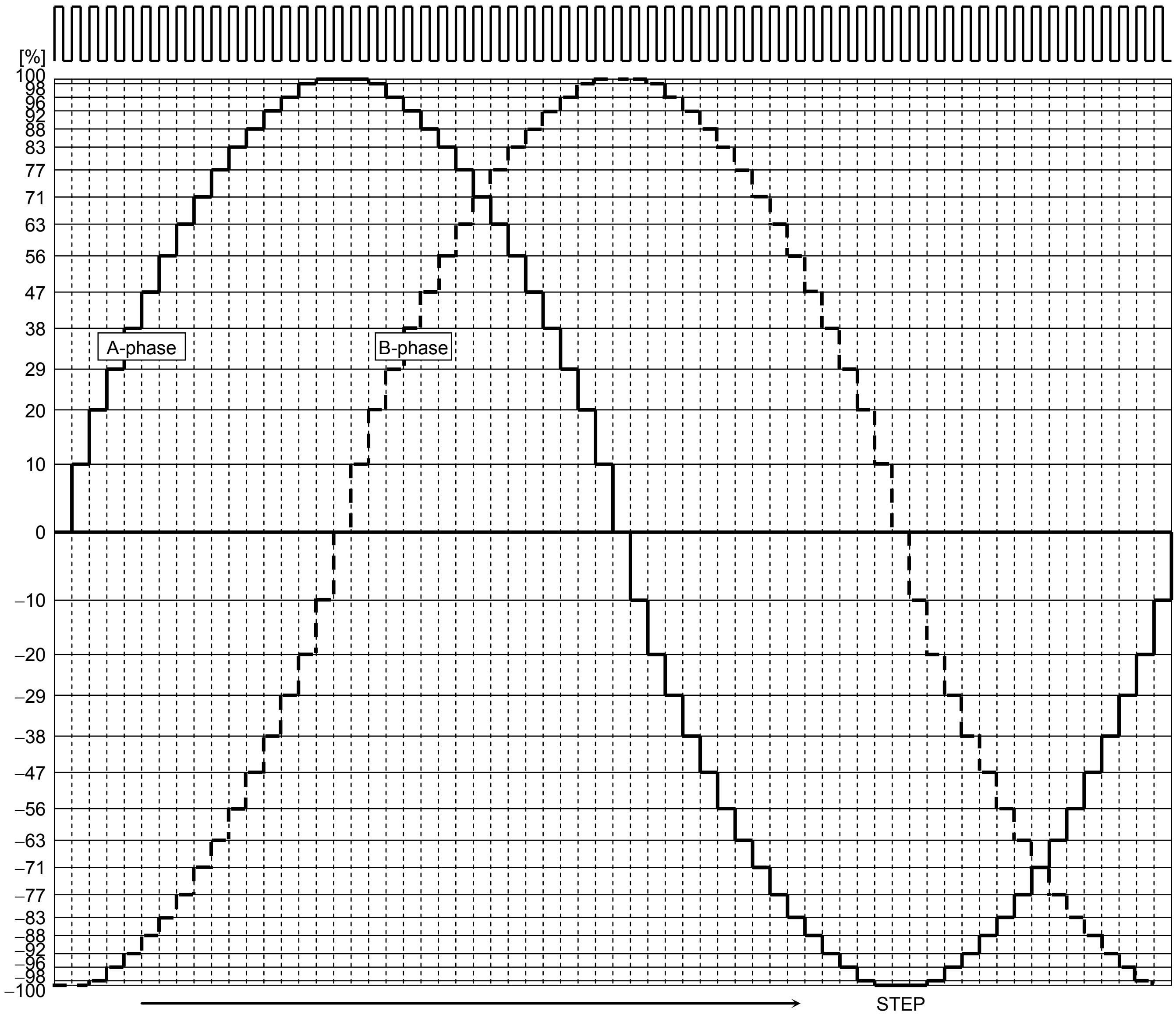
1-2-Phase Excitation (M1: H, M2: L, CW Mode)



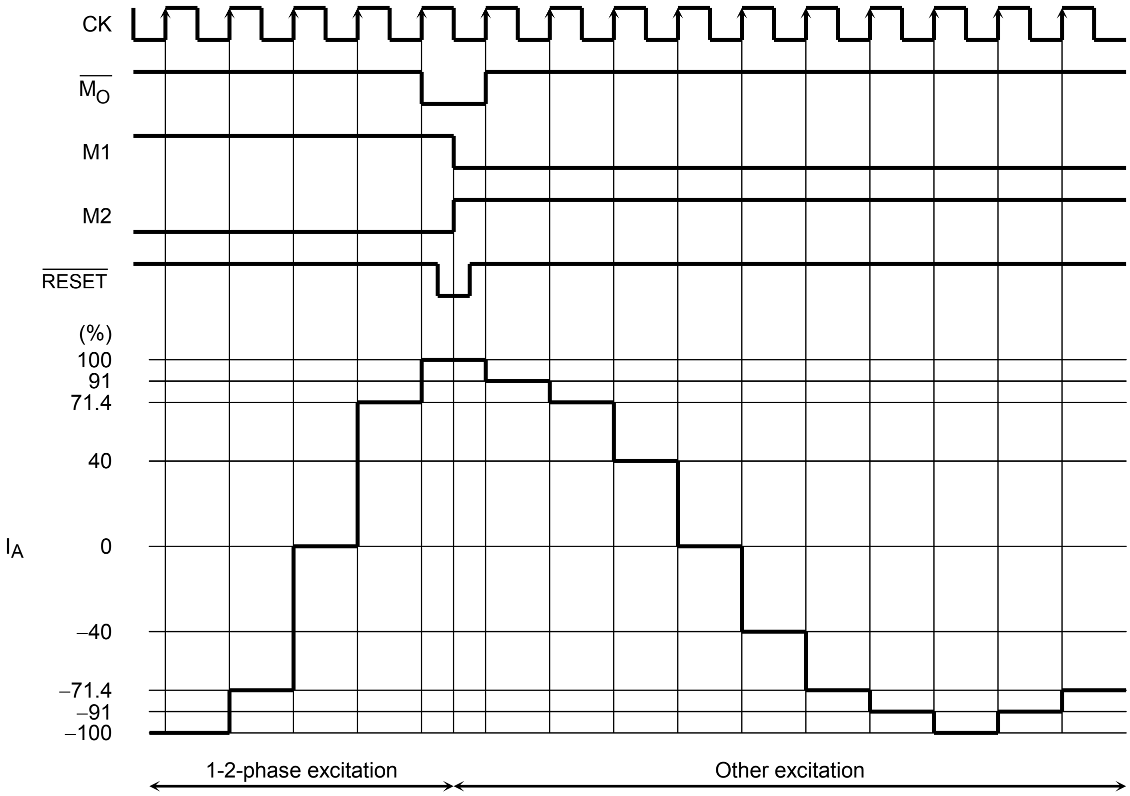
2W1-2-Phase Excitation (M1: H, M2: H, CW Mode)



4W1-2-Phase Excitation (M1: L, M2: H, CW Mode)



<Input Signal Example>



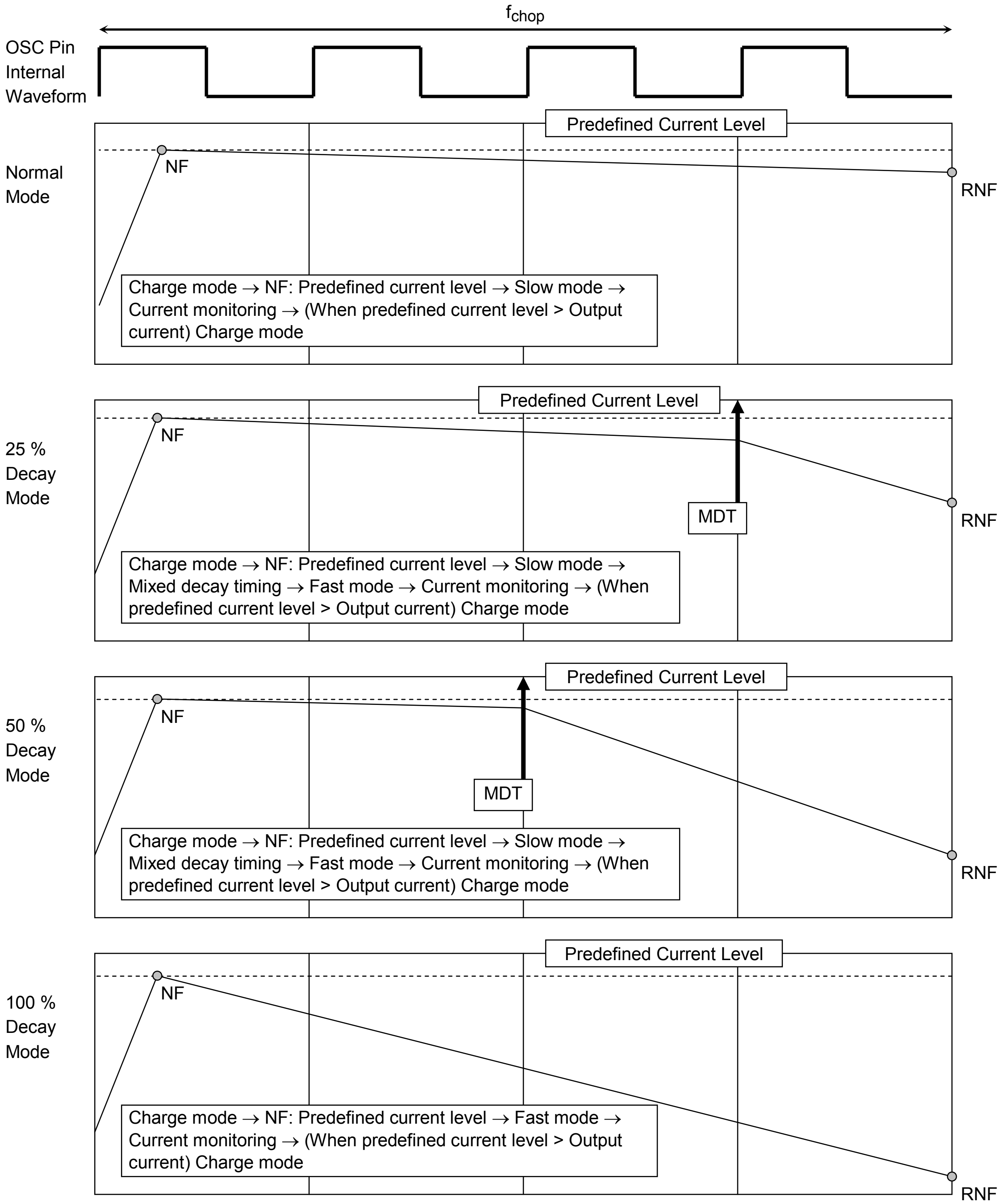
It is recommended that the state of the M1 and M2 pins be changed after setting the $\overline{RESET}$ signal Low during the Initial state (M_O = Low). Even when the M_O signal is Low, changing the M1 and M2 signals without setting the $\overline{RESET}$ signal Low may cause a discontinuity in the current waveform.

9. Current Waveforms and Mixed Decay Mode Settings

The current decay rate of the Decay mode operation can be determined by the DCY1 and DCY2 inputs for constant-current control.

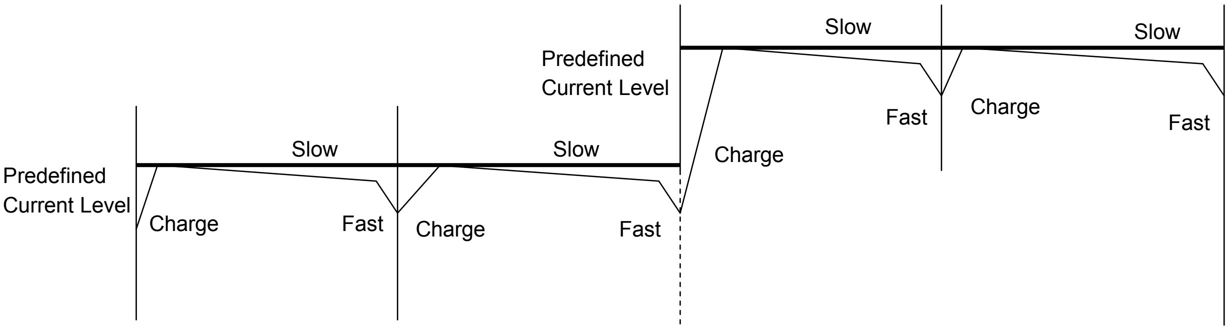
The “NF” refers to the point at which the output current reaches its predefined current level, and the “RNF” refers to the monitoring timing of the predefined current.

The smaller the MDT value, the smaller the current ripple amplitude. However, the current decay rate decreases.

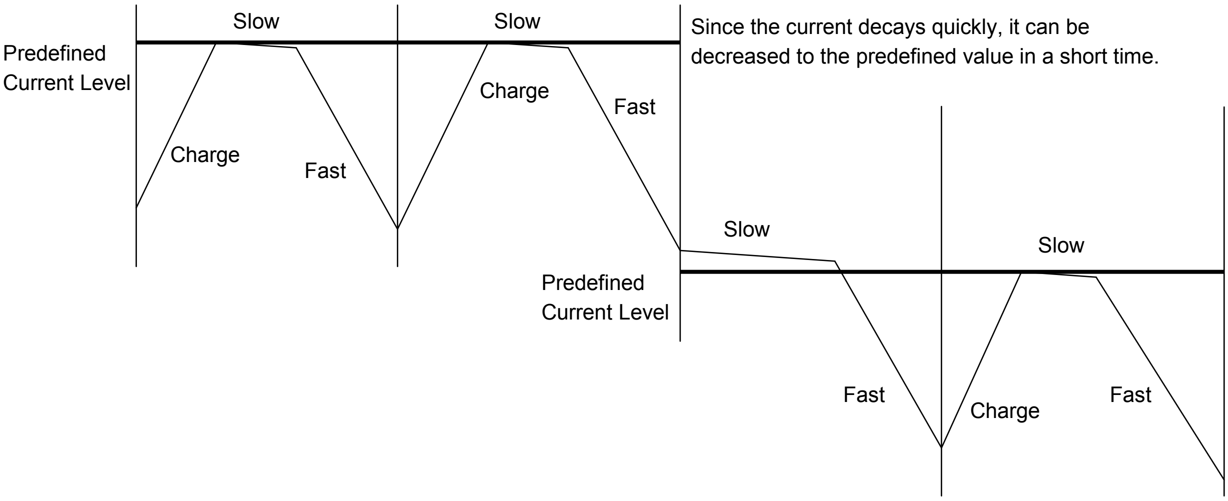


10. Current Control Modes (Effects of Decay Modes)

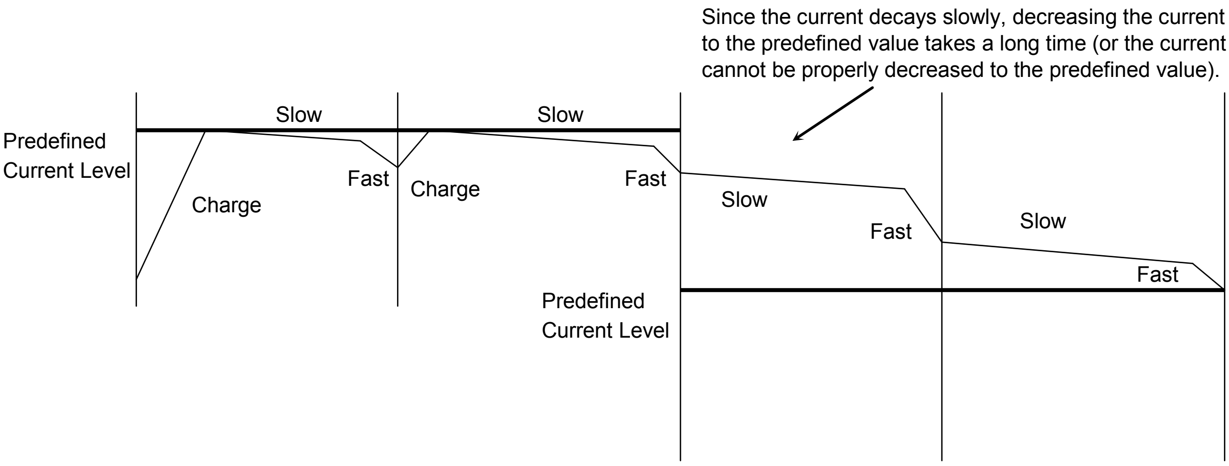
- Increasing the current (sine wave)



- Decreasing the current with a high decay rate (The current decay rate in Mixed Decay mode is the ratio between the time in Fast-Decay mode (discharge time after MDT) and the remainder of the period.)



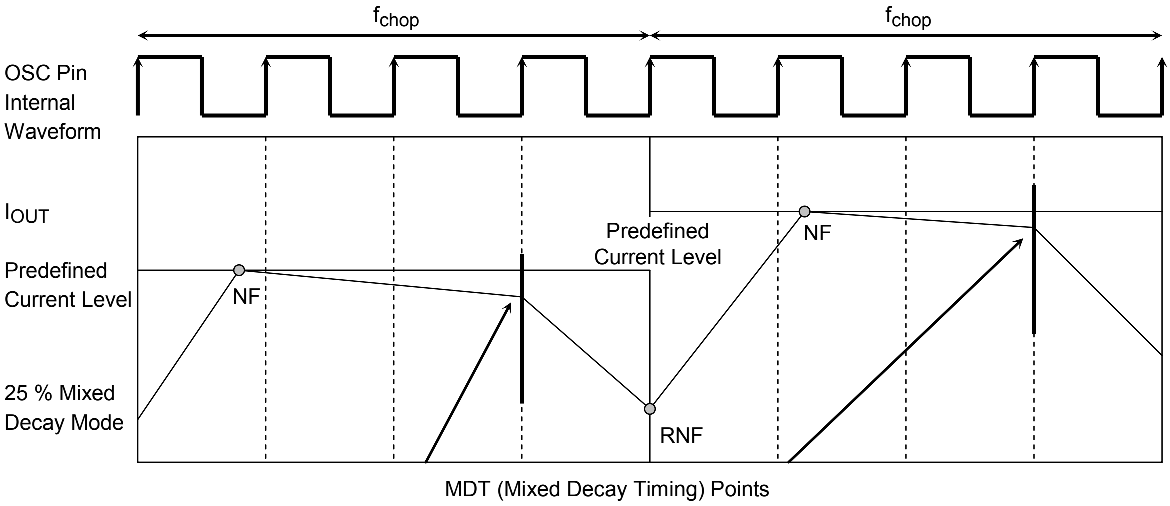
- Decreasing the current with a low decay rate (The current decay rate in Mixed Decay mode is the ratio between the time in Fast-Decay mode (discharge time after MDT) and the remainder of the period.)



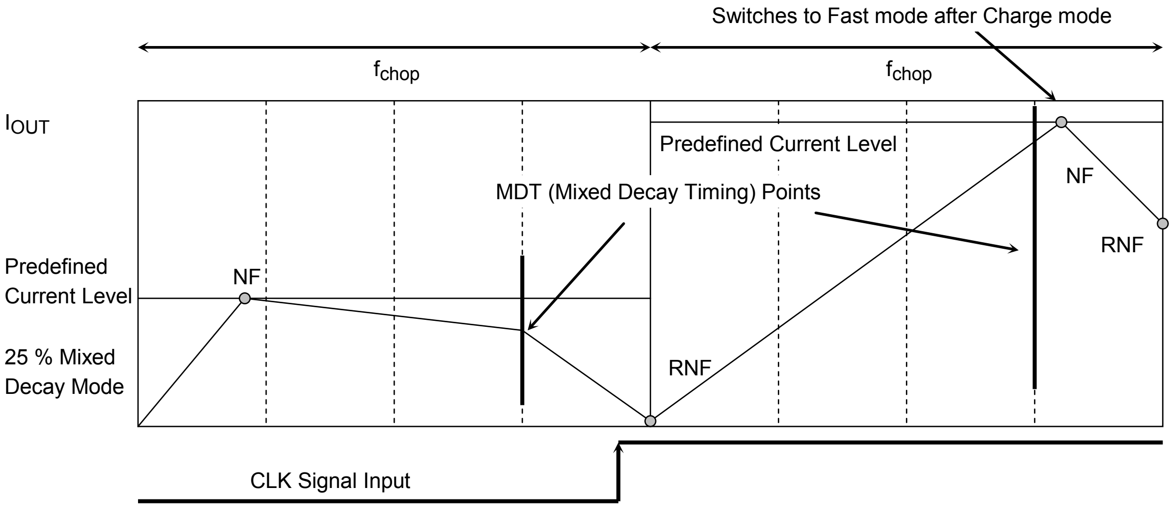
During Mixed Decay and Fast Decay modes, if the predefined current level is less than the output current at the RNF (current monitoring point), the Charge mode in the next chopping cycle will disappear (though the current control mode is briefly switched to Charge mode in actual operations for current sensing) and the current is controlled in Slow and Fast Decay modes (mode switching from Slow Decay mode to Fast Decay mode at the MDT point).

Note: The above figures are rough illustration of the output current. In actual current waveforms, transient response curves can be observed.

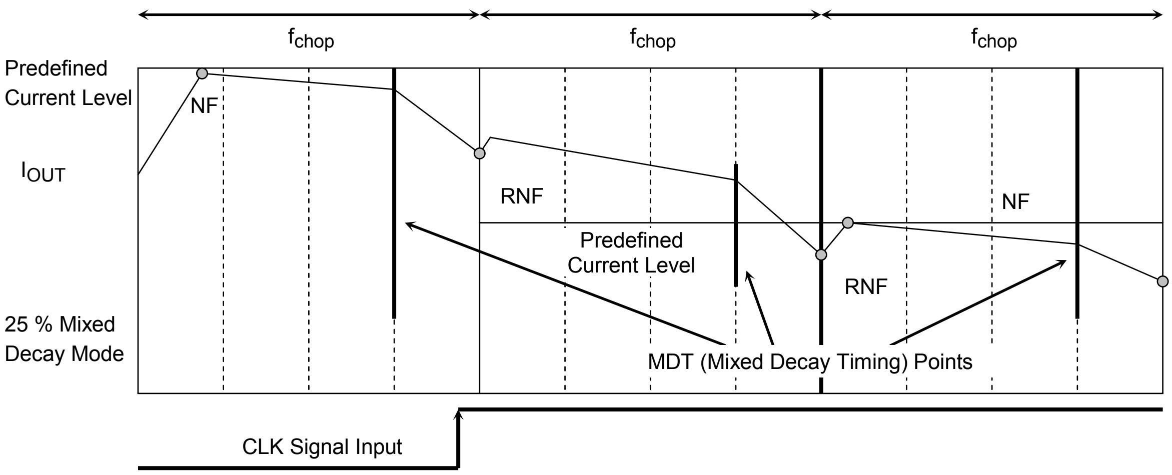
11. Current Waveforms in Mixed Decay Mode



- When the NF points come after Mixed Decay Timing points



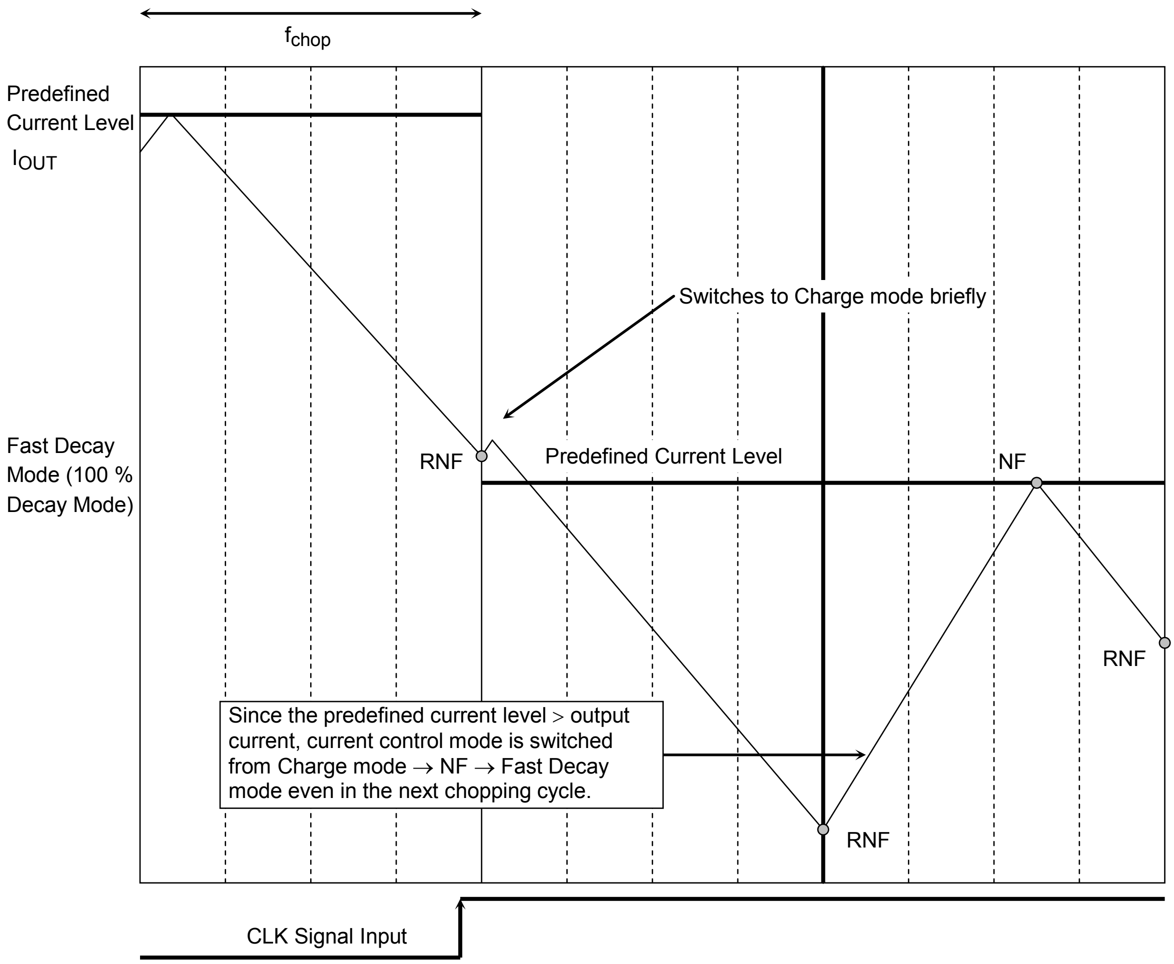
- When the output current value > predefined current level in Mixed Decay mode



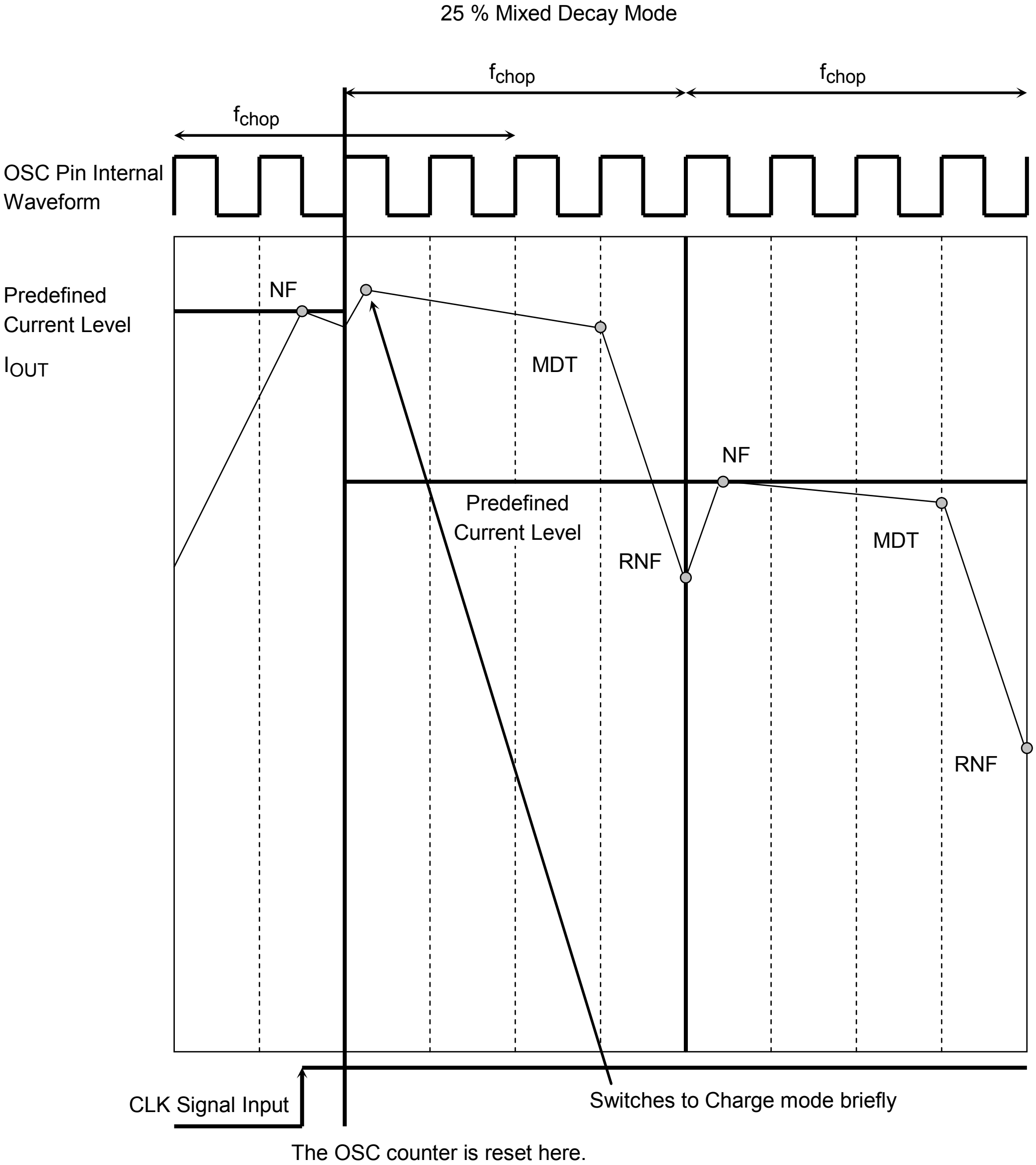
*: Even if the output current rises above the predefined current at the RNF point, the current control mode is briefly switched to Charge mode for current sensing.

12. Current Waveform in Fast Decay Mode

After the output current to the load reaches the current value specified by RNF, torque or other means, the output current to the load will be fed back to the power supply fully in Fast Decay mode.



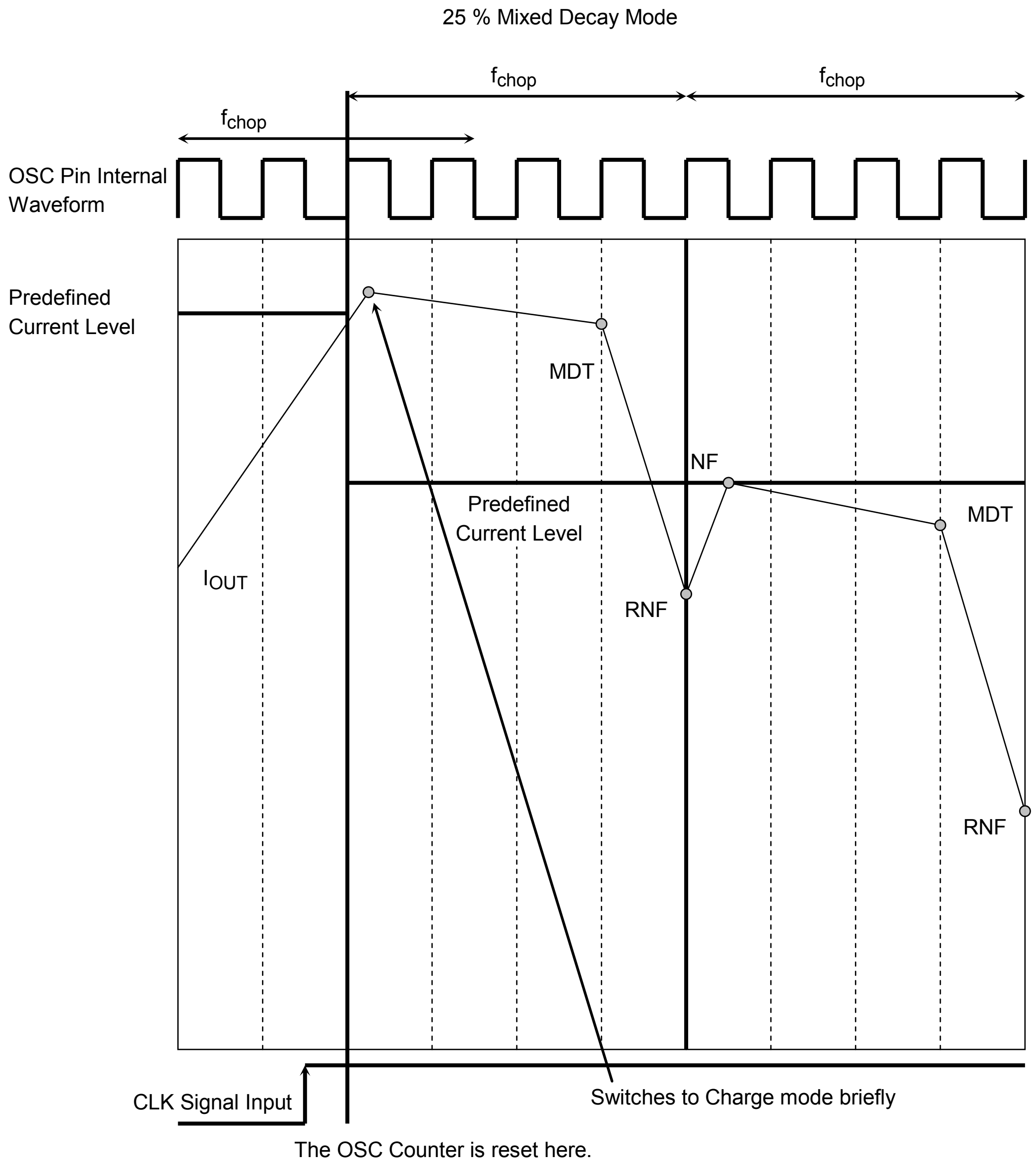
13. CLK and Internal OSC Signals and Output Current Waveform (when the CLK signal is asserted during Slow Decay mode)



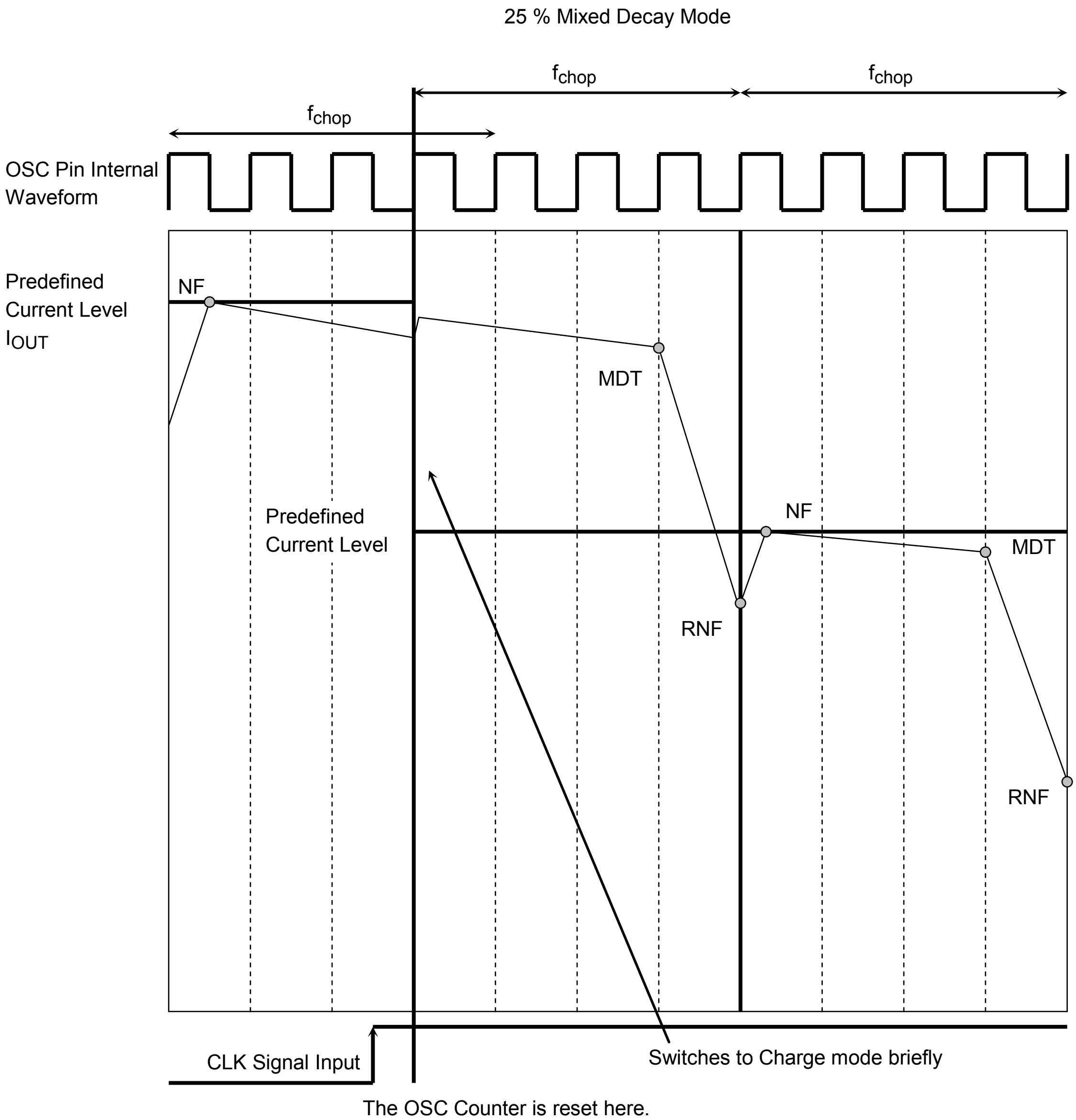
When the CLK signal is asserted, the Chopping Counter (OSC Counter) is forced to reset at the next rising edge of the OSC signal.
As a result, the response to input data is faster compared to methods in which the counter is not reset.
The delay time that is theoretically determined by the logic circuit is one OSC cycle = 10 μs at a 100-kHz chopping rate.
After the OSC Counter is reset by the CLK signal input, the current control mode is invariably switched to Charge mode briefly for current sensing.

Note: Even in Fast Decay mode, the current control mode is invariably switched to Charge mode briefly for current sensing.

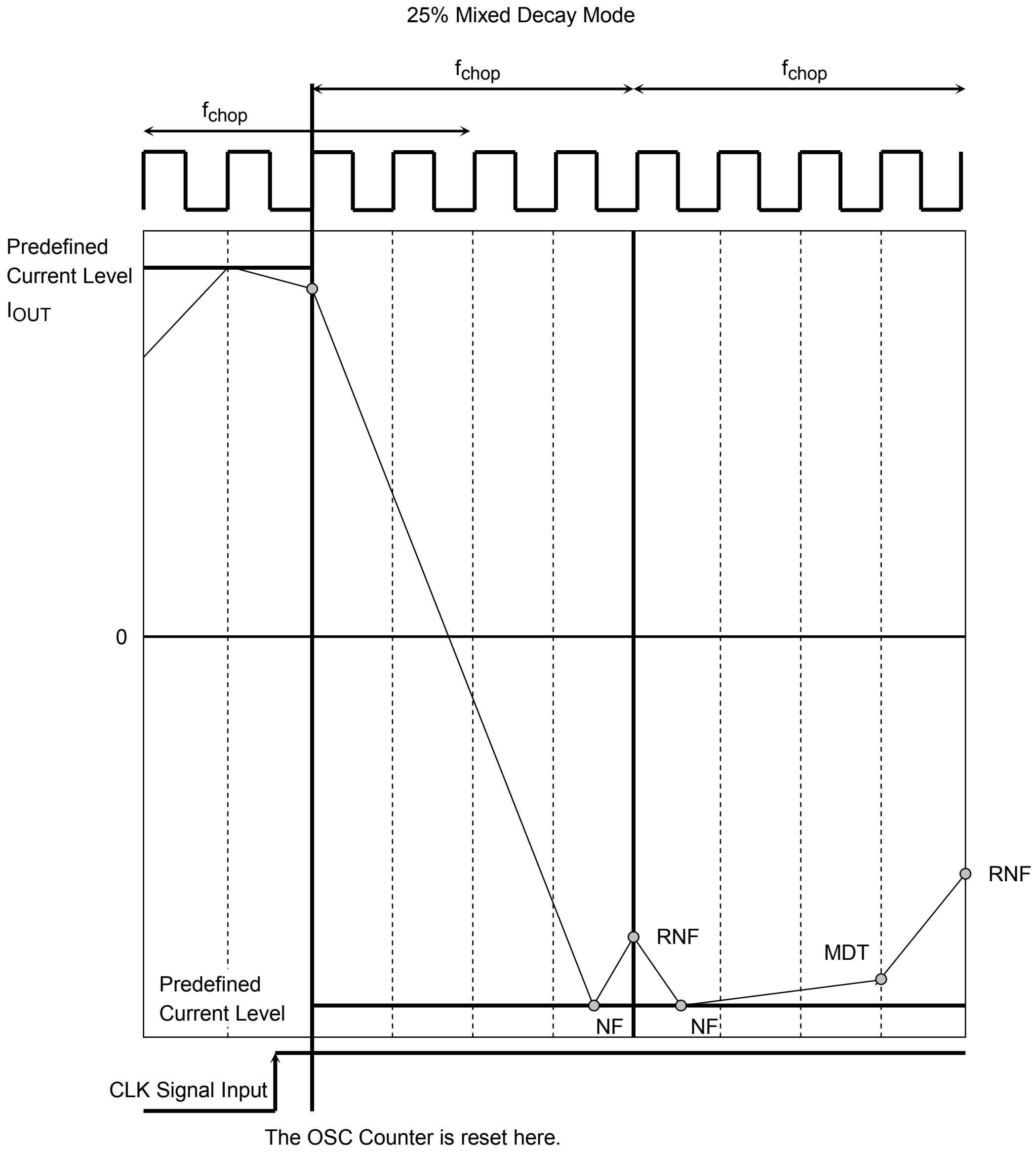
14. CLK and Internal OSC Signals and Output Current Waveform (when the CLK signal is asserted during Charge mode)



15. CLK and Internal OSC Signals and Output Current Waveform (when the CLK signal is asserted during Fast Decay mode)



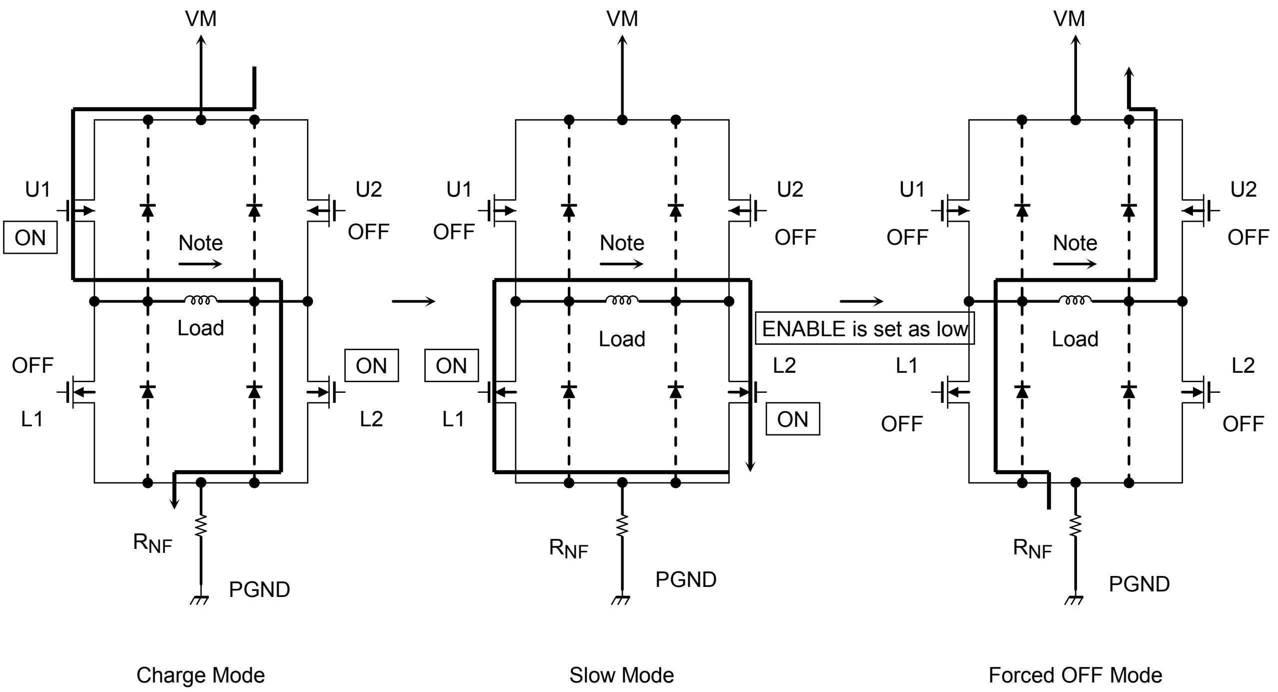
16. Internal OSC Signal and Output Current Waveform when Predefined Current is Changed from Positive to Negative (when the CLK signal is input using 2-phase excitation)



Current Discharge Path when ENABLE is Set as Low During Operation

When all the output transistors are forced off during Slow Decay mode, the coil energy is discharged in the following modes:

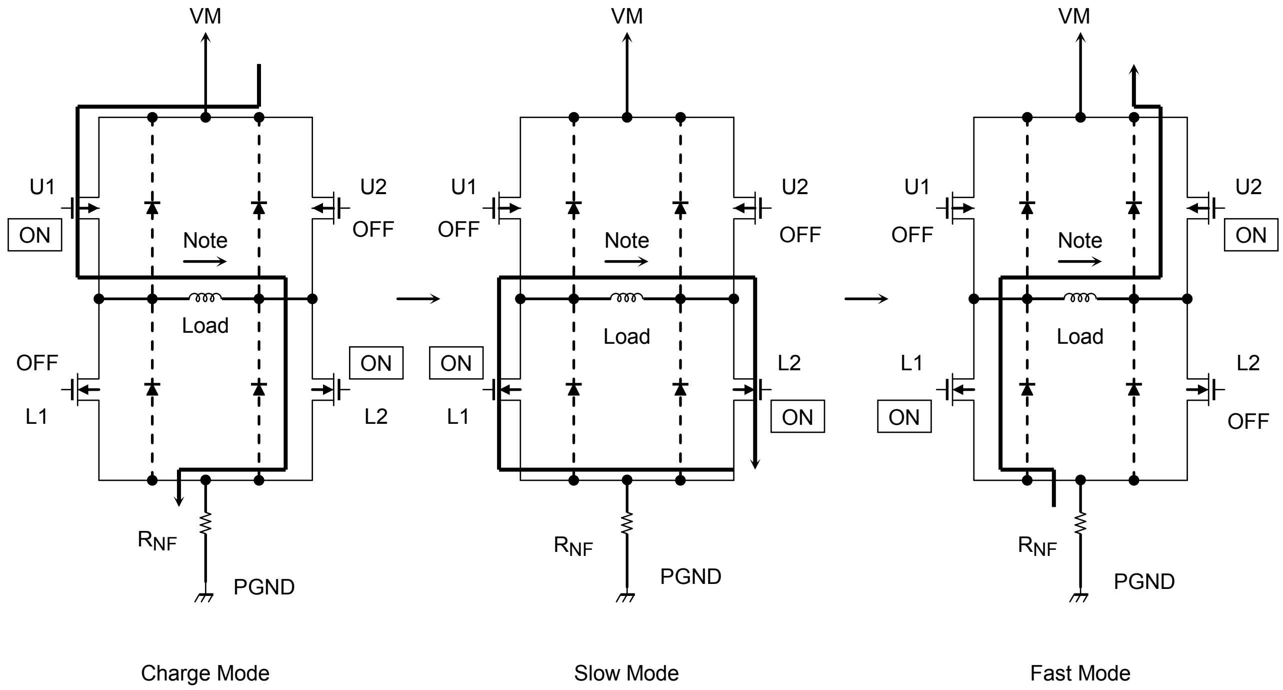
Note: Parasitic diodes are located on dotted lines. However, they are not normally used in normal Mixed Decay mode.



As shown in the figure above, output transistors have parasitic diodes.

Normally, when the energy of the coil is discharged, each transistor is turned on allowing the current to flow in the reverse direction to that in normal operation; as a result, the parasitic diodes are not used. However, when all the output transistors are forced off, the coil energy is discharged via the parasitic diodes.

Output Transistor Operating Modes



Output Transistor Operating Modes

CLK	U1	U2	L1	L2
Charge	ON	OFF	OFF	ON
Slow Decay	OFF	OFF	ON	ON
Fast Decay	OFF	ON	ON	OFF

Note: This table shows an example of when the current flows as indicated by the arrows in the above figures. If the current flows in the opposite direction, refer to the following table:

CLK	U1	U2	L1	L2
Charge	OFF	ON	ON	OFF
Slow Decay	OFF	OFF	ON	ON
Fast Decay	ON	OFF	OFF	ON

Upon transitions of above-mentioned modes, a dead time of about 300 ns is inserted between each mode respectively.