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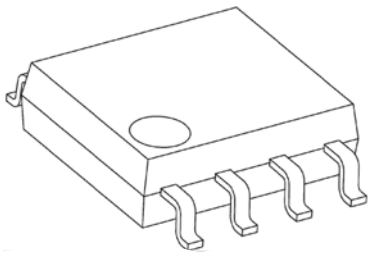
TOSHIBA BiCD Integrated Circuit Silicon Monolithic

TB6819AFG

Critical Conduction Mode (CRM) PFC Controller IC

Features

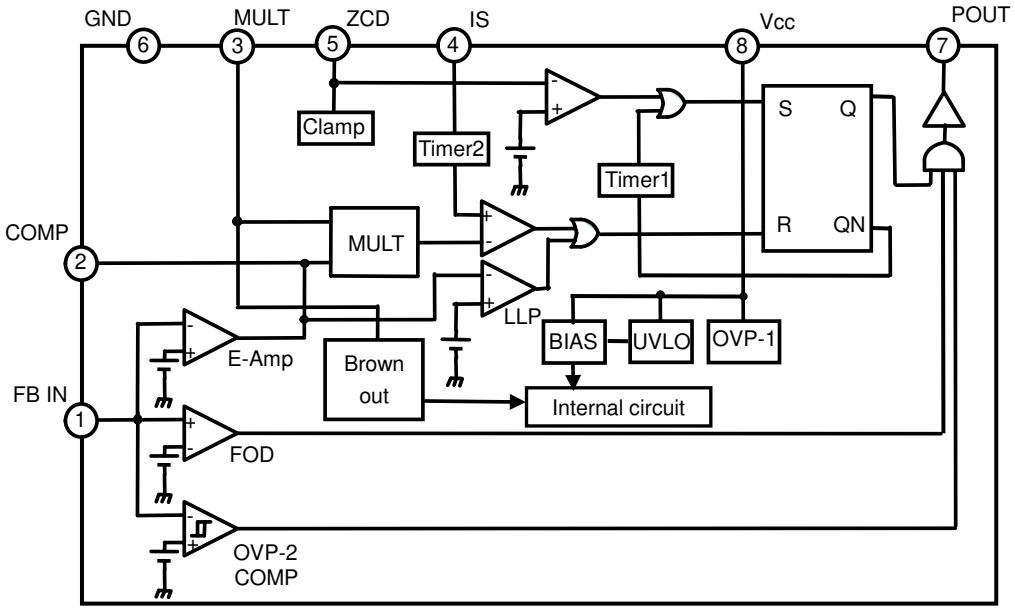
- Operating voltage range: 10.0 to 25 V
- Startup voltage: 12.0 V (typ.)
- Maximum drive current: 1.0 A
- Variety of protection circuits
  - DC Input overvoltage protection (OVP-1)
  - PFC Output overvoltage protection (OVP-2)
  - Under voltage lockout (UVLO)
  - Feedback-loop open detector (FOD)
  - Brown out protection (BOP)
- Package: SOP8



SOP8-P-225-1.27
P-SOP8-0406-1.27-001

Weight: 0.1 g (typ.)

Block Diagram



Absolute Maximum Ratings (Ta = 25°C)

Characteristics	Symbol	Rating	Unit
Supply voltage	Vccmax	25.0	V
Maximum input voltage on all pins	Vinmax	(Note 3)	V
Minimum input voltage on all pins	Vinmin	GND - 0.3	V
Power dissipation 1 (Note 1)	PDmax	650	mW
Operating ambient temperature (Note 2)	Topr	-40 to 90	°C
Junction temperature	Tj	150	°C
Storage temperature	Tstg	-55 to 150	°C

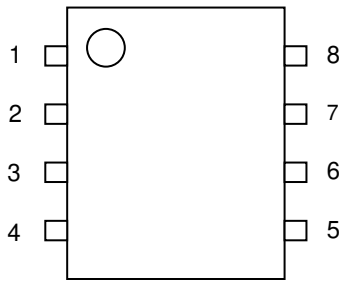
Note 1**:** The rated power dissipation should be decreased by 5.2 mW/°C at above Ta = 25°C ambient.

Note 2**:** Functional operation is guaranteed over the specified temperature range.

Note 3**:** See the table below

Pin No.	Pin Name	Maximum Input Voltage (Rating)	Unit
1	FB IN	5.0	V
2	COMP	5.0	
3	MULT	5.0	
4	IS	5.0	
5	ZCD	7.0	
6	GND	—	
7	POUT	Do not apply any voltage.	
8	Vcc	25.0	

Pin Assignments



1**:** FB IN
2**:** COMP
3**:** MULT
4**:** IS
5**:** ZCD
6**:** GND
7**:** POUT
8**:** Vcc

Pin Function

No.	Pin Name	Functional Description
1	FB IN	Output voltage feedback pin. This is the input of the error amplifier (E-Amp), OVP-2 and FOD. The PFC output voltage should be resistively divided down and applied to this pin. The error amplifier reference voltage is set to 2.51 V (typ.). For other features, see the following. 1. Overvoltage protection on the PFC output (OVP-2) If the PFC output voltage increases and this pin voltage exceeds 2.69 V, the POUT (pin 7) output is forced to Low. The POUT pin will then be enabled again when this pin voltage falls below 2.51 V. 2. Feedback-loop open detection (FOD) If this pin voltage falls below 0.25 V because of error conditions such as a Feedback–loop open, the POUT (pin 7) output is forced to Low. The POUT pin will then be enabled again when this pin voltage reaches 0.5 V.
2	COMP	Error amplifier output. An external filter is required to keep the open loop gain below 0 dB at the frequency twice the AC input frequency that is superimposed on the PFC output. This external filter must be designed to provide enough phase margins.
3	MULT	Detection pin for a full-wave rectified AC voltage waveform. This pin is the input of the multiplier and BOP circuit. The full-wave rectified voltage is resistively divided and connected to this pin. The full-wave rectified voltage applied to this pin is internally multiplied to serve as a reference signal for the PFC operation. If the MULT voltage is below 0.75 V, the BOP is activated and the TB6819AFG does not enter Standby mode. After the TB6819AFG is started, it stops its operation and enters Standby mode if the MULT voltage falls below 0.55 V and peak voltage remains below 0.75 V for 100 ms.
4	IS	Input pin for the current detection comparator. If the IS voltage exceeds the multiplier output voltage, which is the IS comparator reference voltage, the RS flip-flop is reset. Too high a multiplier output voltage causes an external switch to fail to switch off. To avoid this, the upper limit of the IS comparator reference voltage is clamped to 1.7 V.
5	ZCD	Zero current detection pin for an external transformer. The zero-current detector senses an inductor current via the auxiliary winding of the coil and sets the RS flip-flop when the current reaches zero. Since the voltage of auxiliary winding varies significantly, the ZCD pin has an internal clamp circuit. If the inductor current does not reach zero for 200 μs (typ.) while the TB6819AFG is running, the Timer1 restart timer output sets the RS flip-flop and restarts the switching.
6	GND	Ground pin.
7	POUT	Switching pulse output supplied to the FET switch.
8	Vcc	Supply voltage input pin for the TB6819AFG operation. The operating voltage ranges from 10 V (min) to 25 V (max). Owing to the UVLO feature, the TB6819AFG is turned off when Vcc falls below 9.5 V. The TB6819AFG is turned on again when Vcc reaches 12 V.

·Notes when the protection circuits are working

The internal circuit works as shown in the following table when the protectors are operating. Except for TSD, the output of pin 7 is kept at a low level in order to shut down outer FET. Only in the case of TSD is the output of pin 7 is kept floating. It is necessary to connect the pull down resistor of several 10 kΩ to save outer FET when TSD works.

TSD is accorded top priority. Even if the other protector is working, pin 7 floats if the IC temperature exceeds 175°C (typ.).

Protector	Remarks (typ.)	Internal circuit	Pin 7 output
OVP-2	FB IN ≥ Verr (2.51 V) + 180 mV	Working	L
FOD	FB IN ≤ 0.5 V	Working	L
UVLO	Vcc ≤ 9.5 V	Standby	L
Brown out	MULT ≤ 0.75 V	Standby	L
TSD	Chip temperature ≥ 175°C	Standby	Floating

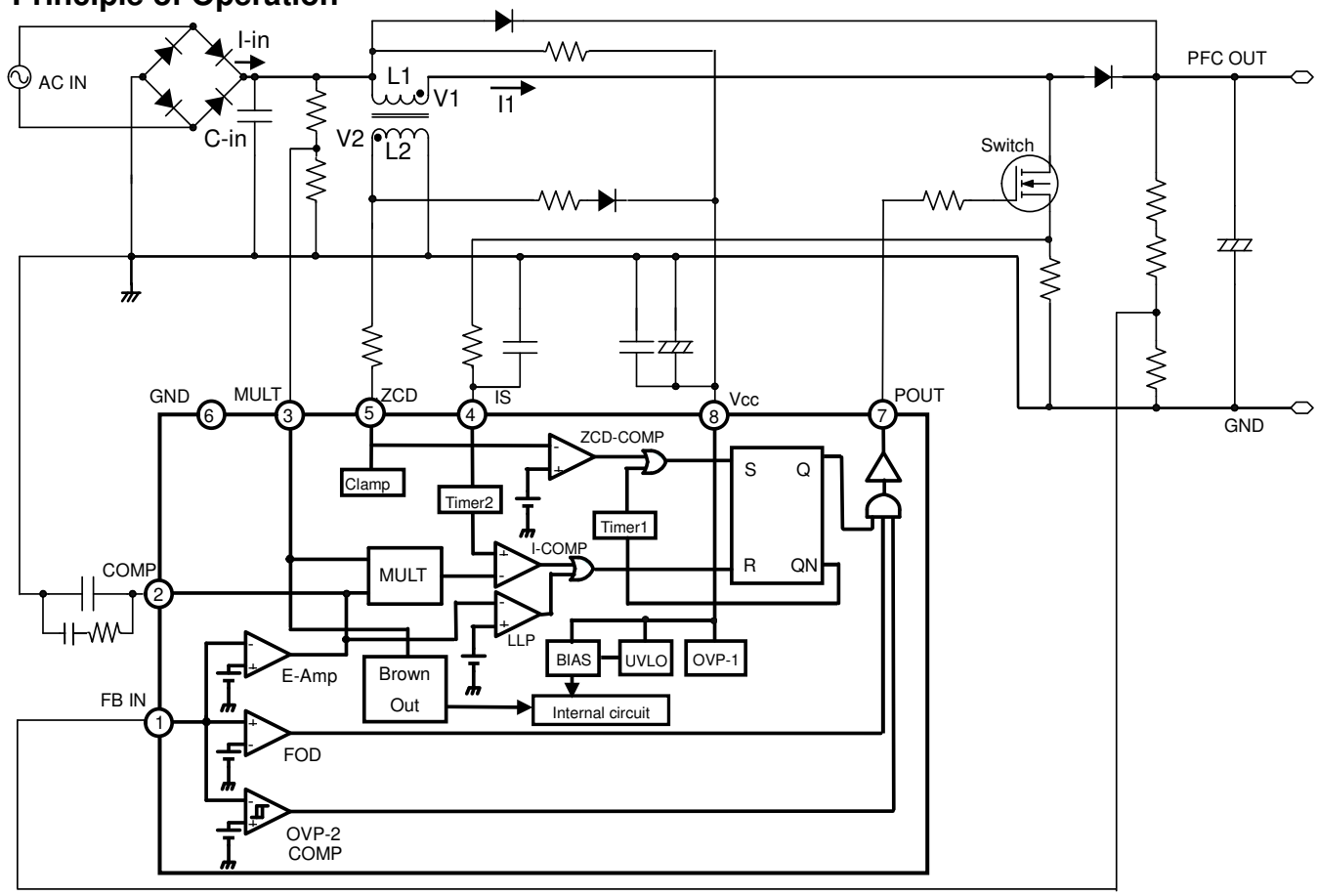
Electrical Characteristics (unless otherwise specified, Vcc = 15V, Ta = 25°C)

Characteristics	Symbol	Remarks	Min.	Typ.	Max.	Unit
Supply voltage range	Vcc	-	10	15	25	V
Current consumption	Icc	75 kHz, 1000 pF	—	4	6.5	mA
Startup current	Istart	At startup	—	72.5	99	μA
Output pulse voltage	V_{OH}	Output load current: 100 mA	Vcc-2.0	—	—	V
	V_{OL}	Output load current: 100 mA	—	—	0.4	
Output pulse rise time	T_{RPF}	Load: 10 Ω, 1000 pF	—	25	50	ns
Output pulse fall time	T_{SPF}	Load: 10 Ω, 1000 pF	—	10	30	ns
Input OVP voltage	V_{OVP-1}	Self-limiting	25	27.5	31.5	V
Output OVP voltage	V_{OVP-2}	Threshold voltage (disables POUT)	Verr+0.12	Verr+0.18	Verr+0.24	V
		Recovery threshold	Verr-0.05	Verr	Verr+0.05	V
FOD trip threshold voltage	V_{FOD}	Threshold voltage (disables POUT)	0.20	0.25	0.30	V
		Hysteresis	180	250	300	mV
UVLO trip threshold voltage	V_{UVLO}	Shutdown threshold	8.8	9.5	10.2	V
		Recovery threshold	11.5	12	12.5	
ZCD trip threshold voltage	V_{ZCD}	Negative-going threshold voltage	1.2	1.4	1.6	V
		Hysteresis	150	300	400	mV
ZCD clamp voltage	V_{ZCDP}	Upper limit: 3 mA	4	5.8	6.3	V
		Lower limit: -3 mA	0.15	0.5	0.9	
E-Amp reference voltage	Verr	-	2.46	2.51	2.56	V
E-Amp mutual conductance	gm	-	55	90	135	μS
Maximum E-Amp current	Ie source	Source	—	-1	—	mA
	Ie sink	Sink	—	1	—	mA
LLP trip threshold voltage	V_{LLP}	Output voltage compensation under light-load conditions	1.8	1.9	2.0	V
IS pin reference voltage	Vis	Upper limit of the IS reference voltage — SOP8-P-225-1.27	1.55	1.7	1.9	V
		Upper limit of the IS reference voltage — P-SOP8-0406-1.27-001	1.64	1.7	1.8	V
IS rise time	ti	Including the RC time constant for noise filtering	210	350	550	ns
Restart time	t res	Timer1	60	200	400	μs
FB IN input current	$I_{FB\ IN}$	FB IN = Open, sink current	-1	—	1	μA
FOD response time	t_{FOD}	-	—	—	1.5	μs
Output OVP response time	t_{OVP-2}	-	—	—	1.5	μs
Quick startup voltage	Vqu	Upper	2.55	2.65	2.80	V
	VqL	Lower	2.1	2.2	2.3	V
MULT input current	I_{MULT}	-	-0.1	—	0.1	μA
MULT gain	G_{MULT}	G_{MULT} × (COMP - 2.5) × MULT = IS COMP = 3.5 V MULT = 2 V – 1 V	0.35	0.5	0.65	—
MULT input linear operation range	V_{LM}	Maximum MULT input voltage(Lower limit: 0V)	3.0	3.5	—	V
	V_{LC}	Maximum COMP input voltage (Lower limit: Verr)	3.5	4.0	—	V
Brown out threshold voltage	Vb	Positive-going threshold voltage (starts the IC)	0.71	0.75	0.79	V
		Hysteresis	0.145	0.2	0.275	V
Brown out turn-on delay	tb	Timer3	50	100	200	ms

Designed values are indicated in following table, these are not tested at the shipping.

Maximum POUT current	Id source	Source (Reference value)	—	0.5	—	A
	Id sink	Sink (Reference value)	—	1.0	—	A
RC time constant for noise filtering	τ_{IS}	Timer2, 40 kΩ / 5 pF (Reference value)	—	200	—	ns
Thermal shutdown threshold	TSD	Threshold temperature (Reference value)	150	175	—	°C
		Hysteresis (Reference value)	—	25	—	°C

Principle of Operation



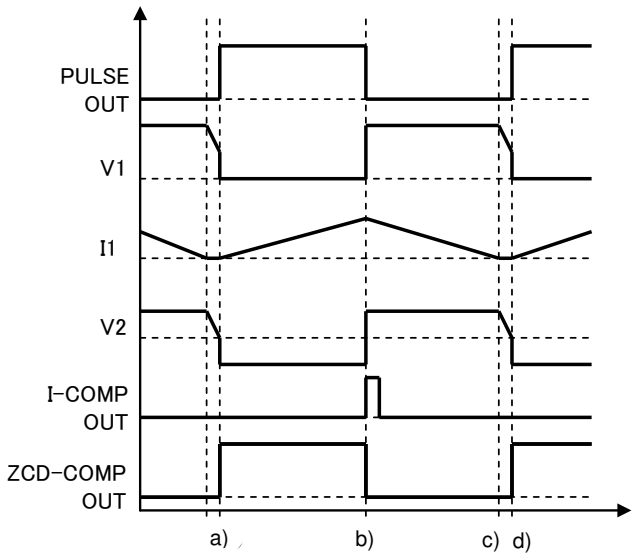
(1) Boost Converter Operation

a) Switch**:** ON → The L1 current increases.

b) The L1 current reaches the I-COMP reference current.
→ RS flip-flop is reset.
→ POUT toggles.
→ Switch goes off.
→ V1 toggles High. → V2 toggles High.

c) The L1 current decreases to zero.
→ The V1 and V2 voltages decrease rapidly.

d) The V2 voltage falls below the ZCD-COMP reference voltage (1.4 V).
→ ZCD-COMP goes High.
→ RS flip-flop is set. → Switch goes on (Back to step "a".)

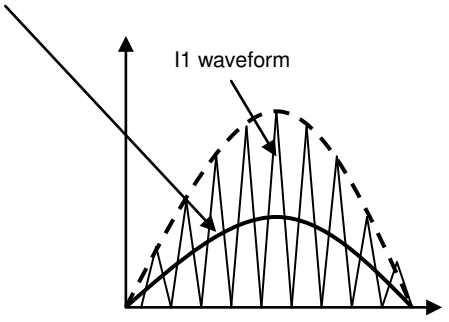


I-in waveform**:** Ripple-current filtering using a capacitor C-in

(2) Power Factor Correction (Critical Conduction Mode)

a) Step 2 causes the I-COMP reference current signal to form a sinusoidal waveform.

b) An envelope of the L1 current that flows upon resetting the RS flip-flop to turn the Switch off forms a sinusoidal waveform.



Waveforms of I-in and I1

Functional Description

(1) Error Amplifier (E-Amp)
This is an error amplifier for regulating the output voltage to be constant. The TB6819AFG internally generates a reference voltage of 2.51 V (typ.).
If the E-Amp output includes the harmonics twice as large as the AC input frequency, the E-Amp system becomes unstable. To avoid this, a filter with a cut-off frequency (fc) of about 20 Hz should be externally connected to the E-Amp output for eliminating harmonics.

(2) DC Input Overvoltage Protection (OVP-1)
This circuit protects the internal circuit from a sudden rise of the Vcc voltage in any event. The OVP-1 incorporates a 27.5V (typ.) voltage limiter.

(3) PFC Output Overvoltage Protection (OVP-2)
This circuit forces the POUT output to Low if the FB IN voltage exceeds 2.69 V (typ.) due to the PFC voltage rise in any event. The POUT output will be enabled again when the FB IN voltage falls below 2.51 V (typ.).

(4) Under Voltage Lockout (UVLO)
This circuit disables the internal circuit if the Vcc voltage falls below 9.5 V (typ.). Once the internal circuit is disabled, it will then be enabled when Vcc reaches 12 V (typ.).

(5) Feedback-Loop Open Detector (FOD)
The POUT output is forced to Low if the FB IN voltage falls below 0.25 V (typ.) because of error conditions such as a feedback–loop open. The POUT output will be enabled again when the FB IN voltage reaches 0.5 V (typ.).

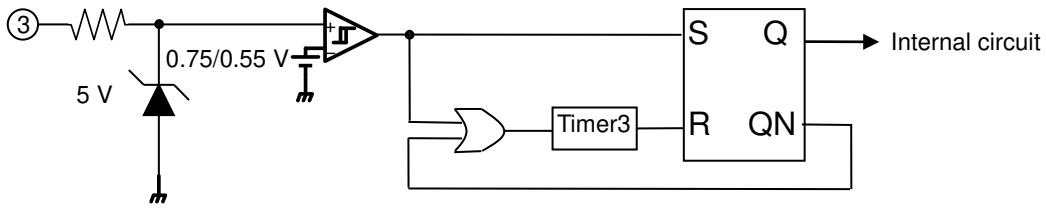
(6) Thermal Shutdown (TSD)
This circuit disables the internal circuit if the chip temperature exceeds 175°C (typ.). The internal circuit will be enabled again when the chip temperature falls below 150°C (typ.).

(7) Light-Load Power Control (LLP)
This function prevents the PFC output voltage from getting too high during no-load and light-load operations.
If an offset voltage is present at the multiplier output, the PFC output voltage might increase abnormally. To avoid this, this feature resets the RS flip-flop if the E-Amp output falls below 1.9 V (typ.).

(8) Restart Timer (Timer1)
This is a restart timer. While the TB6819AFG is running, if the inductor current does not reach zero for 200 μs (typ.), the Timer1 output sets the RS flip-flop and restarts the switching.

(9) Noise Filtering (Timer2)
The TB6819AFG has a filter for filtering pulse noises on the current detect pin (IS pin). Timer2 consists of a 40 kΩ resistor and a 5 pF capacitor.

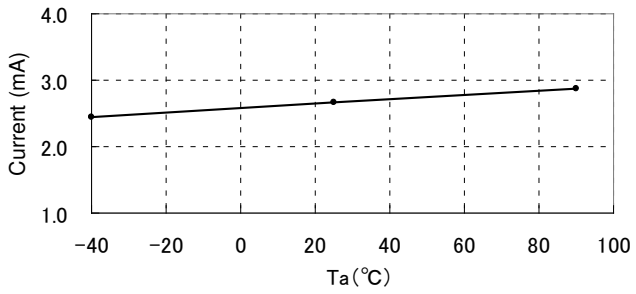
(10) Brown out Protection
Brown out protection disables the internal circuit if AC input voltage falls below the predetermined value. This protection circuit operates separately from the other internal circuits and this feature overrides any other features. At start-up, the RS flip-flop is in the reset state disabling the internal circuit. When the voltage applied to the MULT pin reaches 0.75 V (typ.), the RS flip-flop is set to enable the internal circuit. Timer3 is programmed to start when a logical-OR result of the operation comparator output and the QN output of the RS flip-flop becomes Low. If the logical-OR result is continuously kept Low for 100ms, Timer3 generates a reset pulse for resetting the RS flip-flop. That is, if the MULT voltage falls below 0.55 V and remains below 0.75V for 100ms while the RS flip-flop is set (QN = Low), Timer3 resets the RS flip-flop and puts the TB6819AFG into Standby mode.



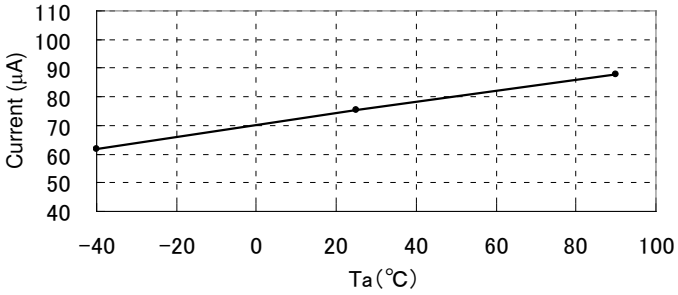
(11) I-COMP
Outputs a reset signal RS-FF by typing what was converted to a voltage source current with a resistor of the MOSFET, compared to the output of the MULT. During this operation, Timer2 filters noise signals having short-pulse durations, such as switching noises. If multiplier output voltage is too high, the RS flip-flop will fail to reset. To avoid this, the upper limit of the IS comparator reference voltage is clamped to 1.7 V.

Typical Performance Curves

Current Consumption vs. Temperature

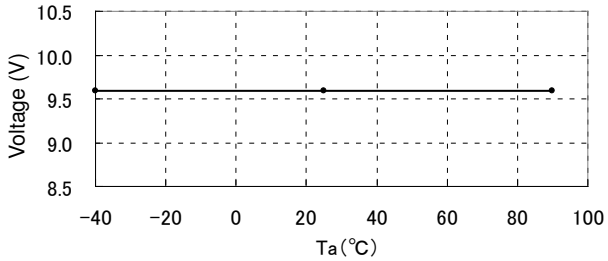


Start up Current Consumption vs. Temperature

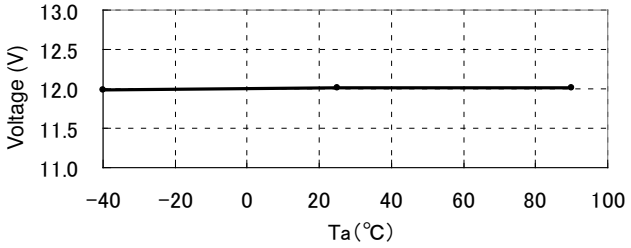


UVLO vs. Temperature

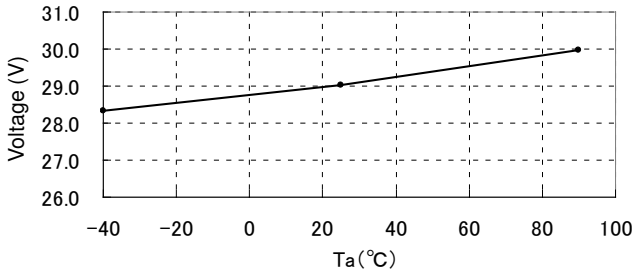
Shut down



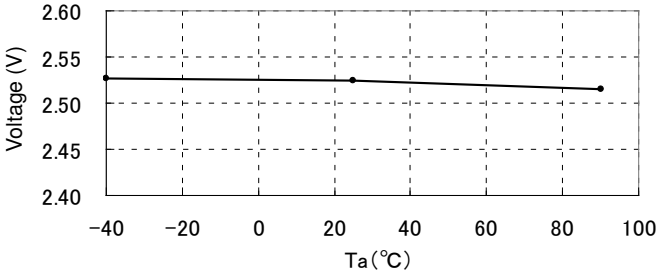
Start up



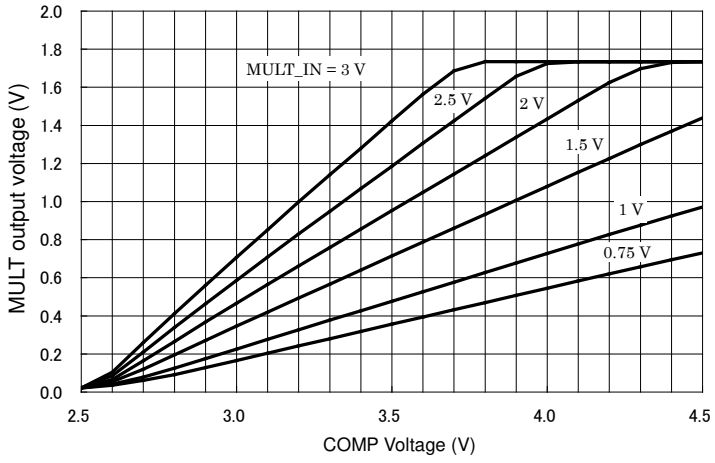
OVP-1 vs. Temperature



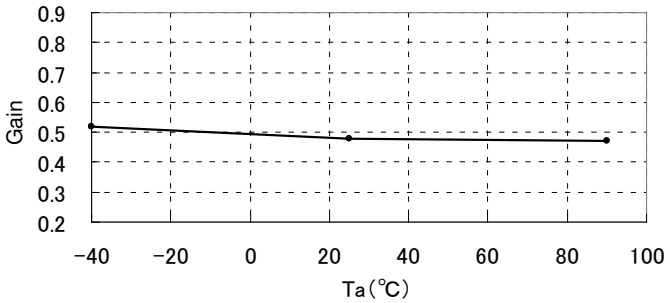
Error Amplifier Reference Voltage vs. Temperature



Multiplier Input-Output Characteristics (Ta = 25°C)

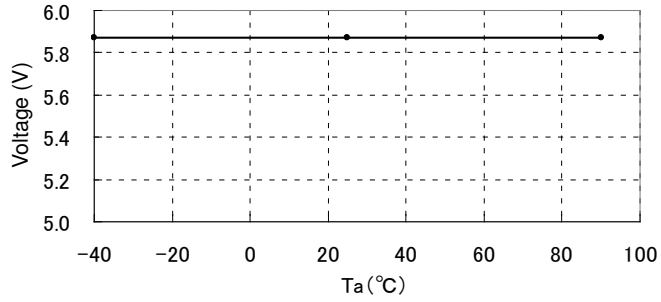


Multiplier Gain vs. Temperature

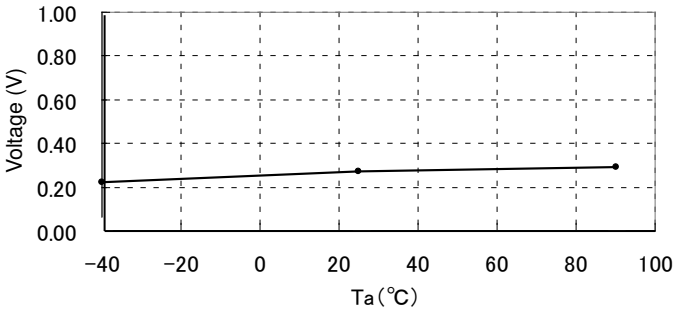


ZCD Voltage Clamp vs. Temperature

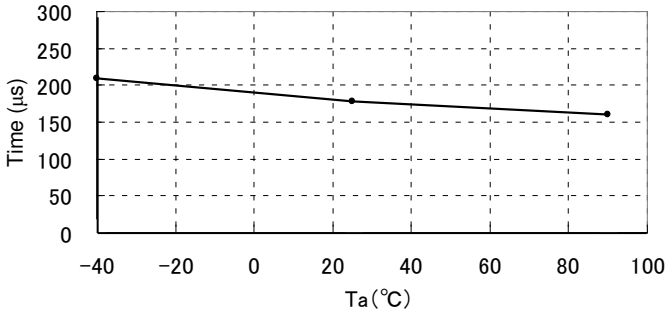
Upper side



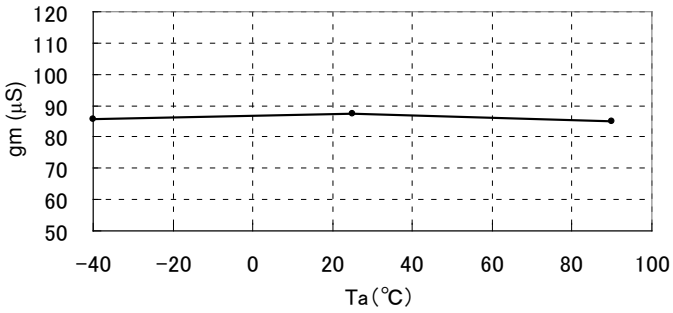
Lower side



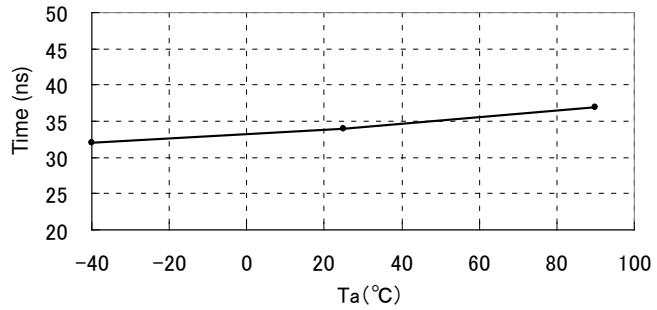
Timer1 Restart Time vs. Temperature



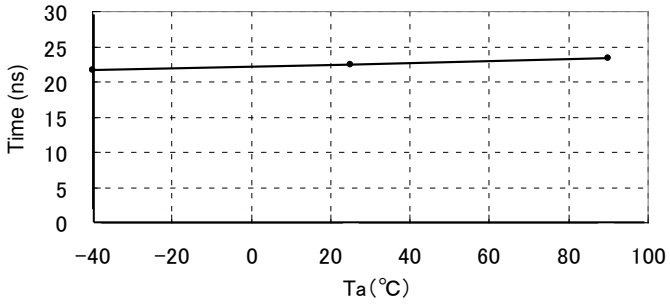
Error Amplifier Conductance vs. Temperature



Gate-Drive Output Pulse on time vs. Temperature

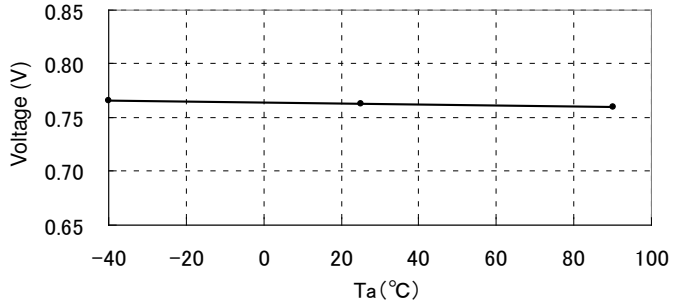


Gate-Drive Output Pulse off time vs. Temperature

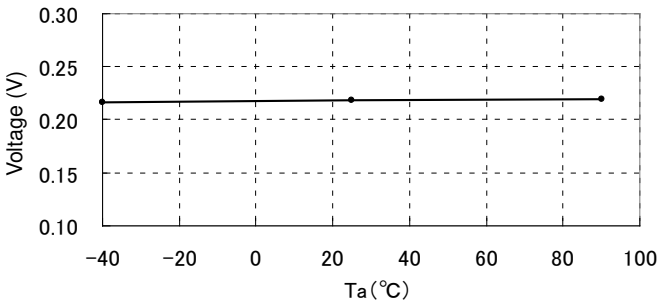


Brown out threshold Voltage vs. Temperature

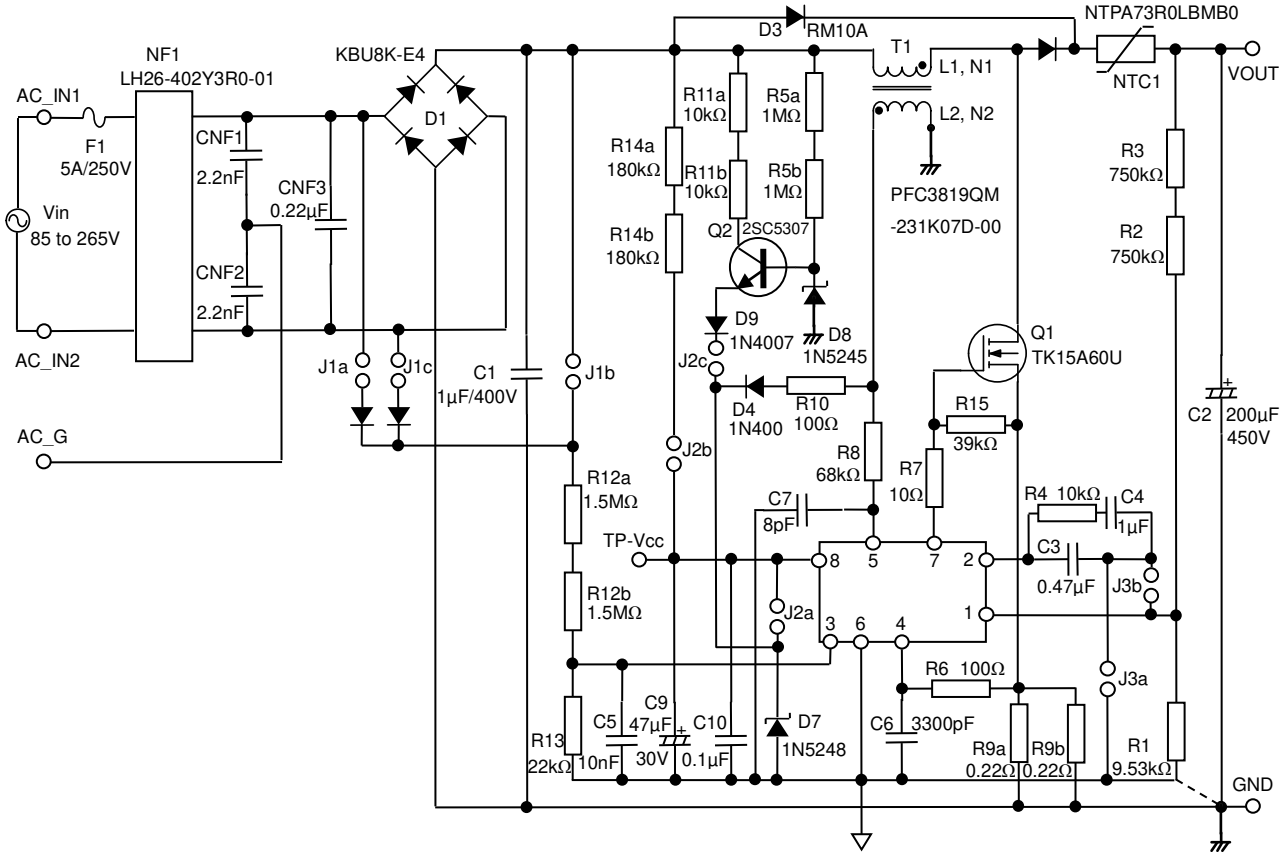
Start up



Hysteresis (shutdown) Voltage vs. Temperature



Applications Information



This chapter provides the minimum description including equations and constants as a guide to understand the TB6819AFG demonstration board. These equations and constants should be optimized according to the specifications of actual applications. Please adjust them according to the specifications to achieve required operation. At the same time, make sure that no problem occurs in the various tests, such as end-product, environmental and durability tests. This application circuit is for 400 V - 200 W output.

(1) L1 Inductance

Since the TB6819AFG operates in CRM mode, the switching frequency fs (Hz) depends on the L1 inductance and input/output conditions.

$$L1 = \frac{(Vo - \sqrt{2} \times Vin\ (min)) \times \eta \times Vin\ (min)^2}{2 \times 100 \times fs \times Vo \times Po}$$

Where Vin (min) (V) is the minimum AC input voltage (effective value), Vo (V) is the output DC voltage, Po (W) is the output power and η (%) is the power efficiency.

The fs value should be within the range between the value sufficiently higher than the audible frequency limit of 20 kHz and 150 kHz, above which an EMI problem can occur. In this application, fs is targeted to be 50 kHz. The power efficiency η is assumed to be about 90%, which is not greatly different from that of actual use. The AC input voltage range is assumed to be between 85V and 265 V. Thus, the minimum value Vin (min) is expected to be 85 V, and the output power Vo is 400 V. Given that Po = 200 W, L1 can be calculated as 227 µH. In this application, a commercially available inductor of 230 µH is used.

(2) Auxiliary Winding L2

The auxiliary winding L2 is used to detect the zero inductor current condition of the inductor L1. L2 is also used for delivering a supply voltage to the TB6819AFG.

Since the maximum (positive-going) reference voltage for the ZCD comparator is 1.9 V, N1/N2 should meet the following condition to properly perform zero current detection using the auxiliary winding L2:

$$N1 / N2 < (Vo - \sqrt{2} \times Vin\ (max)) / 1.9 = 14$$

Where N1 is the number of winding turns of L1, N2 is that of L2 and Vin (max) (V) is the maximum AC input voltage (265 V).

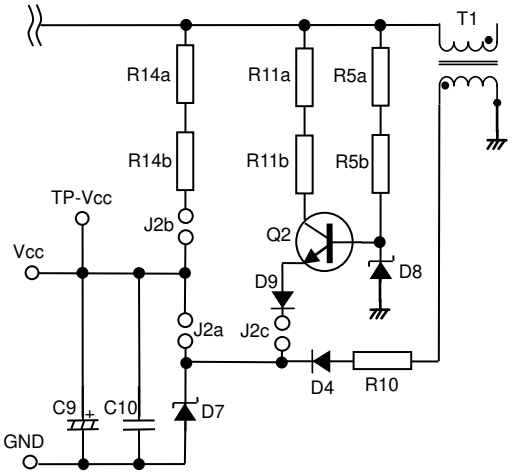
To ensure that the design requirements are met, N1/N2 should preferably be about 10 to allow for design margins.

To deliver a supply voltage to the TB6819AFG by using the auxiliary winding L2, N1 / N2 should meet the following condition:

$$Vo / Vcc (max) < N1 / N2 < Vo / Vcc (min)$$

Where Vcc (max) is the maximum IC supply voltage and Vcc (min) is its minimum value.
To achieve the supply voltage range of 10 to 25 V by only using L2 while obtaining Vo = 400 V on the L1 side, N1 / N2 can be calculated as: 400 / 25 < N1 / N2 < 400 / 10. That is, N1 / N2 should be within the range from 16 to 40. However, an inductor of N1 / N2 = 10 is used to achieve proper IC operation. Therefore, an external circuit is required to step down the supply voltage so that it is within the proper range and also for its stabilization.

In this application, external circuitry for obtaining the IC supply voltage from the auxiliary winding L2 can be configured in one of the following two ways. These two circuits are different in the block for starting up the IC, while remaining the same in the block for voltage step-down and stabilization.



1. Using a startup resistor for starting up the TB6819AFG

Close jumpers J2a and J2b and open J2c. R14a and R14b are the startup resistors and Vcc is supplied through R10 and D4 from the auxiliary winding after the TB6819AFG is started up. The upper limit of Vcc is determined by D7, which is 18V in this application. This circuit is not stable at light load. It is necessary to take care when using a circuit of this type.

2. Using a constant-current circuit for starting up the TB6819AFG

Close jumpers J2a and J2c and open J2b. This setup achieves stable operation at start-up by using a transistor Q2 instead of using a startup resistor for configuring a constant-current circuit. The base potential of Q2 is determined by a Zener diode D8, which is 15V in this application. This constant-current circuit is only used for starting up the TB6819AFG. Thus, it should be ensured that the D9 output potential does not exceed the D7 Zener voltage of 18V. The following relationship should be satisfied between the voltages:

$$Vcc (min) < D9 \text{ output voltage} < D7 \text{ Zener voltage} < Vcc (max)$$

To supply Vcc externally, jumpers J2a, J2b and J2c should all be open and supply voltage from TP-Vcc. At this time, the IC ground pin should be connected to the nearest ground pattern, such as an anode pin of D7 and ground-side terminals of C9 and C10.

In the event of unexpected faults such as short-circuits between adjacent pins, a large current may abruptly flow, damaging the TB6819AFG. This damage can be severe if a short circuit occurs between Vcc (pin 8) and POUT (pin 7) or between GND (pin 6) and POUT (pin 7). Therefore, the maximum possible current flowing to the Vcc pin should be restricted to the minimum extent required for the application.

(3) Multiplier Input Circuit

Circuitry for applying a sine wave signal of the AC input supply voltage to the multiplier can be configured in one of the following ways.

1. Dividing a full-wave rectified voltage waveform

Close jumper J1b and open J1a and J1c.

2. Dividing a voltage waveform prior to full-wave rectification

Close jumpers J1a and J1c and open J1b.

Considering that the IC startup threshold voltages of the BOP function = 0.75V, the rated voltage of the IC = 5 V and the MULT linear input voltage range of the multiplier = 0 to 3.0 V, the R12a, R12b and R13 resistor values should satisfy the following condition:

$$0.75\ V < 85\ V \times \sqrt{2} \times R13 / (R12a + R12b + R13)\ (= 0.875\ V)$$

$$265\ V \times \sqrt{2} \times R13 / (R12a + R12b + R13)\ (= 2.728\ V) < 3.0\ V\ (5\ V)$$

In this application, resistors of the following values are used: R12a = R12b = 1.5 MΩ, R13 = 22 kΩ.

(4) Output Voltage Feedback Circuit

When the DC output voltage is resistively divided and applied to the error amplifier, the R1, R2 and R3 resistor values should satisfy the following equation:

$$Vo \times R1 / (R1 + R2 + R3) = 2.51\ V$$

Where Vo (V) is the output voltage and the error amplifier reference voltage = 2.51 V.

Substituting Vo = 400 V, R2 = R3 = 750 kΩ provides R1 = 9.47 kΩ. In this application however, a resistor of 9.53 kΩ, which is available in the E96 series, is used as R1.

(5) Current Detection Circuit

Iq1, which is the current that flows through an external transistor Q1, is converted into voltage by using a current detection resistor R9, then applied to the IS pin (pin 4). The peak voltage of the IS comparator reference voltage while voltage of Vin (min) is applied is Visp (min), which can be calculated as:

$$0.65 \times Vin\ (min) \times \sqrt{2} \times R13 / (R12a + R12b + R13) = 0.57\ V$$

The maximum current of the Q1 current, Iq1 (max) is limited to Visp (min) / R9.

$$Iq1\ (max) = Visp\ (min) / R9 = 0.57 / R9$$

This current should allow the output power Po to be large enough. Therefore, the following equation should be satisfied:

$$Po \times 100 / \eta = Vin\ (min) \times \sqrt{2} \times Iq1\ (rms)$$

where Iq1 (rms) is the effective value of Iq1.

When Po = 200 W, Vin (min) = 85 V, the power efficiency η = 90%, and also Iq1 (max) = 2 × √2 × Iq1 (rms) considering the CRM current waveform, the above equation can be rewritten as:

$$Iq1\ (max) = Po \times 100 \times 2 \times \sqrt{2} / (\eta \times Vin\ (min) \times \sqrt{2}) = 5.23\ A$$

$$R9 = 0.57 / Iq1\ (max) = 0.11\ \Omega$$

In this application, resistors of 0.22 Ω, R9a and R9b, are connected in parallel.

(6) Zero-Current Detection Circuit

The auxiliary winding L2 is connected to the ZCD pin. At this time, the current through L2 is limited to 3mA, which is the rated current at the ZCD pin, or less by using the current limiting resistor R8. The following relationship should be satisfied depending on whether the external FET is on or off:

$$FET = On: R8 > Vin\ (max) \times \sqrt{2} \times N2 / N1 / 3\ mA = 12.5\ k\Omega$$

$$FET = Off: R8 > Vo \times N2 / N1 / 3mA = 13.3\ k\Omega$$

A resistor of 68 kΩ is used in this application for limiting the current to 1/5 of the rated current.

(7) Output Capacitor

The output capacitance C2 is determined so that the PFC output ripple voltage does not exceed the output overvoltage detection threshold. Since the output voltage ripple is derived from a full-wave rectified input voltage waveform, it contains frequency components of twice the AC input frequency. When Vr is the effective value of ripple voltage, the following equation can be approximately formulated:

$$C2 = Po / (2 \times 2\pi f \times Vr \times Vo)$$

Considering the condition of $\sqrt{2}Vr \leq Vo \times (V_{OVP-2} / Verr-1)$, the above equation can be rewritten as:

$$C2 \geq Po / (\sqrt{2} \times 2\pi f \times Vo^2 \times (V_{OVP-2} / Verr-1))$$

Substituting f = 50 Hz, V_{OVP-2} = 2.63 V (min) and Verr = 2.46 V (min), the following can be obtained:

$$C2 \geq 41\ \mu F$$

A capacitor of 200 μF is used as C2 in this application.

(8) Input Capacitor

An input capacitor C1 for the PFC should be capable of supplying energy stored in the L1 inductor while the FET is on. Since the on/off duty cycle of the FET is about 50%, the C1 capacitor should be temporarily able to supply twice the current. Also, a current reaches its maximum when the AC input voltage is the minimum. Thus, the following relationship should be satisfied:

$$2 \times 1 / 2 \times L1 \times (Po / Vin\ (min))^2 \leq 1 / 2 \times C1 \times Vin\ (min)^2$$

, which can be rewritten as:

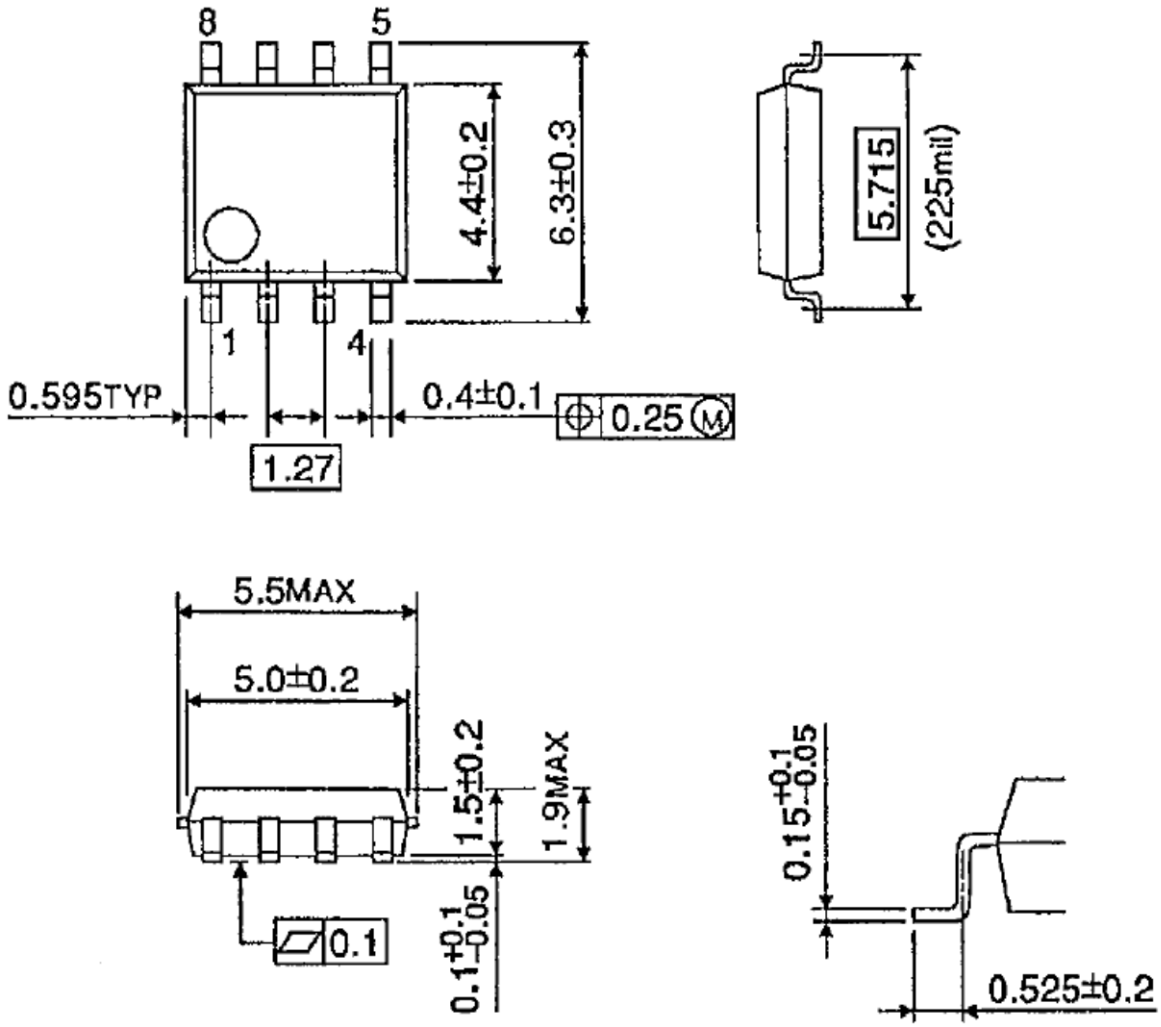
$$C1 \geq 2 \times L1 \times Po^2 / Vin\ (min)^4 = 0.35\ \mu F$$

A capacitor of 1μF is used as C1 in this application.

Package Dimensions

1. SOP8-P-225-1.27
TB6819AFG (O*)

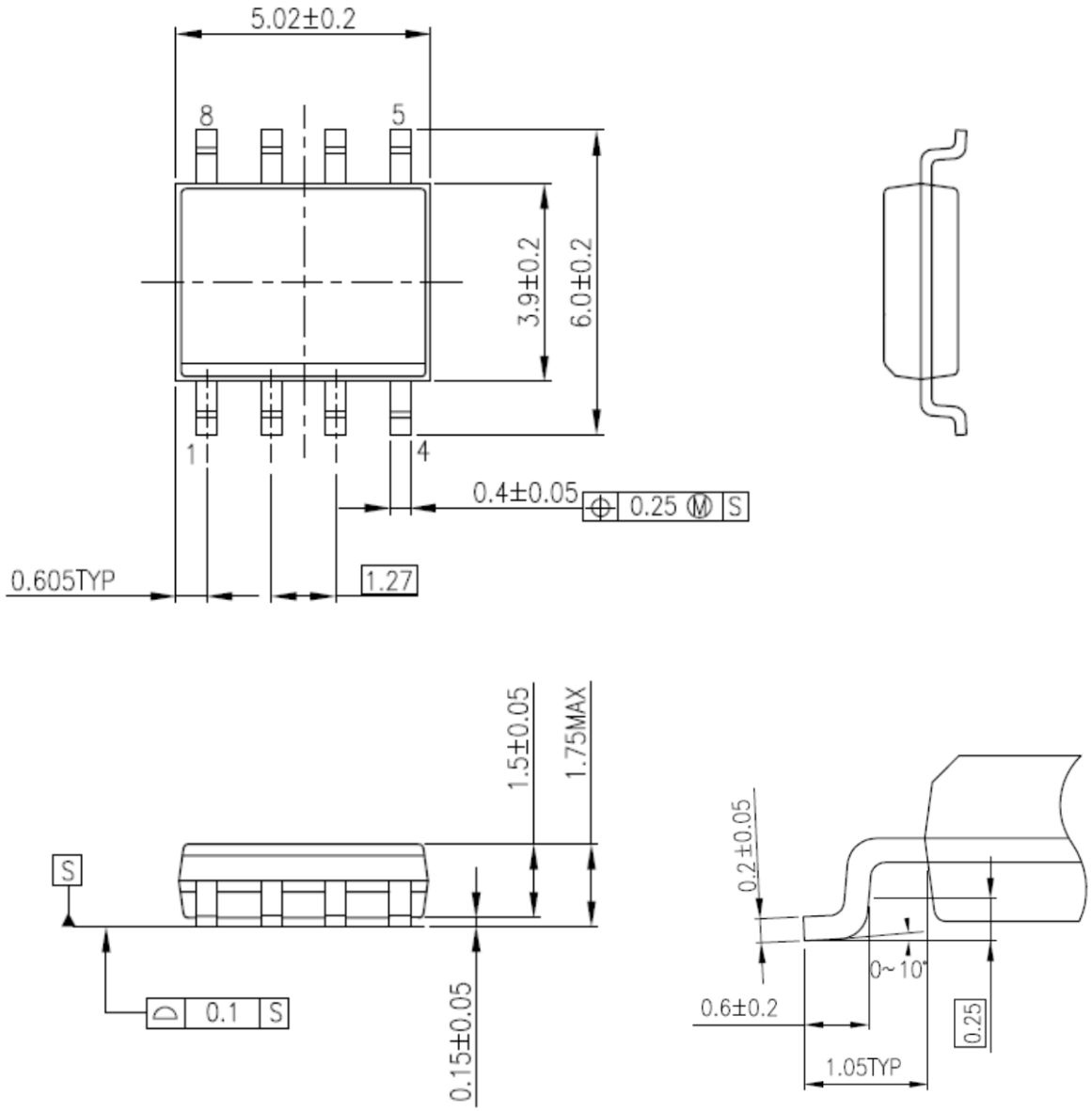
Unit: mm



Weight: 0.1 g (typ.)

2. P-SOP8-0406-1.27-001
TB6819AFG (Z*)

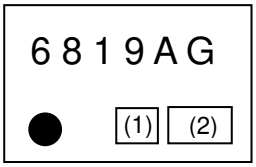
Unit: mm



Weight: 0.1 g (typ.)

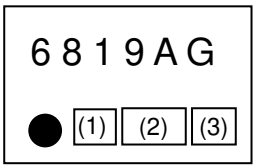
Marking

1. SOP8-P-225-1.27
TB6819AFG (O*)



Lot Code
(1)Production year mark (One character shown in the digit at the end of production year)
(2)Production week mark (Two characters shown in the production week, up to week 53)

2. P-SOP8-0406-1.27-001
TB6819AFG (Z*)



Lot Code
(1)Production year mark (One character shown in the digit at the end of production year)
(2)Production week mark (Two characters shown in the production week, up to week 53)
(3)Production lot mark (One character shown in 1-9, and A-Z except for the “I”, “O”, “Q”)

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