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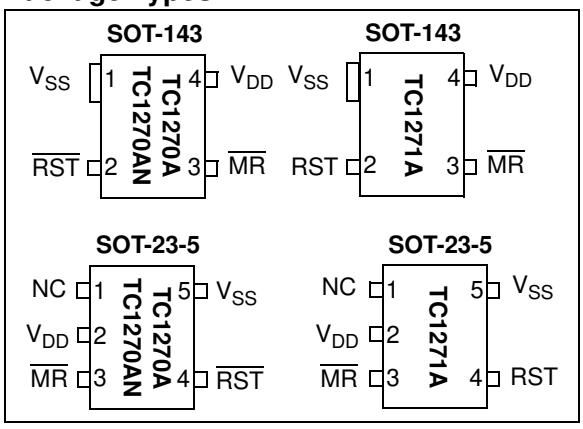
TC1270A/70AN/71A

Voltage Supervisor with Manual Reset Input

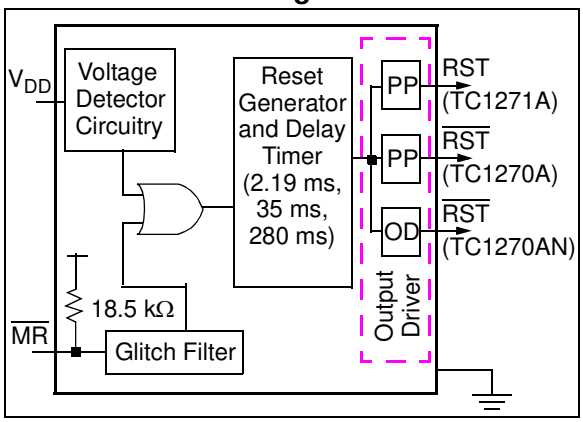
Features:

- Precision Voltage Monitor
  - 2.63V, 2.93V, 3.08V, 4.38V and 4.63V Trip Points (Typical)
- Manual Reset Input
- Reset Time-Out Delay:
  - Standard: 280 ms (Typical)
  - Optional: 2.19 ms, and 35 ms (Typical)
- Power Consumption ≤ 15 µA max
- No glitches on outputs during power-up
- Active Low Output Options:
  - Push-Pull Output and Open-Drain Output
- Active High Output Option:
  - Push-Pull Output
- Replacement for (Specification compatible with):
  - TC1270, TC1271
  - TCM811, TCM812
- Fully Static Design
- Low-Voltage Operation (1.0V)
- ESD Protection:
  - ≥ 4 kV Human Body Model (HBM)
  - ≥ 400V Machine Model (MM)
- Extended (E) Temperature Range:
  -40°C to +125°C
- Package Options:
  - 4-Lead SOT-143
  - 5-Lead SOT-23
  - Pb-free Device

Package Types



Functional Block Diagram



Device Features

Device	Output		Reset Delay (ms) (Typ)(3)	Reset Trip Point (V)(3)	Voltage Range (V)	Temperature Range	Packages	Comment
	Type	Active Level						
TC1270A	Push-Pull	Low	2.19, 35, 280(1)	4.63, 4.38, 3.08, 2.93, 2.63(4)	1.0V to 5.5V	-40°C to +125°C	SOT-143(2), SOT-23-5	Replaces TC1270 and TCM811
TC1270AN	Open-Drain	Low					SOT-143(2), SOT-23-5	New Option
TC1271A	Push-Pull	High					SOT-143(2), SOT-23-5	Replaces TC1271 and TCM812

Note 1: The 280 ms Reset delay time-out is compatible with the TC1270, TC1271, TCM811 and TCM812 devices.
2: The SOT-143 package is compatible with the TC1270, TC1271, TCM811 and TCM812 devices.
3: Custom Reset trip points and Reset delays available, contact your local Microchip sales office.
4: The TC1270/1 and TCM811/12 1.75V trip point option is not supported.

NOTES:

1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

Supply Voltage (V_{DD} to V_{SS}) ..... +7.0V
Input Current, V_{DD} ..... 10 mA
Output Current, $\overline{RESET}$, Reset ..... 10 mA
Voltage on all inputs and outputs
w.r.t. V_{SS} ..... -0.6V to (V_{DD} + 1.0V)
Storage Temperature Range ..... -65°C to +150°C
Operating Temperature Range ..... -40°C to +125°C
Maximum Junction Temperature, T_S ..... 150°C
ESD protection on all pins
Human Body Model ..... ≥ 4 kV
Machine Model ..... ≥ 400V

† Notice: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to a device. The absolute maximum values are merely stress ratings – functional operation of a device at those, or any other conditions above those indicated in the operational listing of these specifications, is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

Electrical Characteristics: Unless otherwise noted, V_{DD} = 5V for L/M versions, V_{DD} = 3.3V for T/S versions, V_{DD} = 3V for R version, T_A = -40°C to +125°C. Typical values are at T_A = +25°C.

Parameter	Sym	Min	Typ(1)	Max	Units	Test Conditions
Operating Voltage Range	V_{DD}	1.0	—	5.5	V	
Supply Current	I_{DD}	—	7	15	µA	$V_{DD} > V_{TRIP}$, for L/M/R/S/T, V_{DD} = 5.5V
		—	4.75	10	µA	$V_{DD} > V_{TRIP}$, for R/S/T, V_{DD} = 3.6V
		—	10	15	µA	$V_{DD} < V_{TRIP}$, for L/M/R/S/T
Reset Trip Point Threshold (3)	V_{TRIP}	4.54	4.63	4.72	V	TC127xAL: T_A = +25°C
		4.50	—	4.75	V	T_A = –40°C to +125°C
		4.30	4.38	4.46	V	TC127xAM: T_A = +25°C
		4.25	—	4.50	V	T_A = –40°C to +125°C
		3.03	3.08	3.14	V	TC127xAT: T_A = +25°C
		3.00	—	3.15	V	T_A = –40°C to +125°C
		2.88	2.93	2.98	V	TC127xAS: T_A = +25°C
		2.85	—	3.00	V	T_A = –40°C to +125°C
		2.72	2.77	2.82	V	TC127xA:(5) T_A = +25°C
		2.70	—	2.85	V	T_A = –40°C to +125°C
		2.58	2.63	2.68	V	TC127xAR: T_A = +25°C
		2.55	—	2.70	V	T_A = –40°C to +125°C

Note 1: Data in the Typical ("Typ") column is at 5V, +25°C, unless otherwise stated.
2: $\overline{RST}$ output for TC1270A and TC1270AN, RST output for TC1271A.
3: TC127XA refers to the TC1270A, TC1270AN or TC1271A device.
4: Hysteresis is within the $V_{TRIP(MIN)}$ to $V_{TRIP(MAX)}$ window.
5: Custom-ordered voltage trip point. Minimum order volume requirement.
6: This specification allows this device to be used in PIC® microcontroller applications that require the In-Circuit Serial Programming™ (ICSP™) feature (see device-specific programming specifications for voltage requirements). The total time that the RST pin can be above the maximum device operational voltage (5.5V) is 100s. Current into the RST pin should be limited to 2 mA. It is recommended that the device operational temperature be maintained between 0°C to +70°C (+25°C preferred). For additional information, refer to Figure 2-41.

ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical Characteristics: Unless otherwise noted, V_{DD} = 5V for L/M versions, V_{DD} = 3.3V for T/S versions, V_{DD} = 3V for R version, T_A = -40°C to +125°C. Typical values are at T_A = +25°C.

Parameter		Sym	Min	Typ(1)	Max	Units	Test Conditions
Reset Threshold Tempco			—	±30	—	ppm/°C	
Reset Trip Point Hysteresis (1)		V_{HYS}	—	0.3	—	%	Percentage of V_{TRIP} Voltage
$\overline{MR}$ Input High Threshold		V_{IH}	2.3	—	—	V	$V_{DD} > V_{TRIP(MAX)}$, L/M only
			0.7 V_{DD}	—	—	V	$V_{DD} > V_{TRIP(MAX)}$, R/S/T only
$\overline{MR}$ Input Low Threshold		V_{IL}	—	—	0.8	V	$V_{DD} > V_{TRIP(MAX)}$, L/M only
			—	—	0.25 V_{DD}	V	$V_{DD} > V_{TRIP(MAX)}$, R/S/T only
$\overline{MR}$ Pull-up Resistance			10	18.5	40	kΩ	
Open-Drain High Voltage on Output		V_{ODH}	—	—	13.5	V	Open-Drain Output pin only. V_{DD} = 3.0V, Time voltage > 5.5 applied ≤ 100s. Current into pin limited to 2 mA +25°C operation recommended (6)
Reset Output Voltage Low (2)	TC1270A/ TC1270AN	V_{OL}	—	—	0.3	V	R/S/T only, I_{SINK} = 1.2 mA, $V_{DD} = V_{TRIP(MIN)}$
	TC1271A		—	—	0.3	V	R/S/T only, I_{SINK} = 1.2 mA, $V_{DD} = V_{TRIP(MAX)}$
	TC1270A/ TC1270AN		—	—	0.4	V	L/M only, I_{SINK} = 3.2 mA, $V_{DD} = V_{TRIP(MIN)}$
	TC1271A		—	—	0.3	V	L/M only, I_{SINK} = 3.2 mA, $V_{DD} = V_{TRIP(MAX)}$
	TC1270A/ TC1270AN		—	—	0.3	V	L/M only, I_{SINK} = 50 µA, V_{DD} > 1.0V
Reset Output Voltage High (2)	TC1270A	V_{OH}	0.8 V_{DD}	—	—	V	R/S/T only, I_{SOURCE} = 500 µA, $V_{DD} = V_{TRIP(MAX)}$
	TC1270A		V_{DD} - 1.5	—	—	V	L/M only, I_{SOURCE} = 800 µA, $V_{DD} = V_{TRIP(MAX)}$
	TC1271A		0.8 V_{DD}	—	—	V	I_{SOURCE} = 500 µA, $V_{DD} \le V_{TRIP(MIN)}$
Input Leakage Current		I_{IL}	—	—	±1	µA	$V_{PIN} = V_{DD}$
Open-Drain $\overline{RST}$ Output Leakage		I_{OLOD}	—	—	1	µA	Open-Drain configuration only.
Capacitive Loading Specification on Output Pins		C_{IO}	—	—	50	pF	

Note 1: Data in the Typical ("Typ") column is at 5V, +25°C, unless otherwise stated.

2: $\overline{RST}$ output for TC1270A and TC1270AN, RST output for TC1271A.

3: TC127XA refers to the TC1270A, TC1270AN or TC1271A device.

4: Hysteresis is within the $V_{TRIP(MIN)}$ to $V_{TRIP(MAX)}$ window.

5: Custom-ordered voltage trip point. Minimum order volume requirement.

6: This specification allows this device to be used in PIC® microcontroller applications that require the In-Circuit Serial Programming™ (ICSP™) feature (see device-specific programming specifications for voltage requirements). The total time that the RST pin can be above the maximum device operational voltage (5.5V) is 100s. Current into the RST pin should be limited to 2 mA. It is recommended that the device operational temperature be maintained between 0°C to +70°C (+25°C preferred). For additional information, refer to Figure 2-41.

1.1 AC CHARACTERISTICS

1.1.1 TIMING PARAMETER SYMBOLOGY

The timing parameter symbols have been created following one of the following formats:

1. TppS2ppS

T	
F	Frequency
E	Error

2. TppS

T	Time

Lowercase letters (pp) and their meanings:

pp	
io	Input or Output pin
rx	Receive
bitclk	RX/TX BITCLK
drt	Device Reset Timer
osc	Oscillator
tx	Transmit
RST	Reset

Uppercase letters and their meanings:

S	
F	Fall
H	High
I	Invalid (High-impedance)
L	Low
P	Period
R	Rise
V	Valid
Z	High-impedance

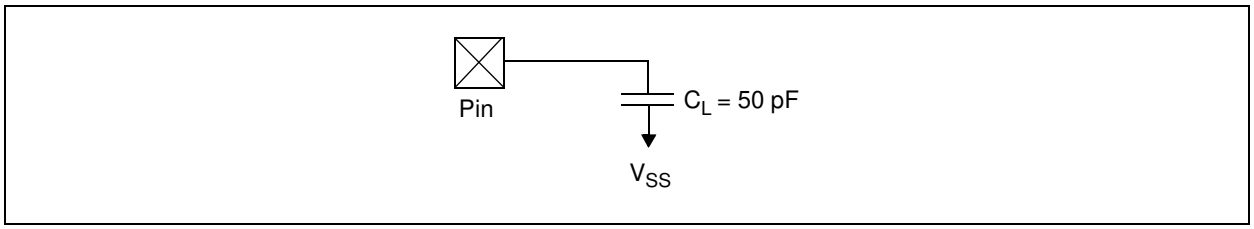
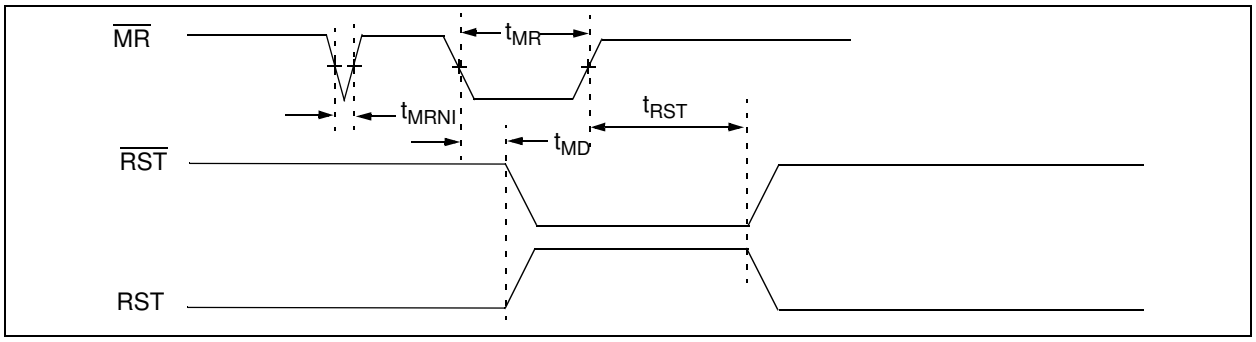


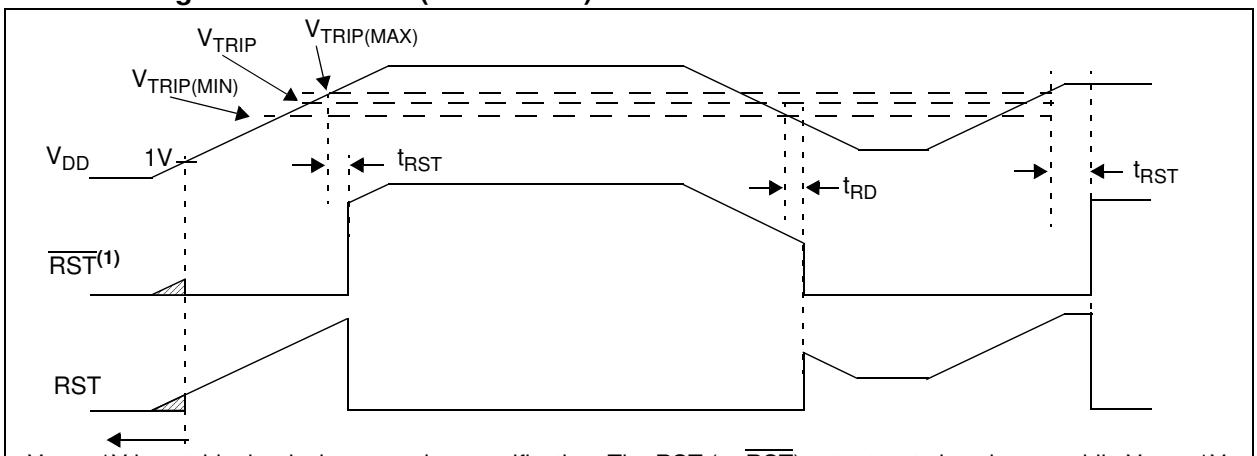
FIGURE 1-1: *Test Load Conditions.*

TIMING DIAGRAMS AND SPECIFICATIONS

$\overline{MR}$ Pin and Reset Pin Waveform



Device Voltage and Reset Pin (Active Low) Waveform



V_{DD} < 1V is outside the device operating specification. The RST (or $\overline{RST}$) output state is unknown while V_{DD} < 1V.

Note 1: The TC1270AN requires an external pull-up resistor.

$\overline{Reset}$ and Device Reset Timer Requirements

Electrical Characteristics: Unless otherwise noted, V_{DD} = 5V for L/M versions, V_{DD} = 3.3V for T/S versions, V_{DD} = 3V for R version, T_A = -40°C to +125°C. Typical values are at T_A = +25°C.

Parameter		Sym	Min	Typ(1)	Max	Units	Test Conditions
V_{DD} to Reset Delay		t_{RD}	—	50	—	µs	$V_{DD} = V_{TRIP(MAX)}$ to $V_{TRIP(MIN)}$ –125 mV
Reset Active Time Out Period	TC127XAx**B**Vyy(3)	t_{RST}	1.09	2.19	4.38	ms	$V_{DD} = V_{TRIP(MAX)}$
	TC127XAx**A**Vyy(3)		17.5	35	70	ms	$V_{DD} = V_{TRIP(MAX)}$
	TC127XAxVyy(3)		140	280	560	ms	$V_{DD} = V_{TRIP(MAX)}$
$\overline{MR}$ Minimum Pulse Width		t_{MR}	10	—	—	µs	
$\overline{MR}$ Noise Immunity		t_{MRNI}	—	0.1	—	µs	
$\overline{MR}$ to Reset Propagation Delay		t_{MD}	—	0.2	—	µs	

Note 1: Unless otherwise stated, data in the Typical ("Typ") column is at 5V, +25°C.

2: $\overline{RST}$ output for TC1270A, RST output for TC1271A.

3: TC127XA refers to the TC1270A, TC1270AN or TC1271A device. "x" indicates the selected voltage trip point, while "yy" indicates the package code.

TEMPERATURE CHARACTERISTICS

Electrical Specifications: Unless otherwise indicated, V_{DD} = +1.0V to +5.5V, V_{SS} = GND.						
Parameters	**Sym**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
Temperature Ranges						
Specified Temperature Range	T_A	-40	—	+125	°C	
Operating Temperature Range	T_A	-40	—	+125	°C	
Storage Temperature Range	T_A	-65	—	+150	°C	
Thermal Package Resistances						
Thermal Resistance, 5L-SOT-23	θ_{JA}	—	256	—	°C/W	
Thermal Resistance, 4L-SOT-143	θ_{JA}	—	426	—	°C/W	

NOTES:

2.0 TYPICAL PERFORMANCE CURVES

Note: The graphs and tables that follow this note are the result of a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

Note: Unless otherwise indicated, all limits are specified for V_{DD} = 1V to 5.5V, T_A = –40°C to +125°C.

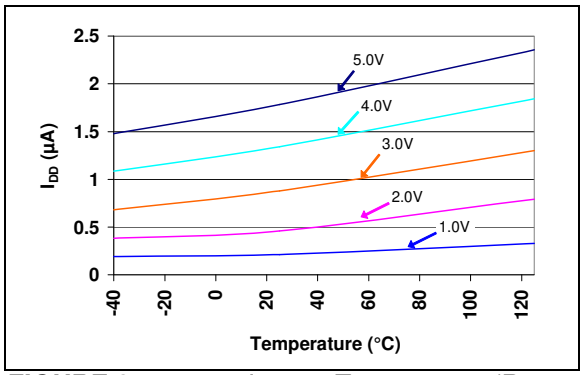


FIGURE 2-1: *I_{DD} vs. Temperature (Reset Power-up Timer Inactive) (TC1270AL, TC1270ANL, TC1271AL - 4.50V min./4.63V typ./4.75V max.).*

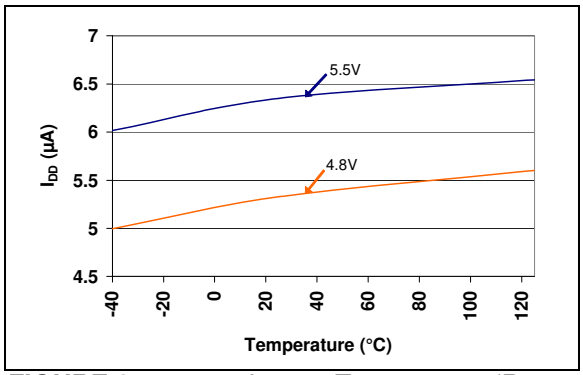


FIGURE 2-4: *I_{DD} vs. Temperature (Reset Power-up Timer Active) (TC1270AL, TC1270ANL, TC1271AL - 4.50V min./4.63V typ./4.75V max.).*

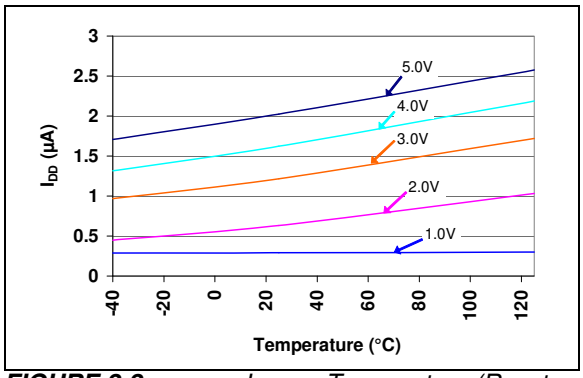


FIGURE 2-2: *I_{DD} vs. Temperature (Reset Power-up Timer Inactive) (TC1270AT, TC1270ANT, TC1271AT - 3.00V min./3.08V typ./3.15V max.).*

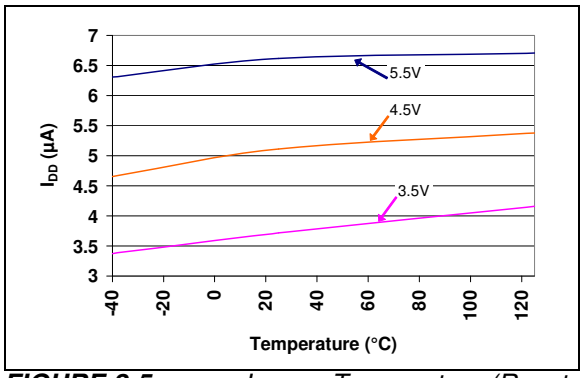


FIGURE 2-5: *I_{DD} vs. Temperature (Reset Power-up Timer Active) (TC1270AT, TC1270ANT, TC1271AT - 3.00V min./3.08V typ./3.15V max.).*

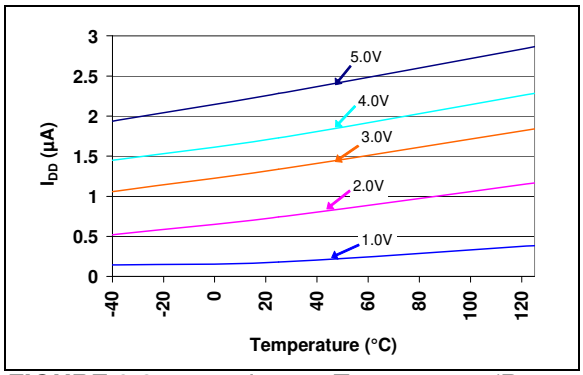


FIGURE 2-3: *I_{DD} vs. Temperature (Reset Power-up Timer Inactive) (TC1270AR, TC1270ANR, TC1271AR - 2.55V min./2.63V typ./2.70V max.).*

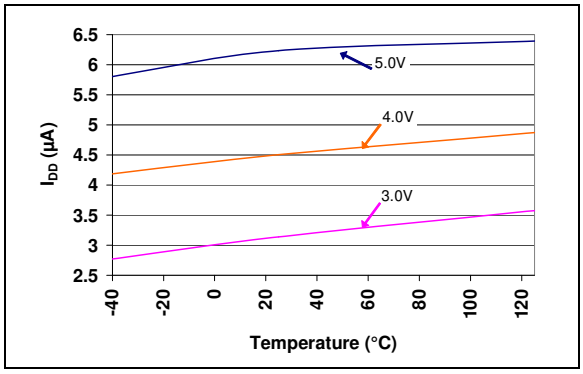


FIGURE 2-6: *I_{DD} vs. Temperature (Reset Power-up Timer Active) (TC1270AR, TC1270ANR, TC1271AR - 2.55V min./2.63V typ./2.70V max.).*

Note: Unless otherwise indicated, all limits are specified for V_{DD} = 1V to 5.5V, T_A = –40°C to +125°C.

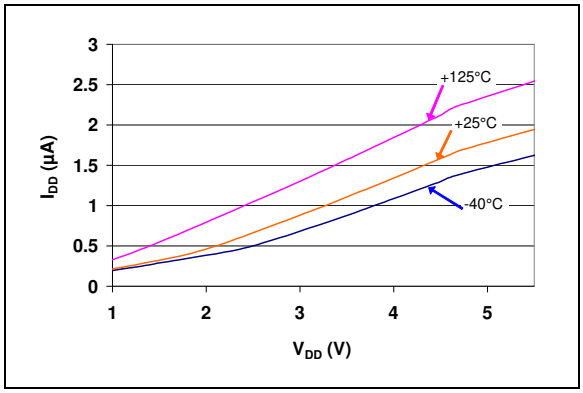


FIGURE 2-7: *I_{DD} vs. V_{DD} (Reset Power-up Timer Inactive) (TC1270AL, TC1270ANL, TC1271AL - 4.50V min./4.63V typ./4.75V max.).*

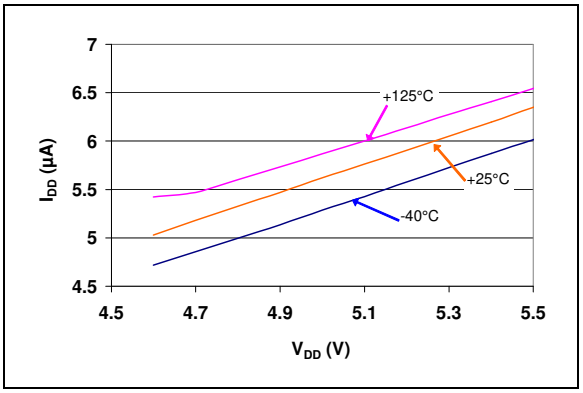


FIGURE 2-10: *I_{DD} vs. V_{DD} (Reset Power-up Timer Active) (TC1270AL, TC1270ANL, TC1271AL - 4.50V min./4.63V typ./4.75V max.).*

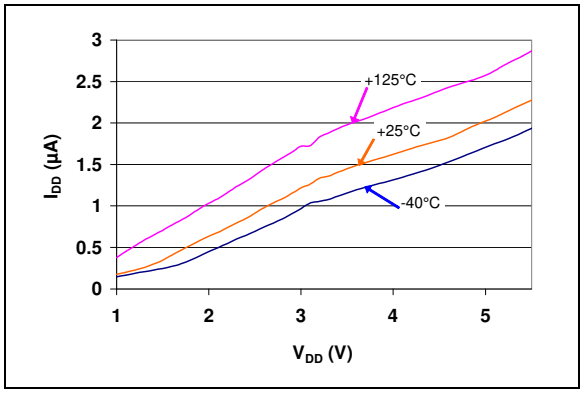


FIGURE 2-8: *I_{DD} vs. V_{DD} (Reset Power-up Timer Inactive) (TC1270AT, TC1270ANT, TC1271AT - 3.00V min./3.08V typ./3.15V max.).*

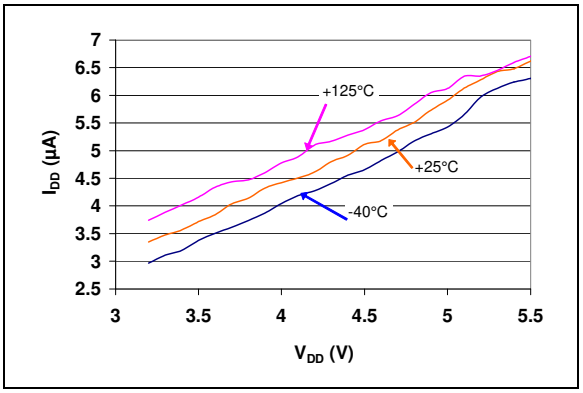


FIGURE 2-11: *I_{DD} vs. V_{DD} (Reset Power-up Timer Active) (TC1270AT, TC1270ANT, TC1271AT - 3.00V min./3.08V typ./3.15V max.).*

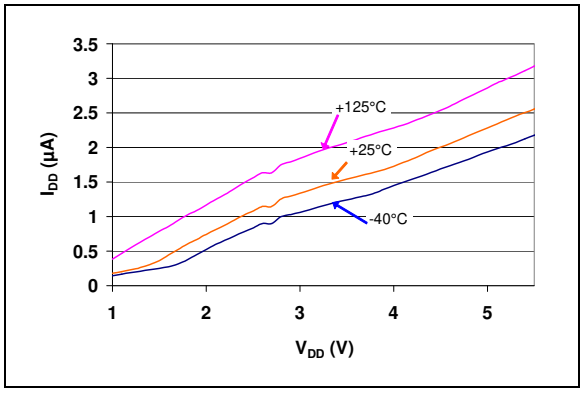


FIGURE 2-9: *I_{DD} vs. V_{DD} (Reset Power-up Timer Inactive) (TC1270AR, TC1270ANR, TC1271AR - 2.55V min./2.63V typ./2.70V max.).*

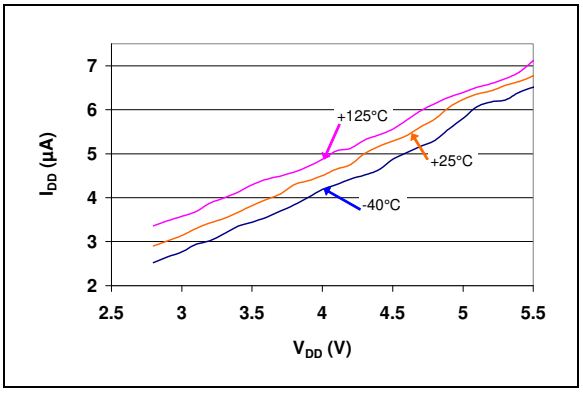


FIGURE 2-12: *I_{DD} vs. V_{DD} (Reset Power-up Timer Active) (TC1270AR, TC1270ANR, TC1271AR - 2.55V min./2.63V typ./2.70V max.).*

Note: Unless otherwise indicated, all limits are specified for V_{DD} = 1V to 5.5V, T_A = –40°C to +125°C.

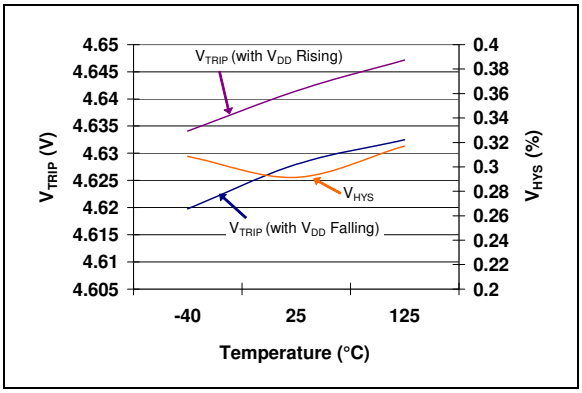


FIGURE 2-13: *V_{TRIP} and V_{HYS} vs. Temperature (TC1270AL, TC1270ANL, TC1271AL - 4.50V min./4.63V typ./4.75V max.).*

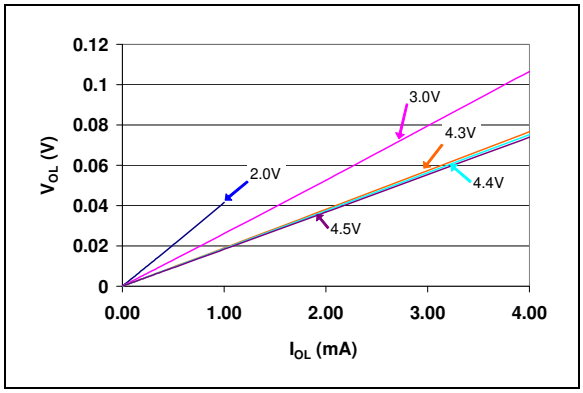


FIGURE 2-16: *V_{OL} vs. I_{OL} (TC1270AL, TC1270ANL, TC1271AL - 4.50V min./4.63V typ./4.75V max.).*

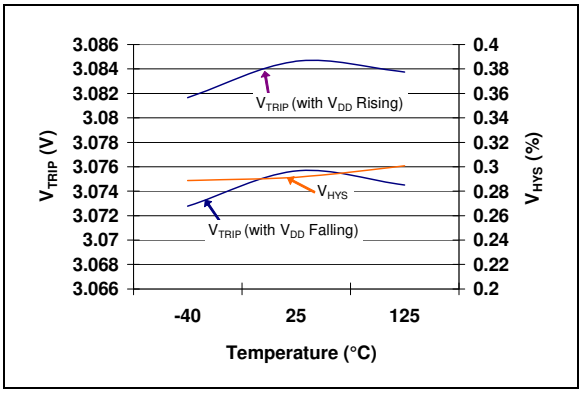


FIGURE 2-14: *V_{TRIP} and V_{HYS} vs. Temperature (TC1270AT, TC1270ANT, TC1271AT - 3.00V min./3.08V typ./3.15V max.).*

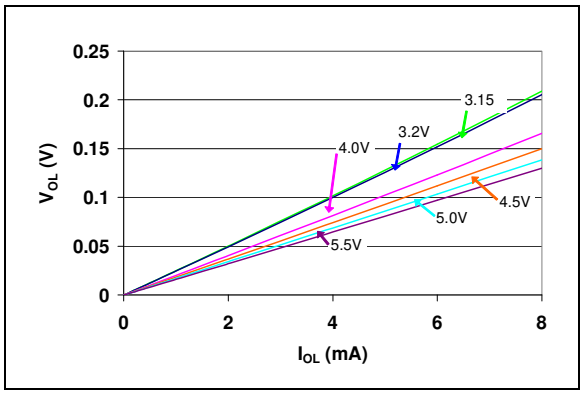


FIGURE 2-17: *V_{OL} vs. I_{OL} (TC1270AT, TC1270ANT, TC1271AT - 3.00V min./3.08V typ./3.15V max.).*

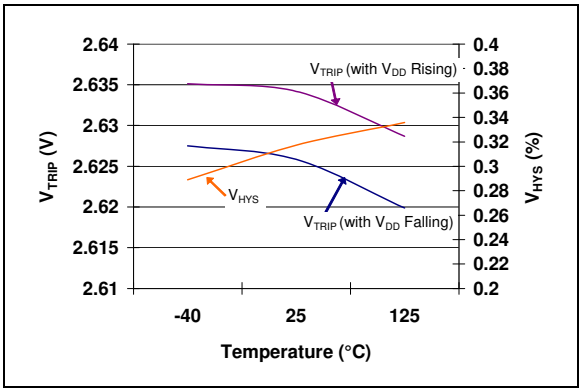


FIGURE 2-15: *V_{TRIP} and V_{HYST} vs. Temperature (TC1270AR, TC1270ANR, TC1271AR - 2.55V min./2.63V typ./2.70V max.).*

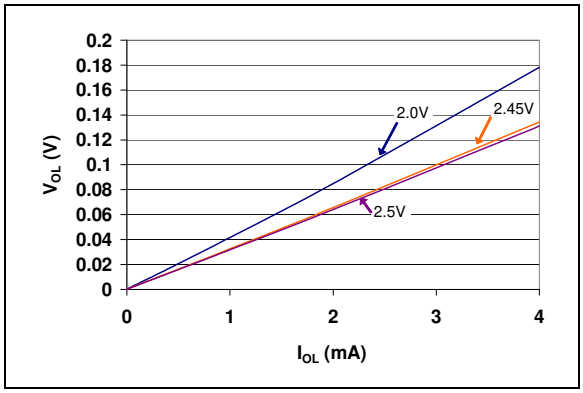


FIGURE 2-18: *V_{OL} vs. I_{OL} (TC1270AR, TC1270ANR, TC1271AR - 2.55V min./2.63V typ./2.70V max.).*

Note: Unless otherwise indicated, all limits are specified for V_{DD} = 1V to 5.5V, T_A = –40°C to +125°C.

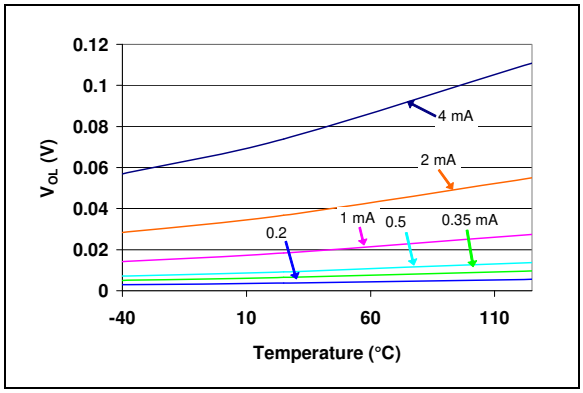


FIGURE 2-19: *V_{OL} vs. Temperature (TC1270AL, TC1270ANL, TC1271AL - 4.50V min./4.63V typ./4.75V max.). @ V_{DD} = 4.5V).*

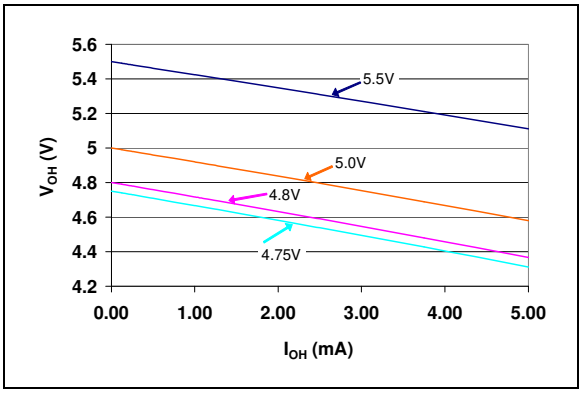


FIGURE 2-22: *V_{OH} vs. I_{OL} (TC1270AL, TC1270ANL, TC1271AL - 4.50V min./4.63V typ./4.75V max.) @ +25°C).*

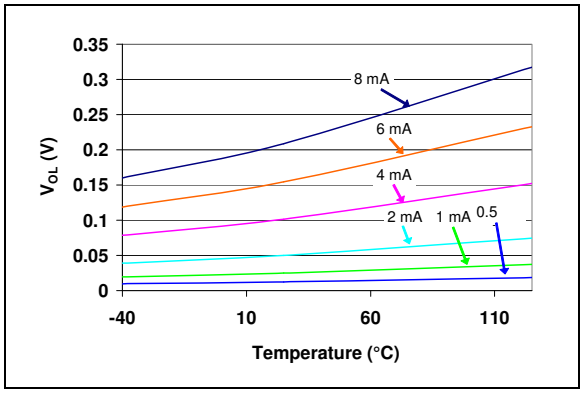


FIGURE 2-20: *V_{OL} vs. Temperature (TC1270AT, TC1270ANT, TC1271AT - 3.00V min./3.08V typ./3.15V max.). @ V_{DD} = 2.7V).*

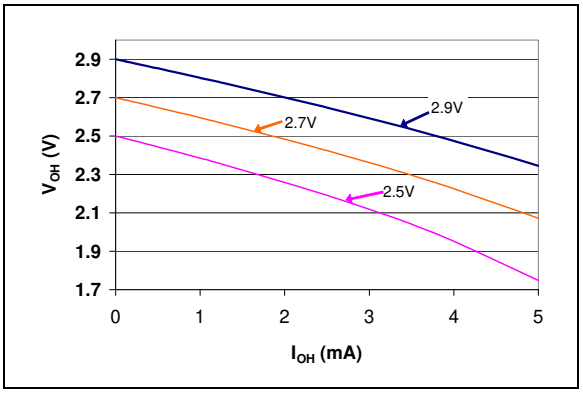


FIGURE 2-23: *V_{OH} vs. I_{OH} (TC1270AT, TC1270ANT, TC1271AT - 3.00V min./3.08V typ./3.15V max.) @ +25°C).*

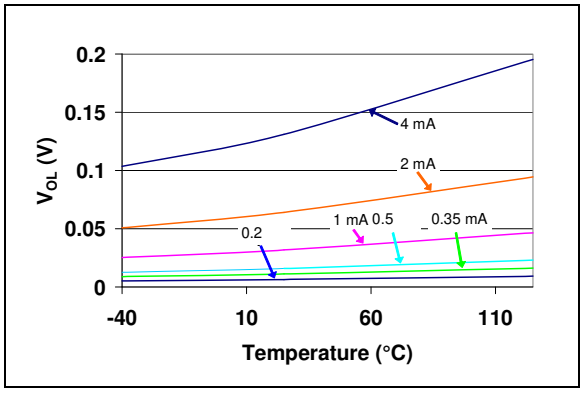


FIGURE 2-21: *V_{OL} vs. Temperature (TC1270AR, TC1270ANR, TC1271AR - 2.55V min./2.63V typ./2.70V max.). @ V_{DD} = 1.8V).*

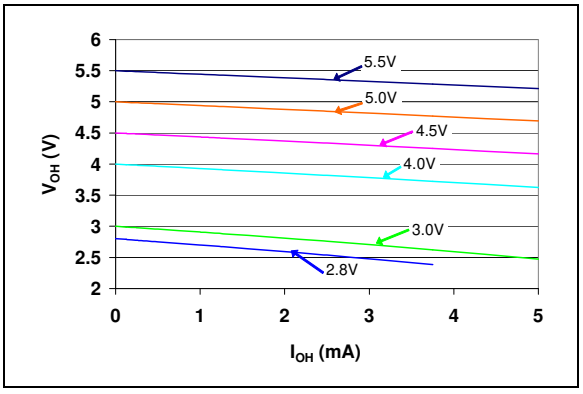


FIGURE 2-24: *V_{OH} vs. I_{OH} (TC1270AR, TC1270ANR, TC1271AR - 2.55V min./2.63V typ./2.70V max.) @ +25°C).*

Note: Unless otherwise indicated, all limits are specified for V_{DD} = 1V to 5.5V, T_A = –40°C to +125°C.

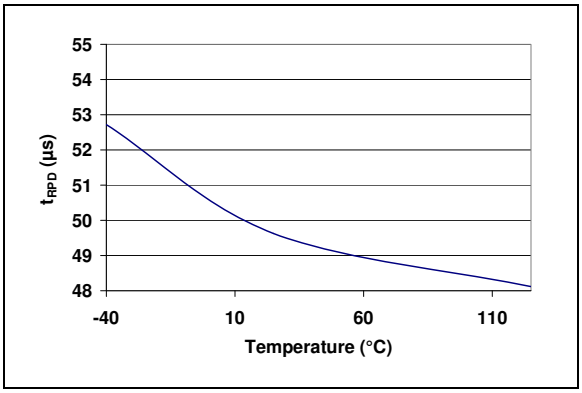


FIGURE 2-25: *V_{DD} Falling to Reset Propagation Delay (t_{RPD}) vs. Temperature (TC1270AL, TC1270ANL, TC1271AL - 4.50V min./4.63V typ./4.75V max.).*

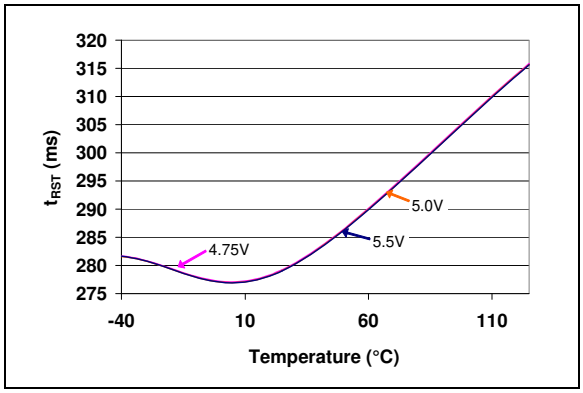


FIGURE 2-28: *Reset Time-Out Period (t_{RST}) vs. Temperature (TC1270AL, TC1270ANL, TC1271AL - 4.50V min./4.63V typ./4.75V max.).*

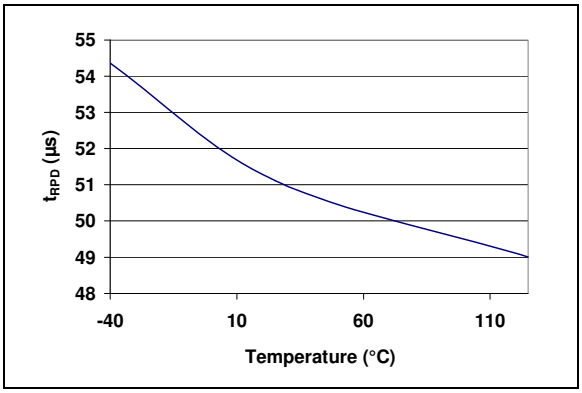


FIGURE 2-26: *V_{DD} Falling to Reset Propagation Delay (t_{RPD}) vs. Temperature (TC1270AT, TC1270ANT, TC1271AT - 3.00V min./3.08V typ./3.15V max.).*

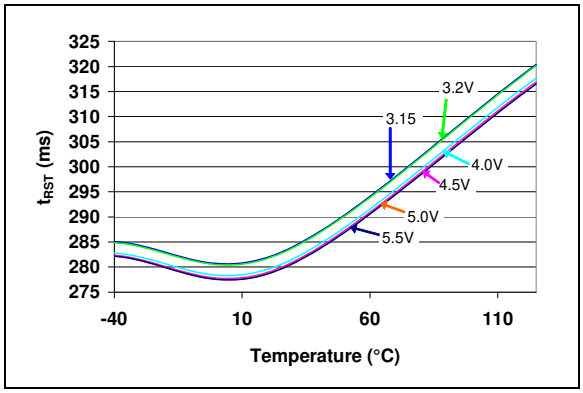


FIGURE 2-29: *Reset Time-Out Period (t_{RST}) vs. Temperature (TC1270AT, TC1270ANT, TC1271AT - 3.00V min./3.08V typ./3.15V max.).*

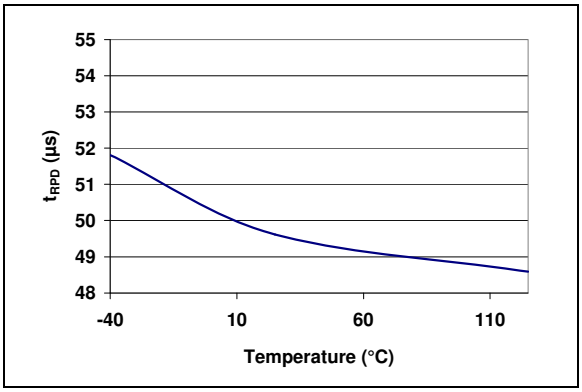


FIGURE 2-27: *V_{DD} Falling to Reset Propagation Delay (t_{RPD}) vs. Temperature (TC1270AR, TC1270ANR, TC1271AR - 2.55V min./2.63V typ./2.70V max.).*

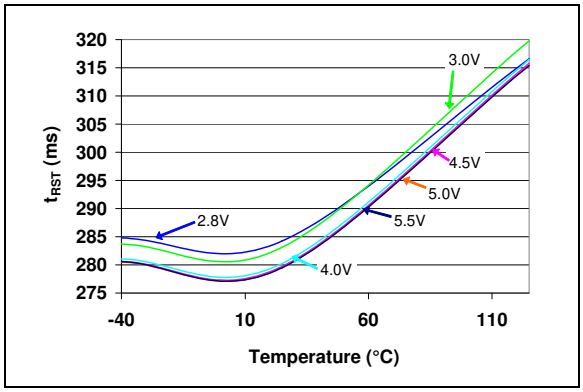


FIGURE 2-30: *Reset Time-Out Period (t_{RST}) vs. Temperature (TC1270AR, TC1270ANR, TC1271AR - 2.55V min./2.63V typ./2.70V max.).*

Note: Unless otherwise indicated, all limits are specified for V_{DD} = 1V to 5.5V, T_A = –40°C to +125°C.

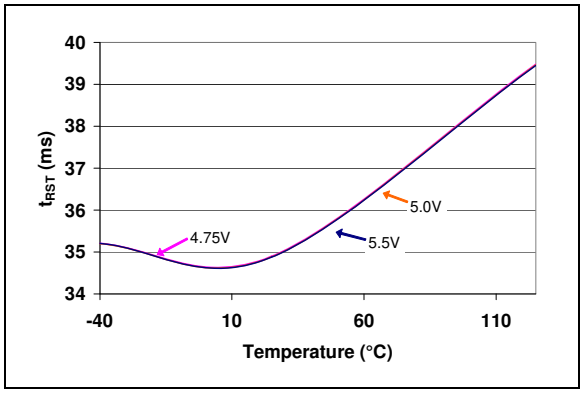


FIGURE 2-31: *Reset Time-Out Period (t_{RST}) (C time out option) vs. Temperature (TC1270AL, TC1270ANL, TC1271AL - 4.50V min./4.63V typ./4.75V max.).*

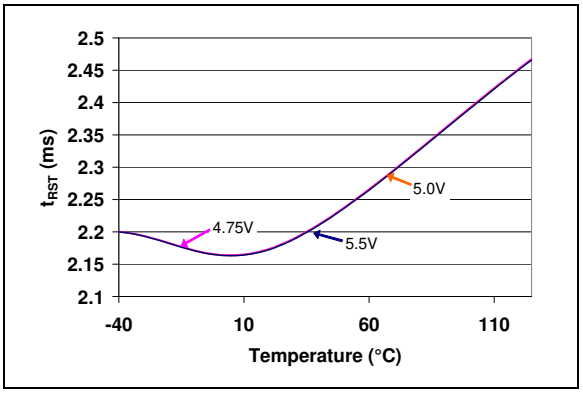


FIGURE 2-34: *Reset Time-Out Period (t_{RST}) (B time out option) vs. Temperature (TC1270AL, TC1270ANL, TC1271AL - 4.50V min./4.63V typ./4.75V max.).*

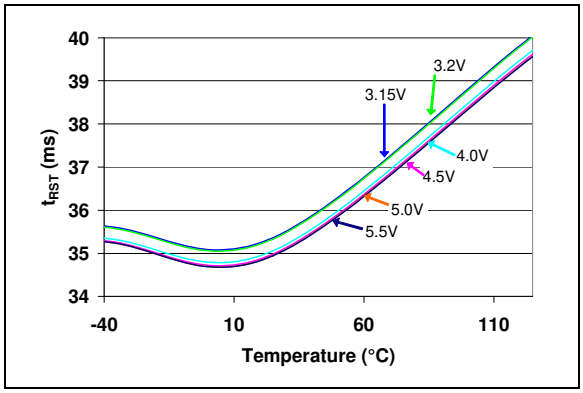


FIGURE 2-32: *Reset Time-Out Period (t_{RST}) (C time out option) vs. Temperature (TC1270AT, TC1270ANT, TC1271AT - 3.00V min./3.08V typ./3.15V max.).*

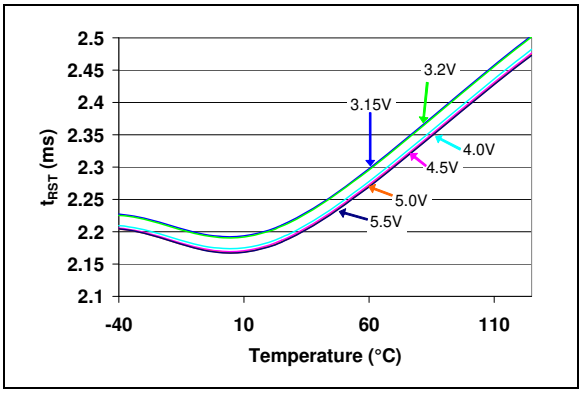


FIGURE 2-35: *Reset Time-Out Period (t_{RST}) (B time out option) vs. Temperature (TC1270AT, TC1270ANT, TC1271AT - 3.00V min./3.08V typ./3.15V max.).*

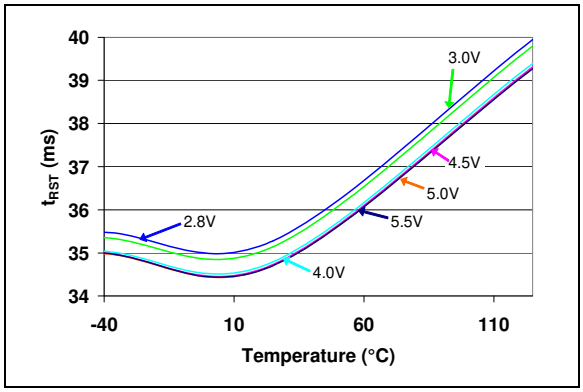


FIGURE 2-33: *Reset Time-Out Period (t_{RST}) (C time out option) vs. Temperature (TC1270AR, TC1270ANR, TC1271AR - 2.55V min./2.63V typ./2.70V max.).*

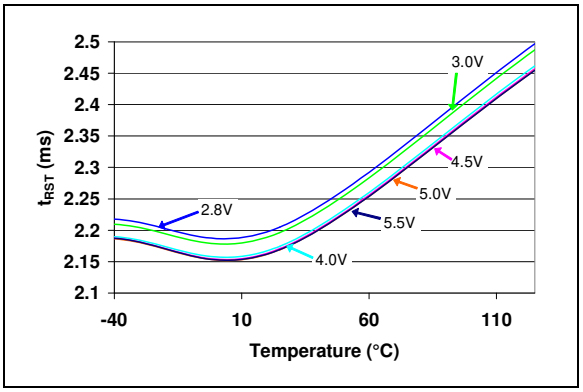


FIGURE 2-36: *Reset Time-Out Period (t_{RST}) (B time out option) vs. Temperature (TC1270AR, TC1270ANR, TC1271AR - 2.55V min./2.63V typ./2.70V max.).*

Note: Unless otherwise indicated, all limits are specified for V_{DD} = 1V to 5.5V, T_A = –40°C to +125°C.

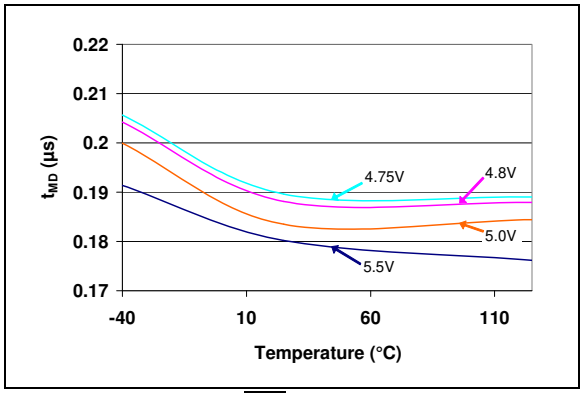


FIGURE 2-37: *$\overline{MR}$ Low to Reset Propagation Delay (t_{MD}) vs. Temperature (TC1270AL, TC1270ANL, TC1271AL - 4.50V min./4.63V typ./4.75V max.).*

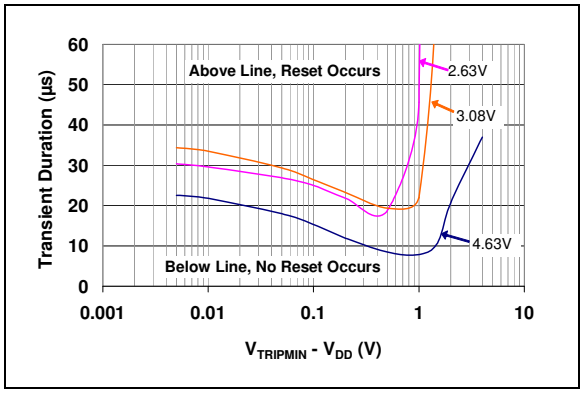


FIGURE 2-40: *V_{DD} Transient Duration vs. Reset Threshold Overdrive (V_{TRIP} (minimum) - V_{DD}).*

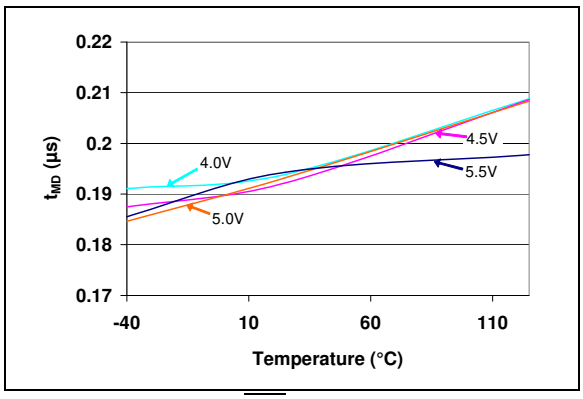


FIGURE 2-38: *$\overline{MR}$ Low to Reset Propagation Delay (t_{MD}) vs. Temperature (TC1270AT, TC1270ANT, TC1271AT - 3.00V min./3.08V typ./3.15V max.).*

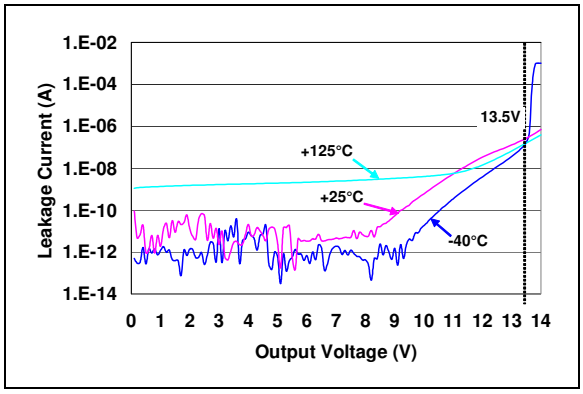


FIGURE 2-41: *Open-Drain Leakage Current vs. Voltage Applied to $\overline{RST}$ Pin (TC1270AR, TC1270ANR, TC1271AR - 2.55V minimum).*

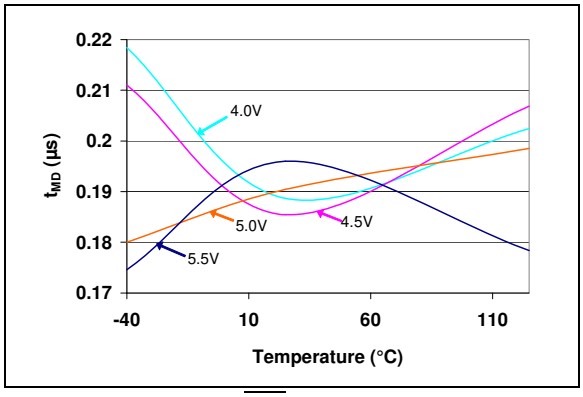


FIGURE 2-39: *$\overline{MR}$ Low to Reset Propagation Delay (t_{MD}) vs. Temperature (TC1270AR, TC1270ANR, TC1271AR - 2.55V min./2.63V typ./2.70V max.).*

NOTES:

3.0 PIN DESCRIPTIONS

Descriptions of the pins are listed in Table 3-1.

TABLE 3-1: PINOUT DESCRIPTION

Pin Number						Sym	Pin		Standard Function
TC1270A (Push-Pull, active-low)		TC1270AN (Open-Drain, active-low)		TC1271A (Push-Pull, active-high)					
SOT-23-5	SOT-143-4	SOT-23-5	SOT-143-4	SOT-23-5	SOT-143-4		Type	Buffer / Driver	
5	1		1	5	1	V_{SS}	—	Power	Ground
4	2	—	—	—	—	$\overline{RST}$	O	Push-Pull	Reset output (Push-Pull), active-low H = V_{DD} > V_{TRIP}, Reset pin is inactive (after Reset Delay Timer completes) L = V_{DD} < V_{TRIP}, Reset pin is active Goes active (Low) if one of these conditions occurs: 1. If V_{DD} falls below the selected Reset voltage threshold. 2. If the $\overline{MR}$ pin is forced low. 3. During power-up.
—	—	4	2	—	—	$\overline{RST}$	O	Open-Drain	Reset output (Open-Drain), active-low Float = V_{DD} > V_{TRIP}, Reset pin is inactive (after Reset Delay Timer completes) L = V_{DD} < V_{TRIP}, Reset pin is active Goes active (Low) if one of these conditions occurs: 1. If V_{DD} falls below the selected Reset voltage threshold. 2. If the $\overline{MR}$ pin is forced low. 3. During power-up.
—	—	—	—	4	2	RST	O	Push-Pull	Reset output (Push-Pull), active-high H = V_{DD} < V_{TRIP}, Reset pin is active L = V_{DD} > V_{TRIP}, Reset pin is inactive (after Reset Delay Timer completes) Goes active (High) if one of these conditions occurs: 1. If V_{DD} falls below the selected Reset voltage threshold. 2. If the $\overline{MR}$ pin is forced low. 3. During power-up.

Note 1: The $\overline{MR}$ pin has an internal weak pull-up (18.5 kΩ typical).

TABLE 3-1: PINOUT DESCRIPTION (CONTINUED)

Pin Number						Sym	Pin		Standard Function
TC1270A (Push-Pull, active-low)		TC1270AN (Open-Drain, active-low)		TC1271A (Push-Pull, active-high)					
SOT-23-5	SOT-143-4	SOT-23-5	SOT-143-4	SOT-23-5	SOT-143-4		Type	Buffer / Driver	
3	3	3	3	3	3	$\overline{MR}$	I	ST[1]	Manual Reset Input Pin This input allows a push button switch to be directly connected to a TC1270A/70AN/71A device's $\overline{MR}$ pin, which can be used to force a system Reset. The input filter ignores noise pulses that occur on the $\overline{MR}$ pin. H = Switch is open (internal pull-up resistor pulls signal high). State of the RST/$\overline{RST}$ pin is determined by other system conditions. L = Switch is depressed (shorted to ground). This forces the RST/$\overline{RST}$ pin Active.
2	4	2	4	2	4	V_{DD}	—	Power	Supply Voltage
1	—	1	—	1	—	NC	—	—	No Connection

Note 1: The $\overline{MR}$ pin has an internal weak pull-up (18.5 kΩ typical).

3.1 Ground Terminal (V_{SS})

V_{SS} provides the negative reference for the analog input voltage. Typically, the circuit ground is used.

3.2 Supply Voltage (V_{DD})

V_{DD} can be used for power supply monitoring or a voltage level that requires monitoring.

3.3 Reset Output (RST and $\overline{RST}$)

There are three types of Reset output pins. These are:

1. Push-Pull active-low Reset
2. Push-Pull active-high Reset
3. Open-Drain active-low Reset, external pull-up resistor required.

3.3.1 ACTIVE-LOW ($\overline{RST}$) – PUSH-PULL

The $\overline{RST}$ push-pull output remains low while V_{DD} is below the Reset voltage threshold (V_{TRIP}). The time that the $\overline{RST}$ pin is held low after the device voltage (V_{DD}) returns to a high level (> V_{TRIP}) is typically 280 ms. After the Reset Delay Timer expires, the $\overline{RST}$ pin will be driven to the high state.

3.3.2 ACTIVE-HIGH (RST) – PUSH-PULL

The RST push-pull output remains high while V_{DD} is below the Reset voltage threshold (V_{TRIP}). The time that the RST pin is held high after the device voltage (V_{DD}) returns to a high level (> V_{TRIP}) is typically 280 ms. After the Reset Delay Timer expires, the RST pin will be driven to the low state.

3.3.3 ACTIVE-LOW ($\overline{RST}$) – OPEN-DRAIN

The $\overline{RST}$ open-drain output remains low while V_{DD} is below the Reset voltage threshold (V_{TRIP}). The time that the $\overline{RST}$ pin is held low after the device voltage (V_{DD}) returns to a high level (> V_{TRIP}) depends on the Reset time-out selected. After the Reset Delay Timer expires, the $\overline{RST}$ pin will float.

3.4 Manual Reset Input ($\overline{MR}$)

The Manual Reset ($\overline{MR}$) input pin allows a push button switch to easily be connected to the system. When the push button is depressed, it forces a system Reset. This pin has circuitry that filters noise that may be present on the $\overline{MR}$ signal.

The $\overline{MR}$ pin is active-low and has an internal pull-up resistor.

4.0 DEVICE OPERATION

4.1 General Description

For many of today's microcontroller applications, care must be taken to prevent low-power conditions that can cause many different system problems. The most common causes are brown-out conditions, where the system supply drops below the operating level momentarily. The second most common cause is when a slowly decaying power supply causes the microcontroller to begin executing instructions without sufficient voltage to sustain volatile memory (RAM), thus producing indeterminate results.

The TC127XA family (TC1270A, TC1270AN and TC1271A) are cost-effective voltage supervisor devices designed to keep a microcontroller in Reset until the system voltage has reached and stabilized at the proper level for reliable system operation. These devices also operate as protection from brown-out conditions when the system supply voltage drops below a safe operating level.

A Manual Reset input ($\overline{MR}$ pin) is provided. This allows a push button switch to be directly connected to the TC127XA device, and is suitable for use as a push button Reset. This allows the system to easily be reset from the external control of the push button switch. No external components are required.

The Reset pin (RST or $\overline{RST}$) will be forced active, if any of the following occur:

- During device power-up
- V_{DD} goes below the device threshold voltage
- The Manual Reset input ($\overline{MR}$) goes low

Figure 4-1 shows a high level block diagram of the devices. The device can be described with three functional blocks. These are:

- Voltage detect circuit
- Manual Reset with glitch filter circuit
- Reset generator circuit

The Reset generator circuit controls the Reset delay time of the Reset output signal.

There are three Reset Delay Timer options. Depending on the option, the Reset signal ($\overline{RST}$/RST pin) will be held active for a minimum of 1.09 ms, 17.5 ms, or 140 ms.

The TC1271A has an active-high RST output while the TC1270A and TC1270AN have an active-low $\overline{RST}$ output.

The TC1270A and TC1271A have a push-pull output driver, while the TC1270AN has an open-drain output.

Figure 4-2 shows a typical circuit for a push-pull device and Figure 4-3 shows a typical circuit for an open-drain device.

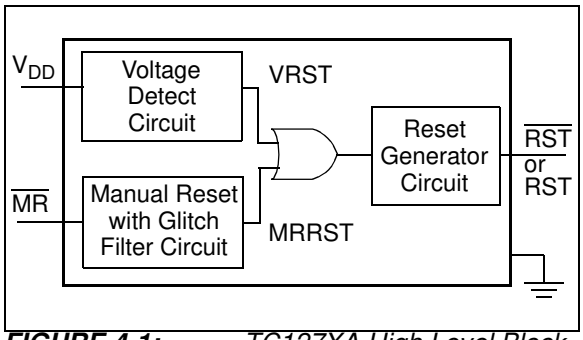


FIGURE 4-1: *TC127XA High Level Block Diagram.*

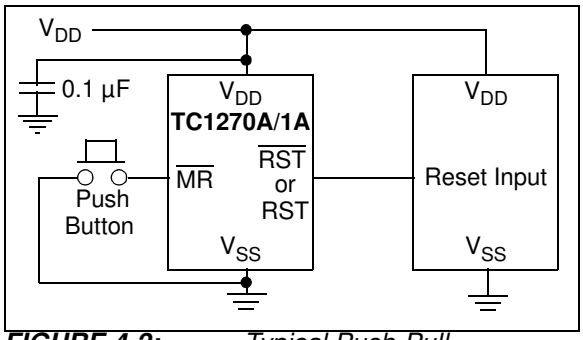


FIGURE 4-2: *Typical Push-Pull Application Circuit.*

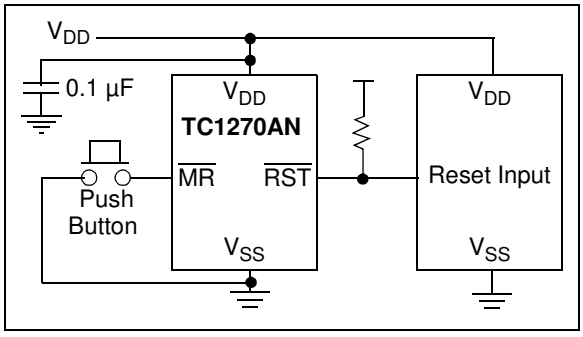


FIGURE 4-3: *Typical Open-Drain Application Circuit.*

The TC1270A and TC1271A devices are available in a 4-Pin SOT-143 package (to maintain footprint compatibility with the TC1270, TC1271, TCM811 and TCM812 devices) and a SOT-23-5 package. The TC1270AN is only available in the SOT-23-5 package.

Low supply current makes these devices suitable for battery-powered applications.

Device specific block diagrams are presented in Figure 4-4 through Figure 4-6.

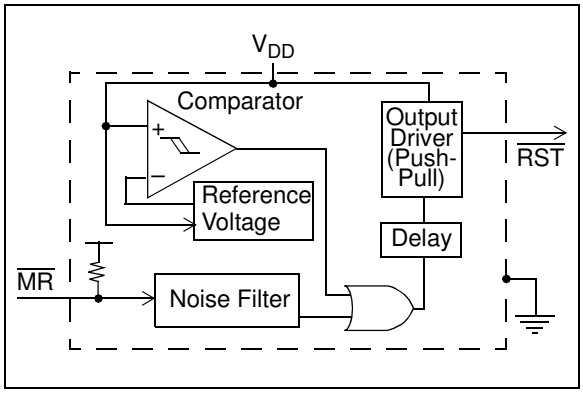


FIGURE 4-4: *TC1270A Block Diagram.*

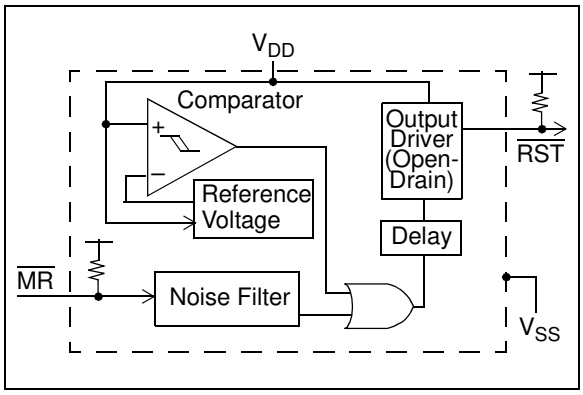


FIGURE 4-5: *TC1270AN Block Diagram.*

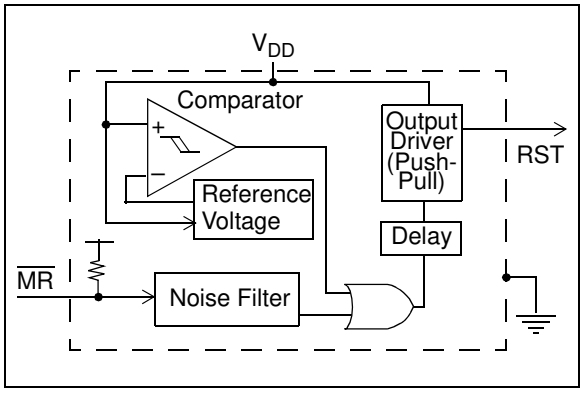


FIGURE 4-6: *TC1271A Block Diagram.*

4.2 Voltage Detect Circuit

The voltage detect circuit monitors V_{DD}. The device's Reset voltage trip point (V_{TRIP}) is selected when the device is ordered. The voltage on the device's V_{DD} pin determines the output state of the $\overline{RST}$/RST pin.

V_{DD} voltages above the $V_{TRIP(MAX)}$ force the $\overline{RST}$/RST pin inactive. V_{DD} voltages below the $V_{TRIP(MIN)}$ force the $\overline{RST}$/RST pin active. The state of the $\overline{RST}$/RST pin is unknown for V_{DD} voltages between $V_{TRIP(MAX)}$ and $V_{TRIP(MIN)}$. This is shown in Table 4-1

TABLE 4-1: V_{DD} LEVELS TO $\overline{RST}$/RST OUTPUT STATES

V_{DD} Voltage Level	Output State	
	$\overline{RST}$	RST
$V_{DD} \geq V_{TRIP(MAX)}$	H(1, 2)	L(1)
$V_{TRIP(MIN)} < V_{DD} < V_{TRIP(MAX)}$	U	U
$V_{DD} \leq V_{TRIP(MIN)}$	L	H

Legend: H = Driven High L = Driven Low
U = Unknown, driven either High or Low

Note 1: The $\overline{RST}$/RST pin will be driven inactive after the Reset Delay Timer (t_{RST}) times out.

2: The TC1270AN $\overline{RST}$ pin will be floated after the Reset Delay Timer (t_{RST}) times out.

The term V_{TRIP} will be used as the general term for the trip point voltage where the device actually trips.

In the case where V_{DD} is falling (for voltages starting above $V_{TRIP(MAX)}$):

- Voltages above $V_{TRIP(MAX)}$ will never cause the $\overline{RST}$/RST output pin to be driven active.
- Voltages below $V_{TRIP(MIN)}$ will always cause the $\overline{RST}$/RST output pin to be driven active.

In the case where V_{DD} is rising (for voltages starting below $V_{TRIP(MIN)}$):

- Voltages above $V_{TRIP(MAX)}$ will always cause the $\overline{RST}$/RST output pin to be driven inactive, (or floated, in the TC1270AN) after the Reset Delay Timer (t_{RST}), times out.

Table 4-2 shows the various device trip point options and their $V_{TRIP(MAX)}$ and $V_{TRIP(MIN)}$ voltages. The negative percentage change from common regulated voltages is also shown.

If the V_{DD} is falling from the regulated voltage as it crosses the V_{TRIP} voltage, the $\overline{RST}$/RST pin is driven active. Then, the desired circuitry is forced into Reset, or the circuitry has the indication that the V_{DD} is below the selected V_{TRIP}.

If the V_{DD} is rising as it crosses the V_{TRIP} voltage, the $\overline{RST}$/RST pin is driven inactive after the Reset Delay Timer elapses. Then, the desired circuitry is released from Reset and will start to operate in its Normal mode, or the circuitry has the indication that the V_{DD} is above the selected V_{TRIP}.

TABLE 4-2: SELECTING THE TRIP POINT

Trip Voltage Selection	$V_{TRIP(MAX)}$ (1)/ $V_{TRIP(MIN)}$ (2)	- % From Regulated Voltage		
		5.0V	3.3V	3.0V
L	4.75V	5.0%	—	—
	4.50V	10.0%	—	—
M	4.50V	10.0%	—	—
	4.25V	15.0%	—	—
T	3.15V	—	4.5%	—
	3.00V	—	9.2%	—
S	3.00V	—	9.2%	—
	2.85V	—	13.7%	—
R	2.70V	—	—	10.0%
	2.55V	—	—	15.0%

Note 1: Voltage regulator circuit must have tighter tolerance (%) than $V_{TRIP(MAX)}$% from regulated voltage.

2: Circuitry being reset must have a wider tolerance (%) than $V_{TRIP(MIN)}$% from regulated voltage.

The TC1270A/TC1270AN/TC1271A devices are optimized to reject fast transient glitches on the V_{DD} line. If the low input signal (which is below V_{TRIP}) is not rejected, the Reset output is driven active within 50 µs of V_{DD} falling through the Reset voltage threshold.

After the device exits the Reset condition, the delay circuitry will hold the $\overline{RST}$/RST pin active until the appropriate Reset delay time (t_{RST}) has elapsed.

During device power-up, the input voltage is below the trip point voltage. The device must enter the valid operating range for the device to start operation.

4.2.1 HYSTERESIS

There is also a minimal hysteresis (V_{HYS}) on the trip point. This is so that small noise signals on the device voltage (V_{DD}) do not cause the Reset pin ($\overline{RST}$/RST) to "jitter" (oscillate between active and inactive levels).

The characterization graphs shown in Figures 2-13 through 2-15 show the device hysteresis as a percentage of the voltage trip point (V_{TRIP}).

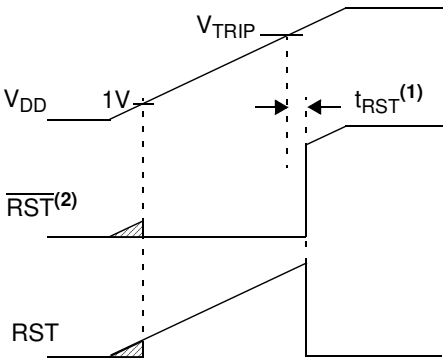
The Reset Delay Timer (t_{RST}) gives a time-based hysteresis for the system.

4.2.2 POWER-UP/RISING V_{DD}

As the device V_{DD} rises, the device's Reset circuit will remain active until the voltage rises above the "actual" trip point (V_{TRIP}).

Figure 4-7 shows a power-up sequence and the waveform of the $\overline{RST}$ and RST pins. As the device powers up, the voltage will start below the valid operating voltage of the device. At this voltage, the $\overline{RST}$/RST output is not valid. Once the voltage is above the minimum operating voltage (1V) and below the selected V_{TRIP}, the Reset output will be active.

Once the device voltage rises above the V_{TRIP} voltage, the Reset Delay Timer (t_{RST}) starts. When the Reset Delay Timer times out, the Reset output ($\overline{RST}$/RST) is driven inactive.



Note 1: Additional system current is consumed during the t_{RST} time.

2: The TC1270AN requires an external pull-up resistor.

FIGURE 4-7: *$\overline{RST}$/RST Pin Operation Power-up.*

4.2.3 POWER-DOWN/BROWN-OUT

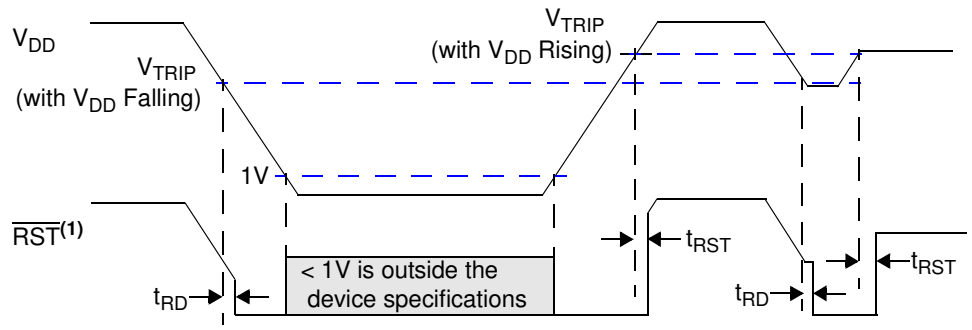
As the device powers-down/browns-out, the V_{DD} falls from a voltage above the devices trip point (V_{TRIP}). The device will trip at a voltage between the maximum trip point ($V_{TRIP(MAX)}$) and the minimum trip point ($V_{TRIP(MIN)}$). Once the device voltage (V_{DD}) goes below this voltage, the $\overline{RST}$/RST pin will be forced to the active state. Table 4-3 shows the state of the $\overline{RST}$ or RST pins.

Figure 4-8 shows the waveform of the $\overline{RST}$ pin as determined by the V_{DD} voltage. As the V_{DD} voltage falls from the normal operating point, the device "enters" Reset by crossing the V_{TRIP} voltage (between $V_{TRIP(MAX)}$ and $V_{TRIP(MIN)}$). Then, when V_{DD} voltage rises, the device "exits" Reset by crossing the V_{TRIP} voltage (below, or at, $V_{TRIP(MAX)}$). After the "exit" state has been detected, the Reset Delay Timer (t_{RST}) starts. When the t_{RST} time completes, the Reset pin is driven inactive.

TABLE 4-3: RESET PIN STATES

Device	State of $\overline{RST}$ Pin when:		State of RST Pin when:		Output Driver
	$V_{DD} < V_{TRIP}$	$V_{DD} > V_{TRIP}$(1)	$V_{DD} < V_{TRIP}$	$V_{DD} > V_{TRIP}$(1)	
TC1270A	L	H	—	—	Push-Pull
TC1271A	—	—	H	L	Push-Pull

Note 1: The $\overline{RST}$/RST pin will be driven inactive after the Reset Delay Timer (t_{RST}) times out.



Note 1: The TC1270AN requires an external pull-up resistor.

FIGURE 4-8: *$\overline{RST}$ Operation as determined by the V_{TRIP}*

4.3 Negative-Going V_{DD} Transients

The minimum pulse width (time) required to cause a Reset may be an important criteria in the implementation of a Power-on Reset (POR) circuit. This time is referred to as transient duration. The TC127XA devices are designed to reject a level of negative-going transients (glitches) on the power supply line.

Transient duration is the amount of time needed for these supervisory devices to respond to a drop in V_{DD}. The transient duration time (t_{TRAN}) is dependent on the magnitude of $V_{TRIP} - V_{DD}$ (overdrive). Any combination of duration and overdrive that lies under the duration/overdrive curve will not generate a Reset signal. Generally speaking, the transient duration time decreases with an increase in the $V_{TRIP} - V_{DD}$ voltage.

Figure 4-9 shows an example transient duration vs. Reset comparator overdrive. It shows that the farther below the trip point the transient pulse goes, the shorter the duration of the pulse required to cause a Reset gets. So, any combination of duration and overdrive that lays **under** the curve will **not** generate a Reset signal. Combinations **above** the curve are detected as a brown-out or power-down.

Transient immunity can be improved by adding a bypass capacitor (typically 0.1 µF) as close as possible to the V_{DD} pin of the TC127XA device.

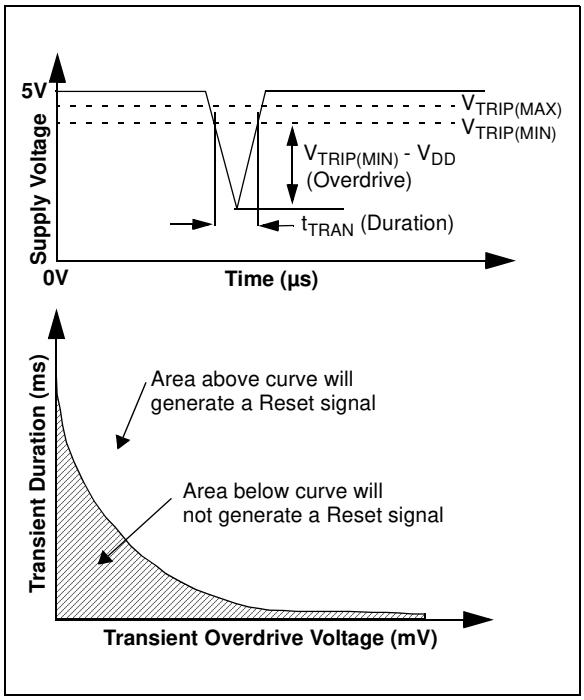


FIGURE 4-9: *Example of Typical Transient Duration Waveform.*

4.4 Manual Reset with Glitch Filter Circuit

The Manual Reset input pin ($\overline{MR}$) allows the Reset pins (RST/$\overline{RST}$) to be manually forced to their active states. The $\overline{MR}$ pin has circuitry to filter noise pulses that may be present on the pin. Figure 4-10 shows a block diagram for using the TC127XA with a push button switch. To minimize the required external components, the $\overline{MR}$ input has an internal pull-up resistor.

A mechanical push button or active logic signal can drive the $\overline{MR}$ input.

Once $\overline{MR}$ has been low for a time, t_{MD} (the manual Reset delay time), the Reset output pins are forced active. The Reset output pins will remain in their active states for the Reset Delay Timer time-out period (t_{RST}).

Figure 4-11 shows a waveform for the manual Reset switch input and the Reset pins output.

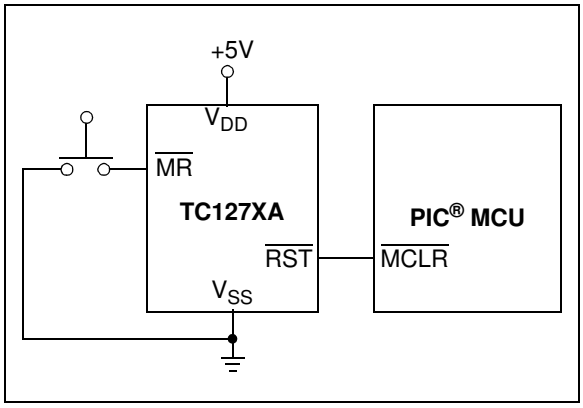


FIGURE 4-10: *Push Button Reset.*

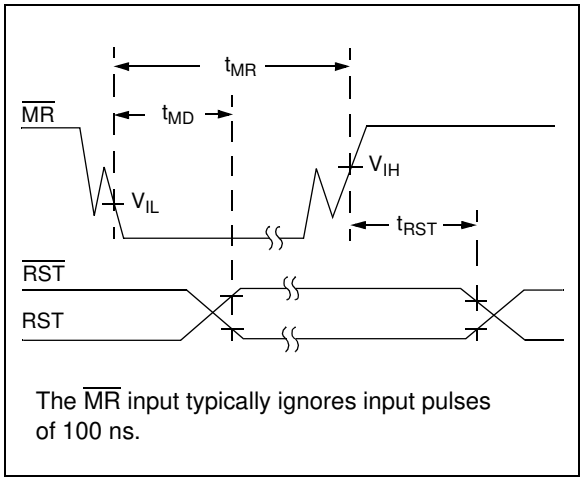


FIGURE 4-11: *$\overline{MR}$ Input – Push Button.*

4.4.1 NOISE FILTER

The noise filter filters out noise spikes (glitches) on the Manual Reset pin ($\overline{MR}$). Noise spikes less than 100 ns (typical) are filtered.

4.5 Reset Generator Circuit

The output signals from the voltage detect circuit and the manual Reset with glitch filter circuit are OR'd together and used to activate the Reset generator module.

After the Reset conditions have been removed (the $\overline{MR}$ pin is no longer forced low and the input voltage is greater than the trip point voltage), the Reset generator circuit determines the Reset delay time-out required.

There are three options for the delay circuit. These are:

- 2.19 ms (typical) delay
- 35 ms (typical) delay
- 280 ms (typical) delay

4.5.1 RESET DELAY TIMER

The Reset Delay Timer ensures that the TC127XA device will "hold" the embedded system in Reset until the system voltage has stabilized. The Reset Delay Timer time-out is shown in Table 4-4.

The Reset Delay Timer starts when the voltage detect circuit output AND the manual Reset with glitch filter circuit output become inactive. While the Reset Delay Timer is active, the $\overline{RST}$ or RST pin is driven to the active state. When the Reset Delay Timer times out, the $\overline{RST}$ or RST pin is driven inactive.

The Reset Delay Timer (t_{RST}) starts after the device voltage rises above the "actual" trip point (V_{TRIP}). When the Reset Delay Timer times out, the Reset output pin (RST/$\overline{RST}$) is driven inactive.

The Reset Delay Timer is cleared if either, or both, the voltage detector circuit output and the manual Reset with glitch filter circuit output become active. The $\overline{RST}$ or RST pin continues to be driven to the active state.

Figure 4-12 illustrates when the Reset Delay Timer (t_{RST}) is active or inactive.

4.5.2 EFFECT OF TEMPERATURE ON RESET POWER-UP TIMER (t_{RPU})

The Reset Delay Timer time-out period (t_{RST}) determines how long the device remains in the Reset condition. This time out is affected by the device V_{DD} and the temperature. Typical responses for varying V_{DD} values and temperatures are presented in Figures 2-28, 2-29 and 2-30.

TABLE 4-4: RESET DELAY TIMER TIME OUTS

t_{RST}			Units
Min	Typ	Max	
1.09	2.19	4.38	ms
17.5	35	70	ms
140	280	560	ms
↑ This is the minimum time that the Reset Delay Timer will "hold" the Reset pin active after V_{DD} rises above V_{TRIP}		↑ This is the maximum time that the Reset Delay Timer will "hold" the Reset pin active after V_{DD} rises above V_{TRIP}	

Note 1: Shaded rows are custom-ordered time outs.

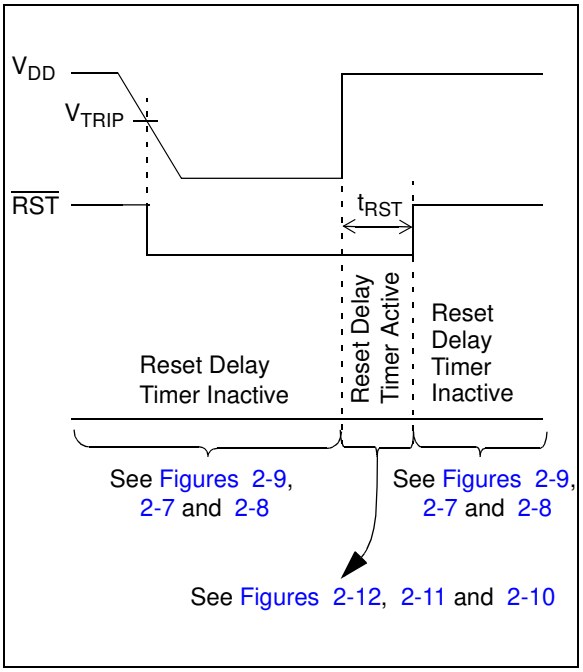


FIGURE 4-12: *Reset Power-up Timer Waveform.*

5.0 APPLICATION INFORMATION

This section presents application-related information that may be useful for your particular design requirements.

5.1 Supply Monitor Noise Sensitivity

The TC127XA devices are optimized for fast responses to negative-going changes in V_{DD}. A system with an inordinate amount of electrical noise on V_{DD} (such as a system using relays) may require a 0.01 µF or 0.1 µF bypass capacitor to reduce detection sensitivity. This capacitor should be installed as close to the TC127XA as possible to keep the capacitor lead length short.

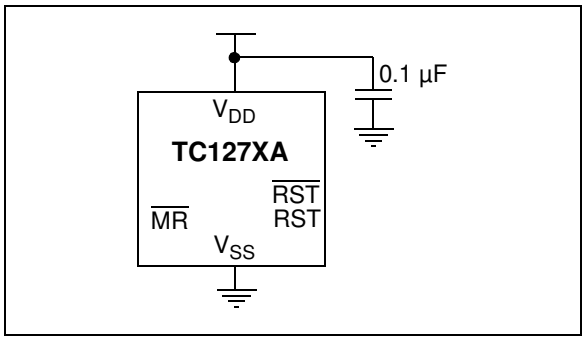


FIGURE 5-1: *Typical Application Circuit with Bypass Capacitor.*

5.2 Conventional Voltage Monitoring

Figure 5-2 and Figure 5-3 show the TC127XA in conventional voltage monitoring applications.

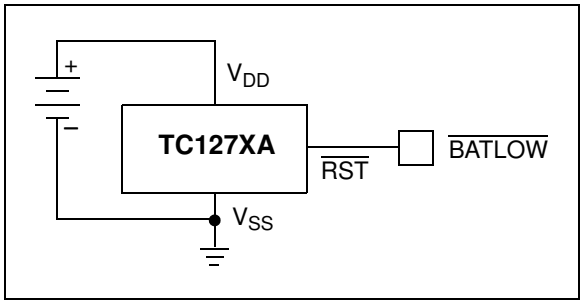


FIGURE 5-2: *Battery Voltage Monitor.*

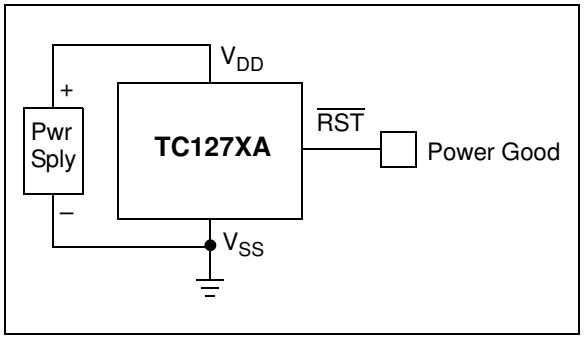


FIGURE 5-3: *Power Good Monitor.*

5.3 Using in PIC® Microcontroller, ICSP™ Applications

Note: This operation can only be done using the device that has an Open-Drain RST pin (TC1270AN).

Figure 5-4 shows the typical application circuit for using the TC1270AN for voltage supervisory function when the PIC microcontroller will be programmed via the In-Circuit Serial Programming™ (ICSP™) feature. Additional information is available in the Microchip Technical Brief TB087, *"Using Voltage Supervisors with PICmicro® Microcontroller Systems which Implement In-Circuit Serial Programming™"* (DS91087).

Note: It is recommended that the current into the RST pin is current that is limited by a 1 kΩ resistor.

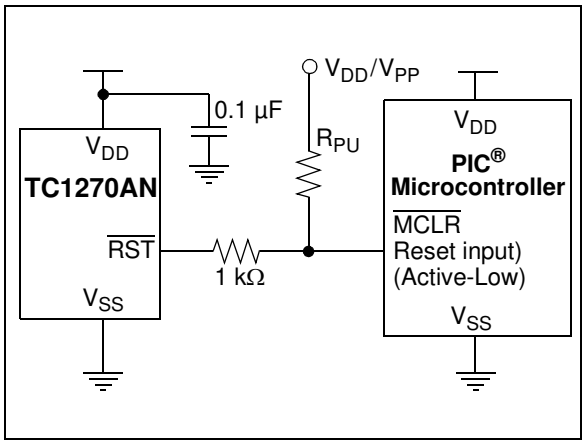


FIGURE 5-4: *Typical Application Circuit for PIC Microcontroller with the ICSP Feature.*