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TC1426/TC1427/TC1428

1.2A Dual High-Speed MOSFET Drivers

Features:

- Low Cost
- Latch-Up Protected: Will Withstand 500 mA Reverse Output Current
- ESD Protected ±2kV
- High Peak Output Current: 1.2A
- Wide Operating Range:
  - 4.5V to 16V
- High Capacitive Load Drive Capability: 1000 pF in 38 nsec
- Low Delay Time: 75 nsec Max
- Logic Input Threshold Independent of Supply Voltage
- Output Voltage Swing to Within 25 mV of Ground or V_{DD}
- Low Output Impedance: 8Ω

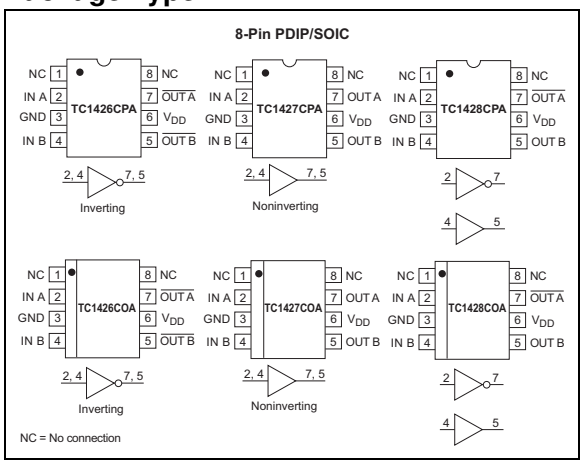
Applications:

- Power MOSFET Drivers
- Switched Mode Power Supplies
- Pulse Transformer Drive
- Small Motor Controls
- Print Head Drive

Device Selection Table

Part Number	Package	Temp. Range
TC1426COA	8-Pin SOIC	0°C to +70°C
TC1426CPA	8-Pin PDIP	0°C to +70°C
TC1427COA	8-Pin SOIC	0°C to +70°C
TC1427CPA	8-Pin PDIP	0°C to +70°C
TC1428COA	8-Pin SOIC	0°C to +70°C
TC1428CPA	8-Pin PDIP	0°C to +70°C

Package Type



General Description:

The TC1426/TC1427/TC1428 are a family of 1.2A dual high-speed drivers. CMOS fabrication is used for low-power consumption and high efficiency.

These devices are fabricated using an epitaxial layer to effectively short out the intrinsic parasitic transistor responsible for CMOS latch-up. They incorporate a number of other design and process refinements to increase their long-term reliability.

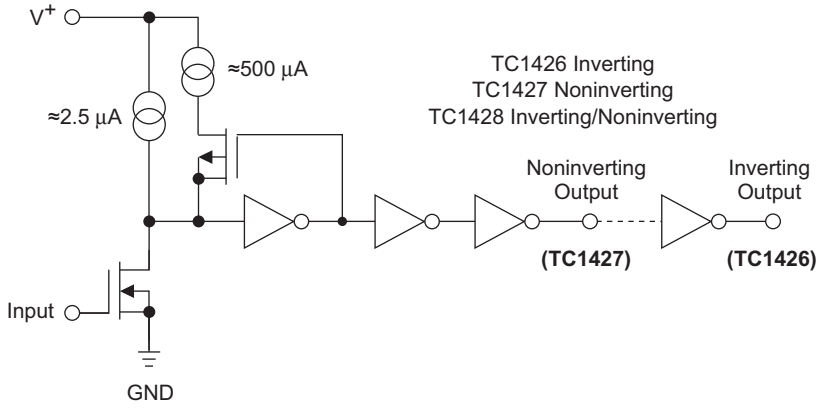
The TC1426 is compatible with the bipolar DS0026, but only draws 1/5 of the quiescent current. The TC1426/TC1427/TC1428 are also compatible with the TC426/TC427/TC428, but with 1.2A peak output current rather than the 1.5A of the TC426/TC427/TC428 devices.

Other compatible drivers are the TC4426/TC4427/TC4428 and the TC4426A/TC4427A/TC4428A. The TC4426/TC4427/TC4428 have the added feature that the inputs can withstand negative voltage up to 5V with diode protection circuits. The TC4426A/TC4427A/TC4428A have matched input to output leading edge and falling edge delays, t_{D1} and t_{D2}, for processing short duration pulses in the 25 nanoseconds range. All of the above drivers are pin compatible.

The high-input impedance TC1426/TC1427/TC1428 drivers are CMOS/TTL input-compatible, do not require the speed-up needed by the bipolar devices, and can be directly driven by most PWM ICs.

This family of devices is available in inverting and non-inverting versions. Specifications have been optimized to achieve low-cost and high-performance devices, well-suited for the high-volume manufacturer.

Functional Block Diagram



NOTE: TC1428 has one inverting and one noninverting driver.
Ground any unused driver input.

1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings*

Supply Voltage ..... +18V
Input Voltage, Any Terminal
..... V_{DD} + 0.3V to GND – 0.3V
Power Dissipation ($T_A \leq 70°C$)
PDIP ..... 730 mW
SOIC ..... 470 mW
Derating Factor
PDIP ..... 8 mW/°C
SOIC ..... 4 mW/°C
Operating Temperature Range
C Version ..... 0°C to +70°C
Storage Temperature Range ..... -65°C to +150°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operation sections of the specifications is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

TC1426/TC1427/TC1428 ELECTRICAL SPECIFICATIONS

Electrical Characteristics: T_A = +25°C, with 4.5V $\leq V_{DD} \leq$ 16V, unless otherwise noted.						
Symbol	**Parameter**	**Min**	**Typ**	**Max**	**Units**	**Test Conditions**
Input						
V_{IH}	Logic 1, High Input Voltage	3	—	—	V	
V_{IL}	Logic 0, Low Input Voltage	—	—	0.8	V	
I_{IN}	Input Current	-1	—	1	µA	$0V \leq V_{IN} \leq V_{DD}$
Output						
V_{OH}	High Output Voltage	V_{DD} – 0.025	—	—	V	Figure 3-1, Figure 3-2
V_{OL}	Low Output Voltage	—	—	0.025	V	Figure 3-1, Figure 3-2
R_O	Output Resistance	— —	12 8	18 12	Ω	I_{OUT} = 10 mA, V_{DD} = 16V
I_{PK}	Peak Output Current	—	1.2	—	A	
I_{REV}	Latch-Up Current Withstand Reverse Current	—	>500	—	mA	
Switching Time (Note 1)						
t_R	Rise Time	—	—	35	nsec	Figure 3-1, Figure 3-2
t_F	Fall Time	—	—	25	nsec	Figure 3-1, Figure 3-2
t_{D1}	Delay Time	—	—	75	nsec	Figure 3-1, Figure 3-2
t_{D2}	Delay Time	—	—	75	nsec	Figure 3-1, Figure 3-2
Power Supply						
I_S	Power Supply Current	— —	— —	9 0.5	mA	V_{IN} = 3V (Both Inputs) V_{IN} = 0V (Both Inputs)

Note 1: Switching times ensured by design.

TC1426/TC1427/TC1428 ELECTRICAL SPECIFICATIONS (CONTINUED)

Electrical Characteristics: Over operating temperature range with 4.5V ≤ V_{DD} ≤ 16V, unless otherwise noted.

Symbol	Parameter	Min	Typ	Max	Units	Test Conditions
Input						
V_{IH}	Logic 1, High Input Voltage	3	—	—	V	
V_{IL}	Logic 0, Low Input Voltage	—	—	0.8	V	
I_{IN}	Input Current	-10	—	10	µA	0V ≤ V_{IN} ≤ V_{DD}
Output						
V_{OH}	High Output Voltage	V_{DD} – 0.025	—	—	V	Figure 3-1, Figure 3-2
V_{OL}	Low Output Voltage	—	—	0.025	V	Figure 3-1, Figure 3-2
R_O	Output Resistance	— —	15 10	23 18	Ω	I_{OUT} = 10 mA, V_{DD} = 16V
I_{REV}	Latch-Up Current Withstand Reverse Current	—	>500	—	mA	
Switching Time (Note 1)						
t_R	Rise Time	—	—	60	nsec	Figure 3-1, Figure 3-2
t_F	Fall Time	—	—	40	nsec	Figure 3-1, Figure 3-2
t_{D1}	Delay Time	—	—	125	nsec	Figure 3-1, Figure 3-2
t_{D2}	Delay Time	—	—	125	nsec	Figure 3-1, Figure 3-2
Power Supply						
I_S	Power Supply Current	— —	— —	13 0.7	mA	V_{IN} = 3V (Both Inputs) V_{IN} = 0V (Both Inputs)

Note 1: Switching times ensured by design.

2.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 2-1.

TABLE 2-1: PIN FUNCTION TABLE

Pin No. (8-Pin PDIP, SOIC)	Symbol	Description
1	NC	No connection.
2	IN A	Control input A, TTL/CMOS compatible logic input.
3	GND	Ground.
4	IN B	Control input B, TTL/CMOS compatible logic input.
5	OUT B	Output B, CMOS totem-pole output.
6	V_{DD}	Supply input, 4.5V to 16V.
7	OUT A	Output A, CMOS totem-pole output.
8	NC	No connection.

3.0 APPLICATIONS INFORMATION

3.1 SUPPLY BYPASSING

Large currents are required to charge and discharge capacitive loads quickly. For example, charging a 1000 pF load to 16V in 25 nsec requires a 0.8A current from the device's power supply.

To ensure low supply impedance over a wide frequency range, a parallel capacitor combination is recommended for supply bypassing. Low-inductance ceramic MLC capacitors with short lead lengths (<0.5-in.) should be used. A 1.0 μF film capacitor in parallel with one or two 0.1 μF ceramic MLC capacitors normally provides adequate bypassing.

3.2 GROUNDING

The TC1426 and TC1428 contain inverting drivers. Individual ground returns for the input and output circuits or a ground plane should be used. This will reduce negative feedback that causes degradation in switching speed characteristics.

3.3 INPUT STAGE

The input voltage level changes the no-load or quiescent supply current. The N-channel MOSFET input stage transistor drives a 2.5 mA current source load. With a logic '1' input, the maximum quiescent supply current is 9 mA. Logic '0' input level signals reduce quiescent current to 500 μA maximum. **Unused driver inputs must be connected to V_{DD} or GND**. Minimum power dissipation occurs for logic '0' inputs for the TC1426/TC1427/TC1428.

The drivers are designed with 100 mV of hysteresis. This provides clean transitions and minimizes output stage current spiking when changing states. Input voltage thresholds are approximately 1.5V, making a logic '1' input any voltage greater than 1.5V up to V_{DD}. Input current is less than 1 μA over this range.

The TC1426/TC1427/TC1428 may be directly driven by the TL494, SG1526/27, TC38C42, TC170 and similar switch-mode power supply integrated circuits.

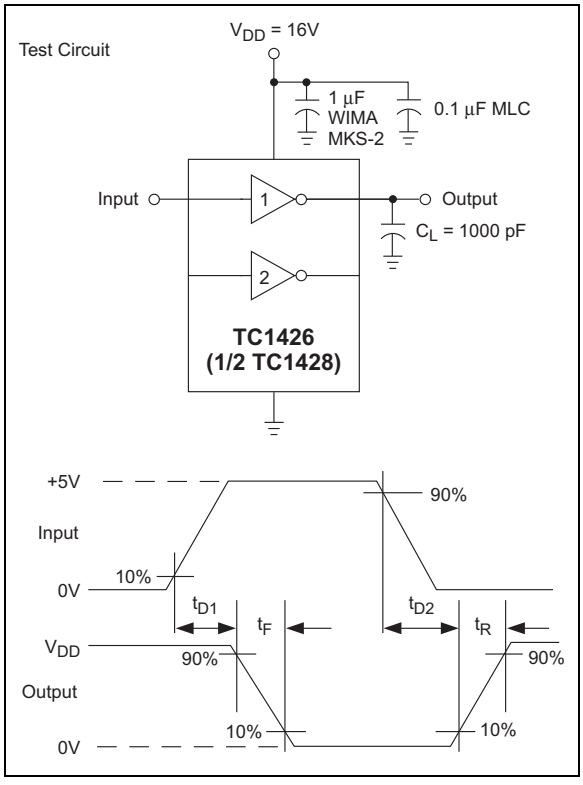


FIGURE 3-1: *Inverting Driver Switching Time*

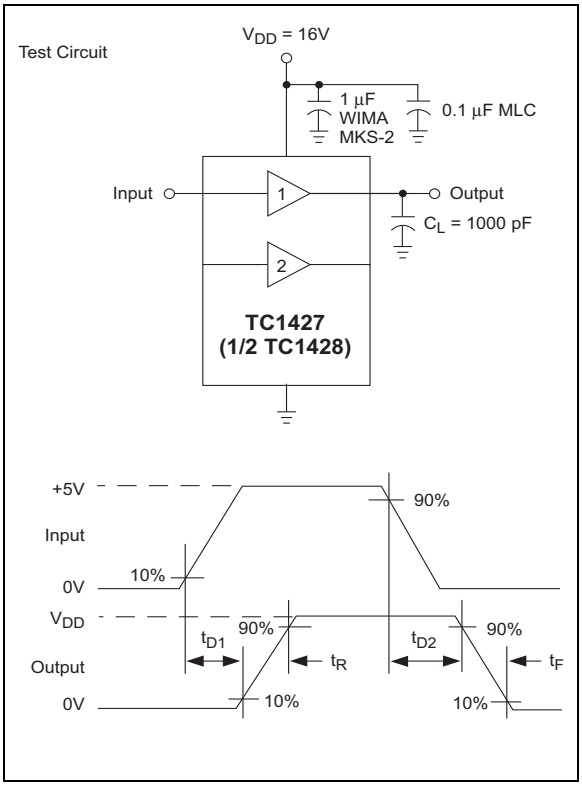
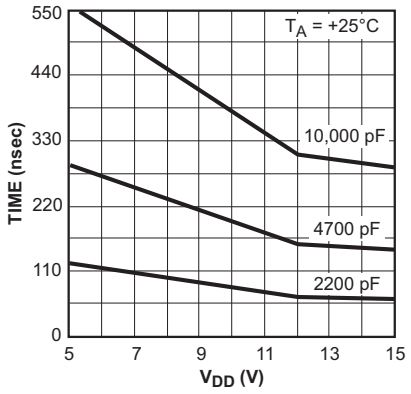


FIGURE 3-2: *Noninverting Driver Switching Time*

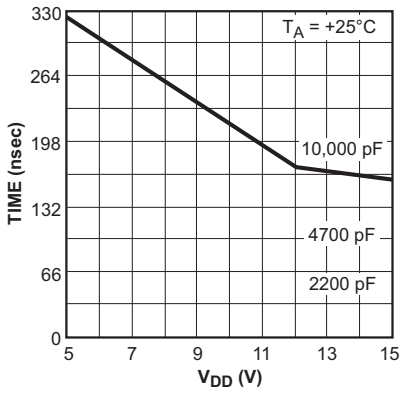
4.0 TYPICAL CHARACTERISTICS

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

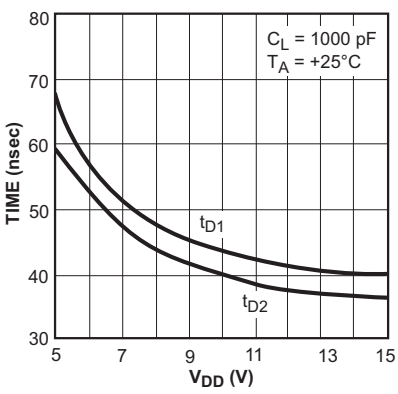
Rise Time vs. Supply Voltage



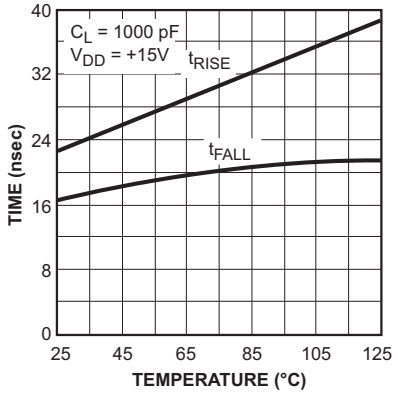
Fall Time vs. Supply Voltage



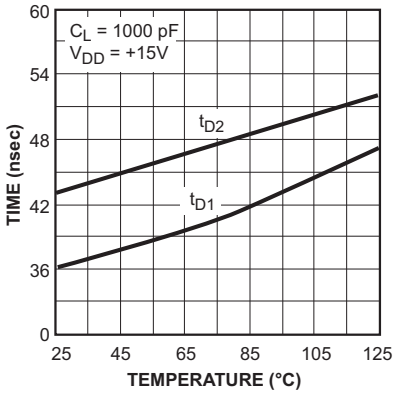
Delay Time vs. Supply Voltage



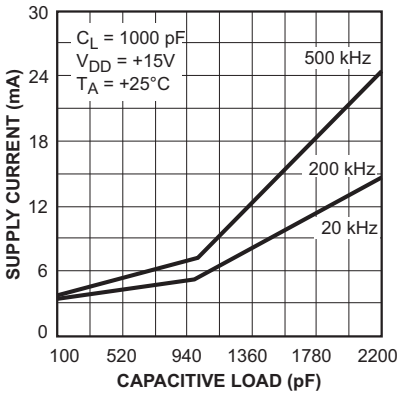
Rise and Fall Times vs. Temperature



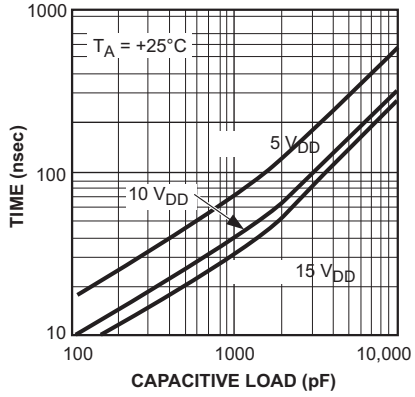
Delay Time vs. Temperature



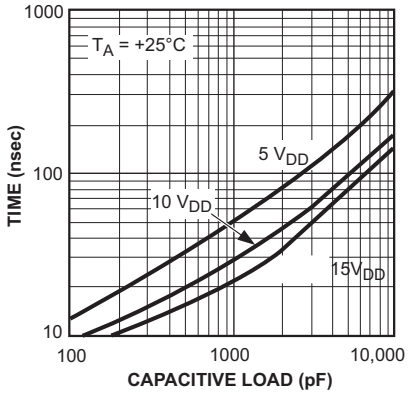
Supply Current vs. Capacitive Load



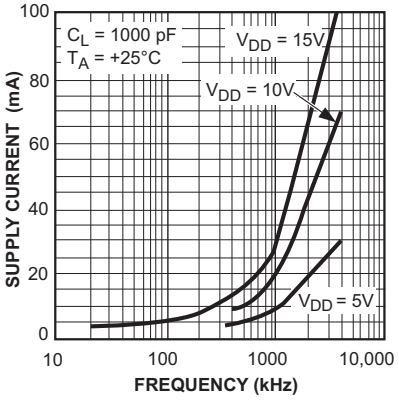
Rise Time vs. Capacitive Load



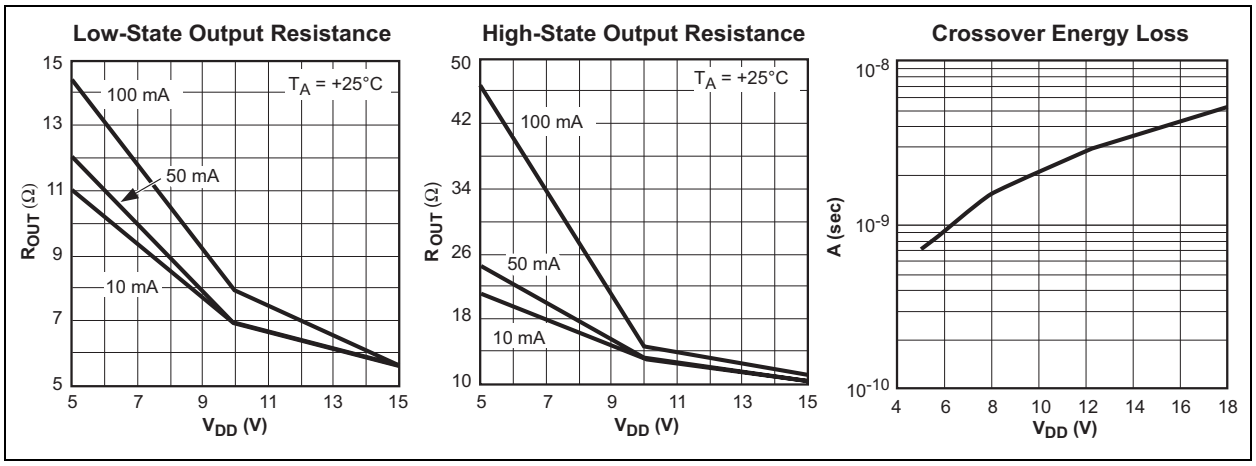
Fall Time vs. Capacitive Load

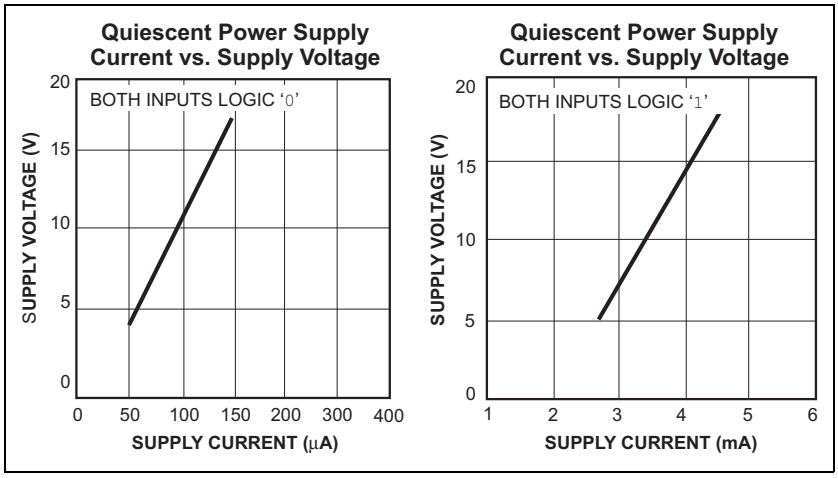


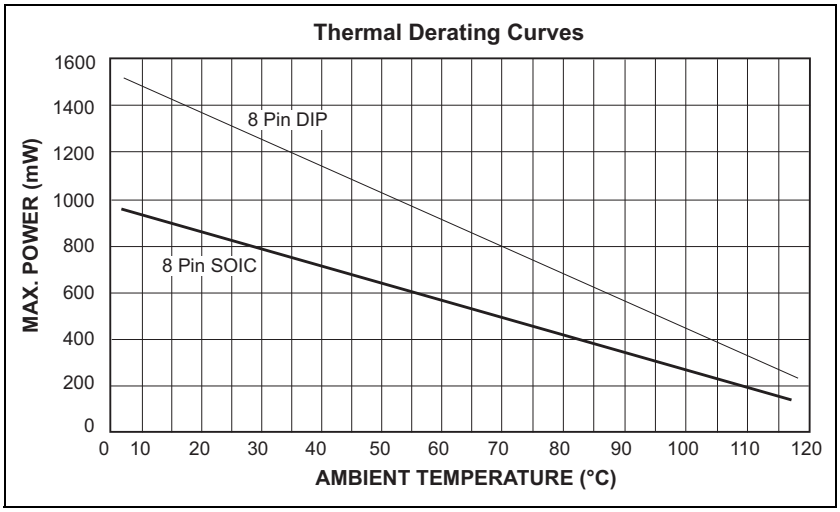
Supply Current vs. Frequency



TYPICAL CHARACTERISTICS (CONTINUED)







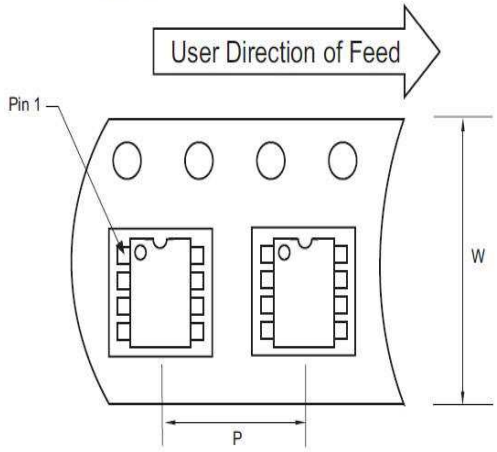
5.0 PACKAGING INFORMATION

5.1 Package Marking Information

Package marking data not available at this time.

5.2 Taping Form

Component Taping Orientation for 8-Pin MSOP Devices

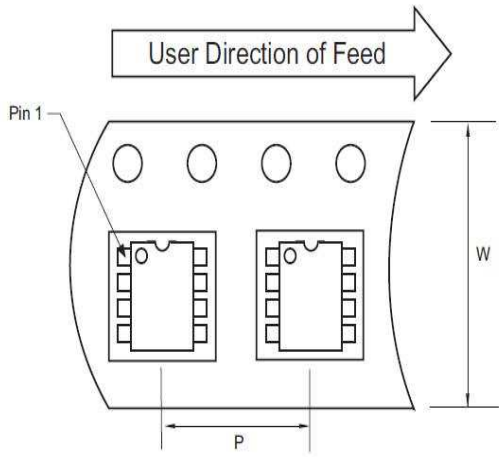


Standard Reel Component Orientation
for 713 Suffix Device

Carrier Tape, Number of Components Per Reel and Reel Size

Package	Carrier Width (W)	Pitch (P)	Part Per Full Reel	Reel Size
8-Pin MSOP	12 mm	8 mm	2500	13 in

Component Taping Orientation for 8-Pin SOIC (Narrow) Devices



Standard Reel Component Orientation
for 713 Suffix Device

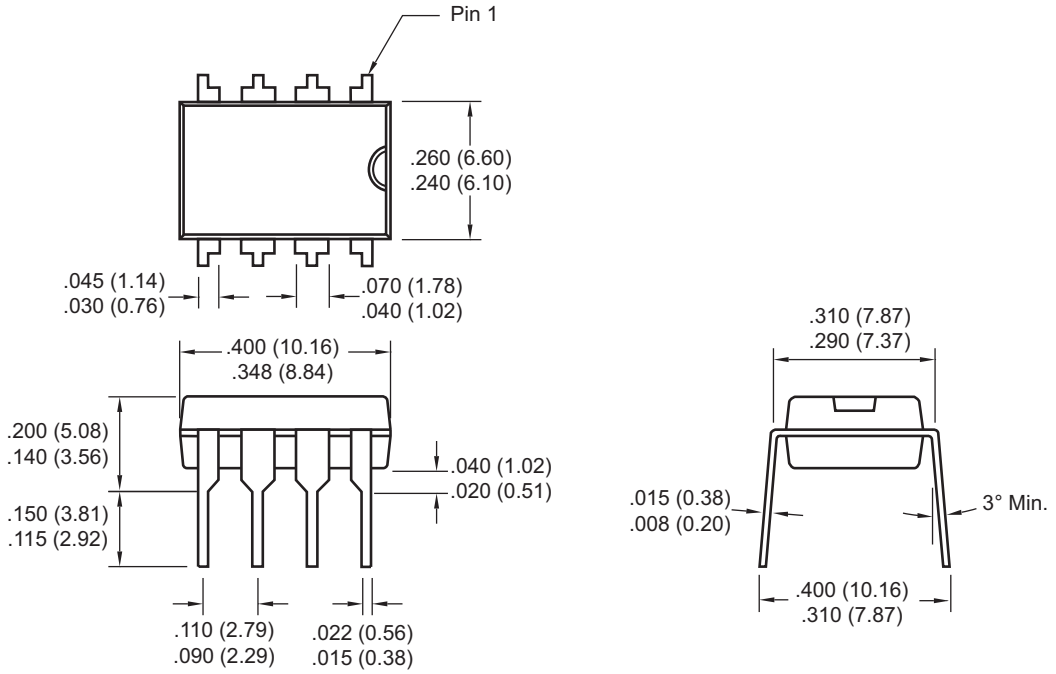
Carrier Tape, Number of Components Per Reel and Reel Size

Package	Carrier Width (W)	Pitch (P)	Part Per Full Reel	Reel Size
8-Pin SOIC (N)	12 mm	8 mm	2500	13 in

5.3 Package Dimensions

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

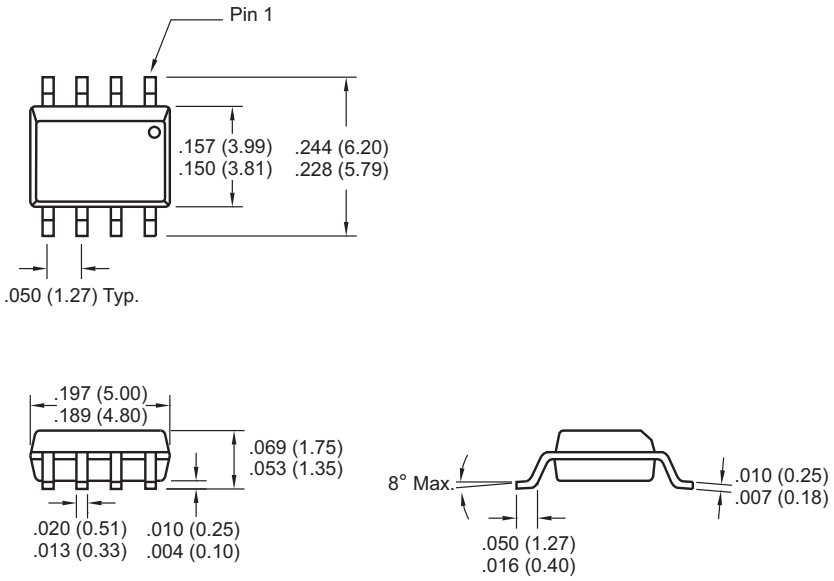
8-Pin Plastic DIP



Dimensions: inches (mm)

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

8-Pin SOIC



Dimensions: inches (mm)

6.0 REVISION HISTORY

Revision D (December 2012)

Added a note to each package outline drawing.

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India - Pune
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Japan - Yokohama
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