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TC1762

32-Bit Single-Chip Microcontroller

TriCore

Microcontrollers

Never stop thinking

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Preliminary

TC1762 Data Sheet
Revision History: V1.0, 2008-04

Previous Version: V0.5 2007-03

Page	Subjects (major changes since last revision)
7	VSSOSC3 is deleted from the TC1762 Logic Symbol.
8, 10	TDATA0 of Pin 17, TCLK0 of Pin 20, TCLK0 of Pin 74 and TDATA0 of Pin 77 are updated in the Pinning Diagram and Pin Definition and Functions Table.
33	Transmit DMA request in Block Diagram of ASC Interfaces is updated.
35	Alternate output functions in block diagram of SSC interfaces are updated.
41	Programmable baud rate of the MLI is updated.
42	TDATA0 and TCLK0 of the block diagram of MLI interfaces are updated.
54	The description for WDT double reset detection is updated.
91	The power sequencing details is updated.
102	MLI timing, maximum operating frequency limit is extended, t31 is added.
106	Thermal resistance junction leads is updated.

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1 Summary of Features

The TC1762 has the following features:

- High-performance 32-bit super-scaler TriCore v1.3 CPU with 4-stage pipeline
  - Superior real-time performance
  - Strong bit handling
  - Fully integrated DSP capabilities
  - Single precision Floating Point Unit (FPU)
  - 66 or 80 MHz operation at full temperature range
- Multiple on-chip memories
  - 32 Kbyte Local Data Memory (SRAM)
  - 4 Kbyte Overlay Memory
  - 8 Kbyte Scratch-Pad RAM (SPRAM)
  - 8 Kbyte Instruction Cache (ICACHE)
  - 1024 Kbyte Flash Memory
  - 16 Kbyte Data Flash (2 Kbyte EEPROM emulation)
  - 16 Kbyte Boot ROM
- 8-channel DMA Controller
- Fast-response interrupt system with 255 hardware priority arbitration levels serviced by CPU
- High-performance on-chip bus structure
  - 64-bit Local Memory Bus (LMB) to Flash memory
  - System Peripheral Bus (SPB) for interconnections of functional units
- Versatile on-chip Peripheral Units
  - Two Asynchronous/Synchronous Serial Channels (ASCs) with baudrate generator, parity, framing and overrun error detection
  - One High Speed Synchronous Serial Channel (SSC) with programmable data length and shift direction
  - One Micro Second Bus (MSC) interface for serial port expansion to external power devices
  - One high-speed Micro Link Interface (MLI) for serial inter-processor communication
  - One MultiCAN Module with two CAN nodes and 64 free assignable message objects for high efficiency data handling via FIFO buffering and gateway data transfer
  - One General Purpose Timer Array Module (GPTA) with a powerful set of digital signal filtering and timer functionality to realize autonomous and complex Input/Output management
  - One 16-channel Analog-to-Digital Converter unit (ADC) with selectable 8-bit, 10-bit, or 12-bit, supporting 32 input channels
  - One 2-channel Fast Analog-to-Digital Converter unit (FADC) with concatenated comb filters for hardware data reduction: supporting 10-bit resolution, with minimum conversion time of 262.5ns (@ 80 MHz) or 318.2ns (@ 66 MHz)

- 32 analog input lines for ADC and FADC
- 81 digital general purpose I/O lines
- Digital I/O ports with 3.3 V capability
- On-chip debug support for OCDS Level 1 and 2 (CPU, DMA)
- Dedicated Emulation Device chip for multi-core debugging, tracing, and calibration via USB V1.1 interface available (TC1766ED)
- Power Management System
- Clock Generation Unit with PLL
- Core supply voltage of 1.5 V
- I/O voltage of 3.3 V
- Full automotive temperature range: -40° to +125°C
- PG-LQFP-176-2 package

Ordering Information

The ordering code for Infineon microcontrollers provides an exact reference to the required product. This ordering code identifies:

- The derivative itself, i.e. its function set, the temperature range, and the supply voltage
- The package and the type of delivery

For the available ordering codes for the TC1762, please refer to the “Product Catalog Microcontrollers” that summarizes all available microcontroller variants.

This document describes the derivatives of the device.The **Table 1-1** enumerates these derivatives and summarizes the differences.

Table 1-1 TC1762 Derivative Synopsis

Derivative	Ambient Temperature Range
SAK-TC1762-128F66HL	T_A = -40°C to +125°C; 66 MHz operation frequency
SAK-TC1762-128F80HL	T_A = -40°C to +125°C; 80 MHz operation frequency

2 General Device Information

Chapter 2 provides the general information for the TC1762.

2.1 Block Diagram

Figure 2-1 shows the TC1762 block diagram.

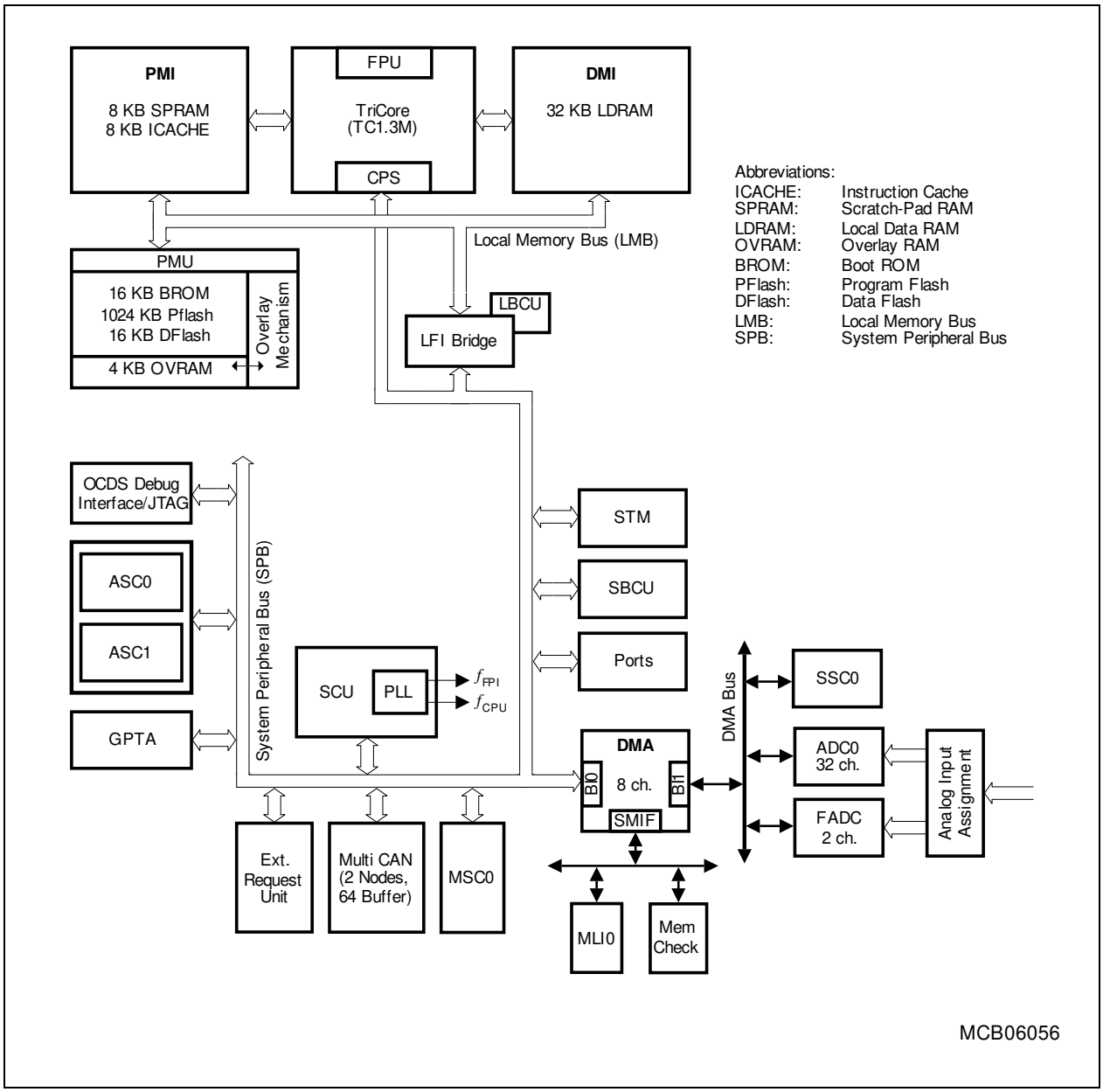

Figure 2-1 TC1762 Block Diagram

2.2 Logic Symbol

Figure 2-2 shows the TC1762 logic symbol.

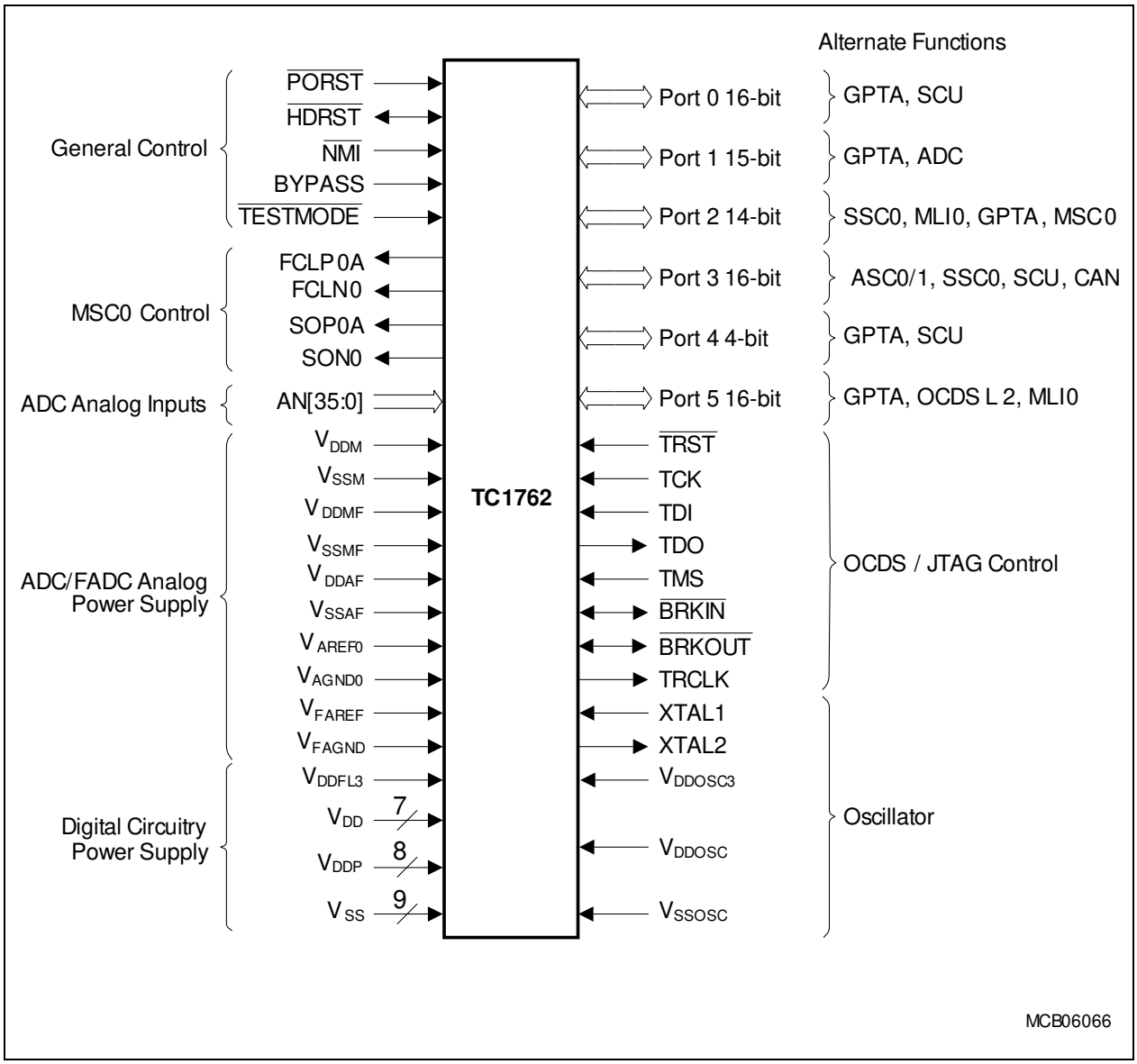

Figure 2-2 TC1762 Logic Symbol

2.3 Pin Configuration

Figure 2-3 shows the TC1762 pin configuration.

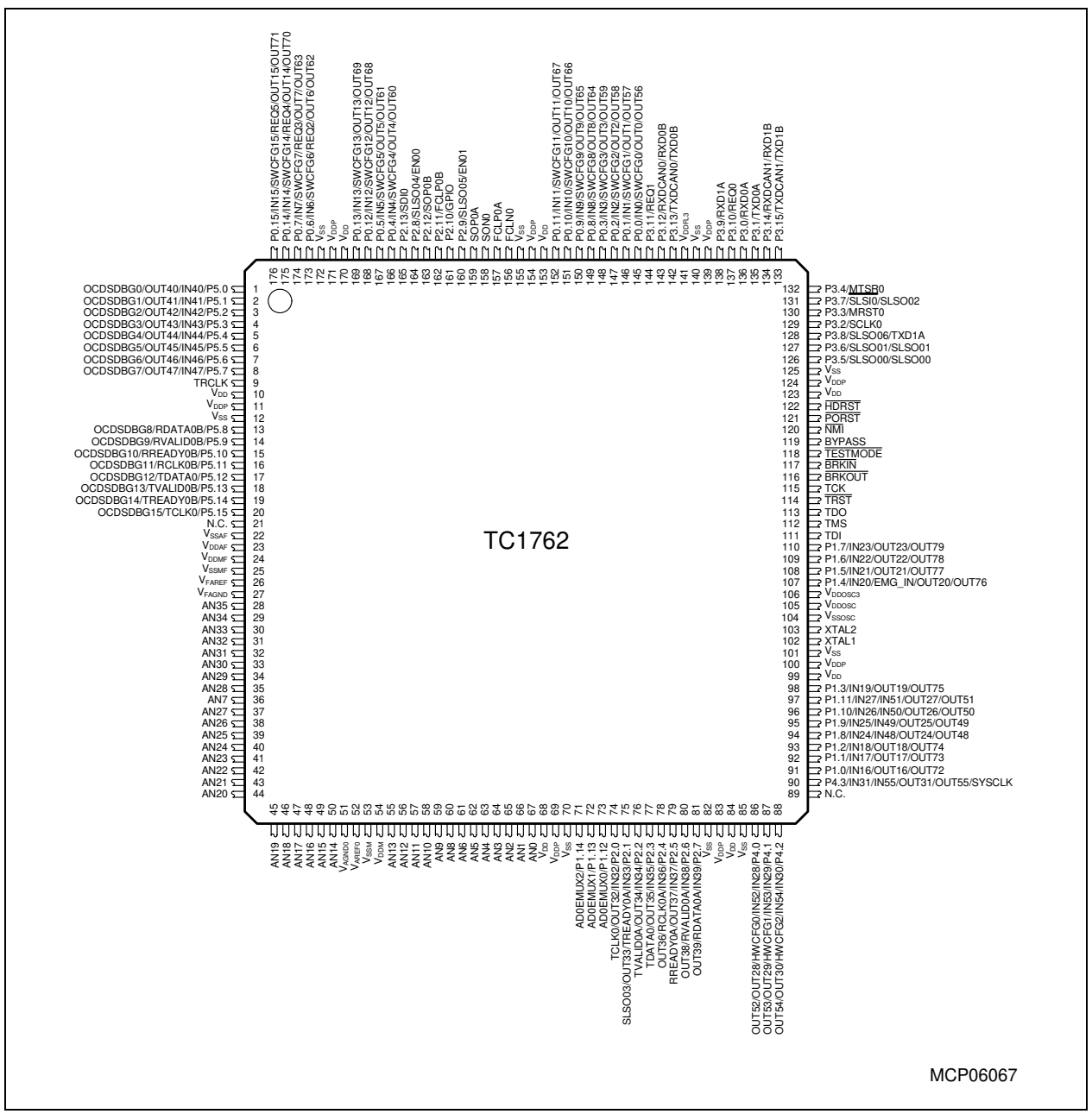

Figure 2-3 TC1762 Pinning for PG-LQFP-176-2 Package

2.4 Pad Driver and Input Classes Overview

The TC1762 provides different types and classes of input and output lines. For understanding of the abbreviations in **Table 2-1** starting at the next page, **Table 4-1** gives an overview on the pad type and class types.

2.5 Pin Definitions and Functions

Table 2-1 shows the TC1762 pin definitions and functions.

Table 2-1 Pin Definitions and Functions

Symbol	Pins	I/O	Pad Driver Class	Power Supply	Functions
Parallel Ports					
P0		I/O	A1	V_{DDP}	**Port 0** Port 0 is a 16-bit bi-directional general-purpose I/O port which can be alternatively used for GPTA I/O lines or external trigger inputs.
P0.0	145				IN0 / OUT0 / OUT56 line of GPTA
P0.1	146				IN1 / OUT1 / OUT57 line of GPTA
P0.2	147				IN2 / OUT2 / OUT58 line of GPTA
P0.3	148				IN3 / OUT3 / OUT59 line of GPTA
P0.4	166				IN4 / OUT4 / OUT60 line of GPTA
P0.5	167				IN5 / OUT5 / OUT61 line of GPTA
P0.6	173				IN6 / OUT6 / OUT62 line of GPTA REQ2 External trigger input 2
P0.7	174				IN7 / OUT7 / OUT63 line of GPTA REQ3 External trigger input 3
P0.8	149				IN8 / OUT8 / OUT64 line of GPTA
P0.9	150				IN9 / OUT9 / OUT65 line of GPTA
P0.10	151				IN10 / OUT10 / OUT66 line of GPTA
P0.11	152				IN11 / OUT11 / OUT67 line of GPTA
P0.12	168				IN12 / OUT12 / OUT68 line of GPTA
P0.13	169				IN13 / OUT13 / OUT69 line of GPTA
P0.14	175				IN14 / OUT14 / OUT70 line of GPTA REQ4 External trigger input 4
P0.15	176				IN15 / OUT15 / OUT71 line of GPTA REQ5 External trigger input 5
					In addition, the state of the port pins are latched into the software configuration input register SCU_SCLIR at the rising edge of HDRST. Therefore, Port 0 pins can be used for operating mode selections by software.

Table 2-1 Pin Definitions and Functions (cont'd)

Symbol	Pins	I/O	Pad Driver Class	Power Supply	Functions
P1		I/O		V_{DDP}	**Port 1** Port 1 is a 15-bit bi-directional general purpose I/O port which can be alternatively used for GPTA I/O lines and ADC0 interface.
P1.0	91		A1		IN16 / OUT16 / OUT72 line of GPTA
P1.1	92		A1		IN17 / OUT17 / OUT73 line of GPTA
P1.2	93		A1		IN18 / OUT18 / OUT74 line of GPTA
P1.3	98		A1		IN19 / OUT19 / OUT75 line of GPTA
P1.4	107		A1		IN20 / OUT20 / OUT76 line of GPTA
P1.5	108		A1		IN21 / OUT21 / OUT77 line of GPTA
P1.6	109		A1		IN22 / OUT22 / OUT78 line of GPTA
P1.7	110		A1		IN23 / OUT23 / OUT79 line of GPTA
P1.8	94		A2		IN24 / OUT24 / IN48 / OUT48 line of GPTA
P1.9	95		A2		IN25 / OUT25 / IN49 / OUT49 line of GPTA
P1.10	96		A2		IN26 / OUT26 / IN50 / OUT50 line of GPTA
P1.11	97		A2		IN27 / OUT27 / IN51 / OUT51 line of GPTA
P1.12	73		A1		AD0EMUX0 ADC0 external multiplexer control output 0
P1.13	72		A1		AD0EMUX1 ADC0 external multiplexer control output 1
P1.14	71		A1		AD0EMUX2 ADC0 external multiplexer control output 2
					In addition, P1.4 also serves as **emergency shut-off input** for certain I/O lines (e.g. GPTA related outputs).

Table 2-1 Pin Definitions and Functions (cont'd)

Symbol	Pins	I/O	Pad Driver Class	Power Supply	Functions	
P2		I/O		V_{DDP}	**Port 2** Port 2 is a 14-bit bi-directional general-purpose I/O port which can be alternatively used for GPTA I/O, and interface for MLI0, MSC0 or SSC0.	
P2.0	74		A2		TCLK0	MLI0 transmit channel clock output A
					IN32 / OUT32	line of GPTA
P2.1	75		A2		TREADY0A	MLI0 transmit channel ready input A
					IN33 / OUT33	line of GPTA
					SLSO03	SSC0 slave select output 3
P2.2	76		A2		TVALID0A	MLI0 transmit channel valid output A
					IN34 / OUT34	line of GPTA
P2.3	77		A2		TDATA0	MLI0 transmit channel data output A
					IN35 / OUT35	line of GPTA
P2.4	78		A1		RCLK0A	MLI0 receive channel clock input A
					IN36 / OUT36	line of GPTA
P2.5	79		A2		RREADY0A	MLI0 receive channel ready output A
					IN37 / OUT37	line of GPTA
P2.6	80		A1		RVALID0A	MLI0 receive channel valid input A
					IN38 / OUT38	line of GPTA
P2.7	81		A1		RDATA0A	MLI0 receive channel data input A
					IN39 / OUT39	line of GPTA

Table 2-1 Pin Definitions and Functions (cont'd)

Symbol	Pins	I/O	Pad Driver Class	Power Supply	Functions	
P2.8	164		A2		SLSO04	SSC0 Slave Select output 4
					EN00	MSC0 enable output 0
P2.9	160		A2		SLSO05	SSC0 Slave Select output 5
					EN01	MSC0 enable output 1
P2.10	161		A2			
P2.11	162		A2		FCLP0B	MSC0 clock output B
P2.12	163		A2		SOP0B	MSC0 serial data output B
P2.13	165		A1		SDI0	MSC0 serial data input

Table 2-1 Pin Definitions and Functions (cont'd)

Symbol	Pins	I/O	Pad Driver Class	Power Supply	Functions	
P3		I/O		V_{DDP}	**Port 3** Port 3 is a 16-bit bi-directional general-purpose I/O port which can be alternatively used for ASC0/1, SSC0 and CAN lines.	
P3.0	136		A2		RXD0A	ASC0 receiver inp./outp. A
P3.1	135		A2		TXD0A	ASC0 transmitter output A
					This pin is sampled at the rising edge of $\overline{\text{PORST}}$. If this pin and the BYPASS input pin are both active, then oscillator bypass mode is entered.	
P3.2	129		A2		SCLK0	SSC0 clock input/output
P3.3	130		A2		MRST0	SSC0 master receive input/ slave transmit output
P3.4	132		A2		MTSR0	SSC0 master transmit output/slave receive input
P3.5	126		A2		SLSO00	SSC0 slave select output 0
P3.6	127		A2		$\overline{\text{SLSO01}}$	SSC0 slave select output 1
P3.7	131		A2		$\overline{\text{SLSI0}}$	SSC0 slave select input
					SLSO02	SSC0 slave select output 2
P3.8	128		A2		SLSO06	SSC0 slave select output 6
					TXD1A	ASC1 transmitter output A
P3.9	138		A2		RXD1A	ASC1 receiver inp./outp. A
P3.10	137		A1		REQ0	External trigger input 0
P3.11	144		A1		REQ1	External trigger input 1
P3.12	143		A2		RXDCAN0	CAN node 0 receiver input
					RXD0B	ASC0 receiver inp./outp. B
P3.13	142		A2		TXDCAN0	CAN node 0 transm. output
					TXD0B	ASC0 transmitter output B
P3.14	134		A2		RXDCAN1	CAN node 1 receiver input
					RXD1B	ASC1 receiver inp./outp. B
P3.15	133		A2		TXDCAN1	CAN node 1 transm. output
					TXD1B	ASC1 transmitter output B

Table 2-1 Pin Definitions and Functions (cont'd)

Symbol	Pins	I/O	Pad Driver Class	Power Supply	Functions
P4		I/O		V_{DDP}	**Port 4 / Hardware Configuration Inputs**
P4.[3:0]					HWCFG[3:0] Boot mode and boot location inputs; inputs are latched with the rising edge of HDRST. During normal operation, Port 4 pins may be used as alternate functions for GPTA or system clock output.
P4.0	86		A1		IN28 / OUT28 / IN52 / OUT52 line of GPTA
P4.1	87		A1		IN29 / OUT29 / IN53 / OUT53 line of GPTA
P4.2	88		A2		IN30 / OUT30 / IN54 / OUT54 line of GPTA
P4.3	90		A2		IN31 / OUT31 / IN55 / OUT55 line of GPTA SYSCLK System Clock Output

Table 2-1 Pin Definitions and Functions (cont'd)

Symbol	Pins	I/O	Pad Driver Class	Power Supply	Functions	
P5		I/O	A2	V_{DDP}	**Port 5** Port 5 is a 16-bit bi-directional general-purpose I/O port. In emulation, it is used as a trace port for OCDS Level 2 debug lines. In normal operation, it is used for GPTA I/O or the MLI0 interface.	
P5.0	1				OCDSDBG0	OCDS L2 Debug Line 0 (Pipeline Status Sig. PS0)
					IN40 / OUT40	line of GPTA
P5.1	2				OCDSDBG1	OCDS L2 Debug Line 1 (Pipeline Status Sig. PS1)
					IN41 / OUT41	line of GPTA
P5.2	3				OCDSDBG2	OCDS L2 Debug Line 2 (Pipeline Status Sig. PS2)
					IN42 / OUT42	line of GPTA
P5.3	4				OCDSDBG3	OCDS L2 Debug Line 3 (Pipeline Status Sig. PS3)
					IN43 / OUT43	line of GPTA
P5.4	5				OCDSDBG4	OCDS L2 Debug Line 4 (Pipeline Status Sig. PS4)
					IN44 / OUT44	line of GPTA
P5.5	6				OCDSDBG5	OCDS L2 Debug Line 5 (Break Qualification Line BRK0)
					IN45 / OUT45	line of GPTA
P5.6	7				OCDSDBG6	OCDS L2 Debug Line 6 (Break Qualification Line BRK1)
					IN46 / OUT46	line of GPTA
P5.7	8				OCDSDBG7	OCDS L2 Debug Line 7 (Break Qualification Line BRK2)
					IN47 / OUT47	line of GPTA

Table 2-1 Pin Definitions and Functions (cont'd)

Symbol	Pins	I/O	Pad Driver Class	Power Supply	Functions	
P5.8	13				OCDSDBG8	OCDS L2 Debug Line 8 (Indirect PC Addr. PC0)
					RDATA0B	MLI0 receive channel data input B
P5.9	14				OCDSDBG9	OCDS L2 Debug Line 9 (Indirect PC Addr. PC1)
					RVALID0B	MLI0 receive channel valid input B
P5.10	15				OCDSDBG10	OCDS L2 Debug Line 10 (Indirect PC Addr. PC2)
					RREADY0B	MLI0 receive channel ready output B
P5.11	16				OCDSDBG11	OCDS L2 Debug Line 11 (Indirect PC Addr. PC3)
					RCLK0B	MLI0 receive channel clock input B
P5.12	17				OCDSDBG12	OCDS L2 Debug Line 12 (Indirect PC Addr. PC04)
					TDATA0	MLI0 transmit channel data output B
P5.13	18				OCDSDBG13	OCDS L2 Debug Line 13 (Indirect PC Addr. PC05)
					TVALID0B	MLI0 transmit channel valid output B
P5.14	19				OCDSDBG14	OCDS L2 Debug Line 14 (Indirect PC Address PC6)
					TREADY0B	MLI0 transmit channel ready input B
P5.15	20				OCDSDBG15	OCDS L2 Debug Line 15 (Indirect PC Address PC7)
					TCLK0	MLI0 transmit channel clock output B

Table 2-1 Pin Definitions and Functions (cont'd)

Symbol	Pins	I/O	Pad Driver Class	Power Supply	Functions
MSC0 Outputs					
			C	V_{DDP}	**LVDS MSC Clock and Data Outputs**[2)]
FCLP0A	157	O			MSC0 Differential Driver Clock Output Positive A
FCLN0	156	O			MSC0 Differential Driver Clock Output Negative
SOP0A	159	O			MSC0 Differential Driver Serial Data Output Positive A
SON0	158	O			MSC0 Differential Driver Serial Data Output Negative

Table 2-1 Pin Definitions and Functions (cont'd)

Symbol	Pins	I/O	Pad Driver Class	Power Supply	Functions
Analog Inputs					
AN[35:0]		I	D	–	**Analog Input Port** The Analog Input Port provides altogether 36 analog input lines to ADC0 and FADC. AN[31:0]: ADC0 analog inputs [31:0] AN[35:32]: FADC analog differential inputs
AN0	67				Analog input 0
AN1	66				Analog input 1
AN2	65				Analog input 2
AN3	64				Analog input 3
AN4	63				Analog input 4
AN5	62				Analog input 5
AN6	61				Analog input 6
AN7	36				Analog input 7
AN8	60				Analog input 8
AN9	59				Analog input 9
AN10	58				Analog input 10
AN11	57				Analog input 11
AN12	56				Analog input 12
AN13	55				Analog input 13
AN14	50				Analog input 14
AN15	49				Analog input 15
AN16	48				Analog input 16
AN17	47				Analog input 17
AN18	46				Analog input 18
AN19	45				Analog input 19
AN20	44				Analog input 20
AN21	43				Analog input 21
AN22	42				Analog input 22
AN23	41				Analog input 23
AN24	40				Analog input 24
AN25	39				Analog input 25
AN26	38				Analog input 26
AN27	37				Analog input 27
AN28	35				Analog input 28
AN29	34				Analog input 29
AN30	33				Analog input 30

Table 2-1 Pin Definitions and Functions (cont'd)

Symbol	Pins	I/O	Pad Driver Class	Power Supply	Functions
AN31 AN32 AN33 AN34 AN35	32 31 30 29 28	I	D	–	Analog input 31 Analog input 32 Analog input 33 Analog input 34 Analog input 35
System I/O					
TRST	114	I	A2[1]	V_{DDP}	**JTAG Module Reset/Enable Input**
TCK	115	I	A2[1]	V_{DDP}	**JTAG Module Clock Input**
TDI	111	I	A1[1]	V_{DDP}	**JTAG Module Serial Data Input**
TDO	113	O	A2	V_{DDP}	**JTAG Module Serial Data Output**
TMS	112	I	A2[1]	V_{DDP}	**JTAG Module State Machine Control Input**
BRKIN	117	I/O	A3	V_{DDP}	**OCDS Break Input (Alternate Output)[2][3]**
BRK OUT	116	I/O	A3	V_{DDP}	**OCDS Break Output (Alternate Input)[2][3]**
TRCLK	9	O	A4	V_{DDP}	**Trace Clock for OCDS_L2 Lines[2]**
NMI	120	I	A2[4][5]	V_{DDP}	**Non-Maskable Interrupt Input**
HDRST	122	I/O	A2[6]	V_{DDP}	**Hardware Reset Input / Reset Indication Output**
PORST[7]	121	I	A2[4]	V_{DDP}	**Power-on Reset Input**
BYPASS	119	I	A1[1]	V_{DDP}	**PLL Clock Bypass Select Input** This input has to be held stable during power-on resets. With BYPASS = 1, the spike filters in the HDRST, PORST and NMI inputs are switched off.
TEST MODE	118	I	A2[4][8]	V_{DDP}	**Test Mode Select Input** For normal operation of the TC1762, this pin should be connected to high level.
XTAL1 **XTAL2**	102 103	I O	n.a.	V_{DDOSC}	**Oscillator/PLL/Clock Generator Input/Output Pins**
N.C.	21, 89	–	–	–	**Not Connected** These pins are reserved for future extension and must not be connected externally.

Table 2-1 Pin Definitions and Functions (cont'd)

Symbol	Pins	I/O	Pad Driver Class	Power Supply	Functions
Power Supplies					
V_{DDM}	54	–	–	–	**ADC Analog Part Power Supply (3.3 V)**
V_{SSM}	53	–	–	–	**ADC Analog Part Ground for V_{DDM}**
V_{DDMF}	24	–	–	–	**FADC Analog Part Power Supply (3.3 V)**
V_{SSMF}	25	–	–	–	**FADC Analog Part Ground for V_{DDMF}**
V_{DDAF}	23	–	–	–	**FADC Analog Part Logic Power Supply (1.5 V)**
V_{SSAF}	22	–	–	–	**FADC Analog Part Logic Ground for V_{DDAF}**
V_{AREF0}	52	–	–	–	**ADC Reference Voltage**
V_{AGND0}	51	–	–	–	**ADC Reference Ground**
V_{FAREF}	26	–	–	–	**FADC Reference Voltage**
V_{FAGND}	27	–	–	–	**FADC Reference Ground**
V_{DDOSC}	105	–	–	–	**Main Oscillator and PLL Power Supply (1.5 V)**
V_{DDOSC3}	106	–	–	–	**Main Oscillator Power Supply (3.3 V)**
V_{SSOSC}	104	–	–	–	**Main Oscillator and PLL Ground**
V_{DDFL3}	141	–	–	–	**Power Supply for Flash (3.3 V)**
V_{DD}	10, 68, 84, 99, 123, 153, 170	–	–	–	**Core Power Supply (1.5 V)**