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32-Bit

Microcontroller

TC1782

32-Bit Single-Chip Microcontroller

Data Sheet

V 1.4.1 2014-05

Microcontrollers

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Microcontrollers

Table of Contents

1 Summary of Features

The **SAK-TC1782F-320F180HR** / **SAK-TC1782F-320F180HL** has the following features:

- High-performance 32-bit super-scalar TriCore V1.3.1 CPU with 4-stage pipeline
  - Superior real-time performance
  - Strong bit handling
  - Fully integrated DSP capabilities
  - Single precision Floating Point Unit (FPU)
  - 180 MHz operation at full temperature range
- 32-bit Peripheral Control Processor with single cycle instruction (PCP2)
  - 16 Kbyte Parameter Memory (PRAM)
  - 32 Kbyte Code Memory (CMEM)
  - 180 MHz operation at full temperature range
- Multiple on-chip memories
  - 2.5 Mbyte Program Flash Memory (PFLASH) with ECC
  - 128 Kbyte Data Flash Memory (DFLASH) usable for EEPROM emulation
  - 128 Kbyte Data Memory (LDRAM)
  - Instruction Cache: up to 16 Kbyte (ICACHE, configurable)
  - 40 Kbyte Code Scratchpad Memory (SPRAM)
  - Data Cache: up to 4 Kbyte (DCACHE, configurable)
  - 8 Kbyte Overlay Memory (OVRAM)
  - 16 Kbyte BootROM (BROM)
- 16-Channel DMA Controller
- Sophisticated interrupt system with 2×255 hardware priority arbitration levels serviced by CPU or PCP2
- High performing on-chip bus structure
  - 64-bit Local Memory Buses between CPU, Flash and Data Memory
  - 32-bit System Peripheral Bus (SPB) for on-chip peripheral and functional units
  - One bus bridge (LFI Bridge)
- Versatile On-chip Peripheral Units
  - Two Asynchronous/Synchronous Serial Channels (ASC) with baud rate generator, parity, framing and overrun error detection
  - Three High-Speed Synchronous Serial Channels (SSC) with programmable data length and shift direction
  - One serial Micro Second Bus interface (MSC) for serial port expansion to external power devices
  - One High-Speed Micro Link interface (MLI) for serial inter-processor communication
  - One MultiCAN Module with 3 CAN nodes and 128 free assignable message objects for high efficiency data handling via FIFO buffering and gateway data transfer (one CAN node supports TTCAN functionality)
  - One FlexRay™ module with 2 channels (E-Ray).

  - One General Purpose Timer Array Module (GPTA) with additional Local Timer Cell Array (LTCA2) providing a powerful set of digital signal filtering and timer functionality to realize autonomous and complex Input/Output management
- 32 analog input lines for ADC
  - 2 independent kernels (ADC0 and ADC1)
  - Analog supply voltage range from 3.3 V to 5 V (single supply)
- 4 different FADC input channels
  - channels with impedance control and overlaid with ADC1 inputs
  - Extreme fast conversion, 21 cycles of f_{FADC} clock
  - 10-bit A/D conversion (higher resolution can be achieved by averaging of consecutive conversions in digital data reduction filter)
- 86 digital general purpose I/O lines (GPIO), 4 input lines
- Digital I/O ports with 3.3 V capability
- On-chip debug support for OCDS Level 1 (CPU, PCP, DMA, On Chip Bus)
- Dedicated Emulation Device chip available (TC1782ED)
  - multi-core debugging, real time tracing, and calibration
  - four/five wire JTAG (IEEE 1149.1) or two wire DAP (Device Access Port) interface
- Power Management System
- Clock Generation Unit with PLL

Summary of Features

The **SAK-TC1782N-320F180HR** / **SAK-TC1782N-320F180HL** has the following features:

- High-performance 32-bit super-scalar TriCore V1.3.1 CPU with 4-stage pipeline
  - Superior real-time performance
  - Strong bit handling
  - Fully integrated DSP capabilities
  - Single precision Floating Point Unit (FPU)
  - 180 MHz operation at full temperature range
- 32-bit Peripheral Control Processor with single cycle instruction (PCP2)
  - 16 Kbyte Parameter Memory (PRAM)
  - 32 Kbyte Code Memory (CMEM)
  - 180 MHz operation at full temperature range
- Multiple on-chip memories
  - 2.5 Mbyte Program Flash Memory (PFLASH) with ECC
  - 128 Kbyte Data Flash Memory (DFLASH) usable for EEPROM emulation
  - 128 Kbyte Data Memory (LDRAM)
  - Instruction Cache: up to 16 Kbyte (ICACHE, configurable)
  - 40 Kbyte Code Scratchpad Memory (SPRAM)
  - Data Cache: up to 4 Kbyte (DCACHE, configurable)
  - 8 Kbyte Overlay Memory (OVRAM)
  - 16 Kbyte BootROM (BROM)
- 16-Channel DMA Controller
- Sophisticated interrupt system with 2×255 hardware priority arbitration levels serviced by CPU or PCP2
- High performing on-chip bus structure
  - 64-bit Local Memory Buses between CPU, Flash and Data Memory
  - 32-bit System Peripheral Bus (SPB) for on-chip peripheral and functional units
  - One bus bridge (LFI Bridge)
- Versatile On-chip Peripheral Units
  - Two Asynchronous/Synchronous Serial Channels (ASC) with baud rate generator, parity, framing and overrun error detection
  - Three High-Speed Synchronous Serial Channels (SSC) with programmable data length and shift direction
  - One serial Micro Second Bus interface (MSC) for serial port expansion to external power devices
  - One High-Speed Micro Link interface (MLI) for serial inter-processor communication
  - One MultiCAN Module with 3 CAN nodes and 128 free assignable message objects for high efficiency data handling via FIFO buffering and gateway data transfer (one CAN node supports TTCAN functionality)

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- 32 analog input lines for ADC
  - 2 independent kernels (ADC0 and ADC1)
  - Analog supply voltage range from 3.3 V to 5 V (single supply)
- 4 different FADC input channels
  - channels with impedance control and overlaid with ADC1 inputs
  - Extreme fast conversion, 21 cycles of f_{FADC} clock
  - 10-bit A/D conversion (higher resolution can be achieved by averaging of consecutive conversions in digital data reduction filter)
- 86 digital general purpose I/O lines (GPIO), 4 input lines
- Digital I/O ports with 3.3 V capability
- On-chip debug support for OCDS Level 1 (CPU, PCP, DMA, On Chip Bus)
- Dedicated Emulation Device chip available (TC1782ED)
  - multi-core debugging, real time tracing, and calibration
  - four/five wire JTAG (IEEE 1149.1) or two wire DAP (Device Access Port) interface
- Power Management System
- Clock Generation Unit with PLL

The **SAK-TC1782N-256F133HR** / **SAK-TC1782N-256F133HL** has the following features:

- High-performance 32-bit super-scalar TriCore V1.3.1 CPU with 4-stage pipeline
  - Superior real-time performance
  - Strong bit handling
  - Fully integrated DSP capabilities
  - Single precision Floating Point Unit (FPU)
  - 133 MHz operation at full temperature range
- 32-bit Peripheral Control Processor with single cycle instruction (PCP2)
  - 16 Kbyte Parameter Memory (PRAM)
  - 32 Kbyte Code Memory (CMEM)
  - 133 MHz operation at full temperature range
- Multiple on-chip memories
  - 2 Mbyte Program Flash Memory (PFLASH) with ECC
  - 128 Kbyte Data Flash Memory (DFLASH) usable for EEPROM emulation
  - 128 Kbyte Data Memory (LDRAM)
  - Instruction Cache: up to 16 Kbyte (ICACHE, configurable)
  - 40 Kbyte Code Scratchpad Memory (SPRAM)
  - Data Cache: up to 4 Kbyte (DCACHE, configurable)
  - 8 Kbyte Overlay Memory (OVRAM)
  - 16 Kbyte BootROM (BROM)
- 16-Channel DMA Controller
- Sophisticated interrupt system with 2×255 hardware priority arbitration levels serviced by CPU or PCP2
- High performing on-chip bus structure
  - 64-bit Local Memory Buses between CPU, Flash and Data Memory
  - 32-bit System Peripheral Bus (SPB) for on-chip peripheral and functional units
  - One bus bridge (LFI Bridge)
- Versatile On-chip Peripheral Units
  - Two Asynchronous/Synchronous Serial Channels (ASC) with baud rate generator, parity, framing and overrun error detection
  - Three High-Speed Synchronous Serial Channels (SSC) with programmable data length and shift direction
  - One serial Micro Second Bus interface (MSC) for serial port expansion to external power devices
  - One High-Speed Micro Link interface (MLI) for serial inter-processor communication
  - One MultiCAN Module with 3 CAN nodes and 128 free assignable message objects for high efficiency data handling via FIFO buffering and gateway data transfer (one CAN node supports TTCAN functionality)

  - One General Purpose Timer Array Module (GPTA) with additional Local Timer Cell Array (LTCA2) providing a powerful set of digital signal filtering and timer functionality to realize autonomous and complex Input/Output management
- 32 analog input lines for ADC
  - 2 independent kernels (ADC0 and ADC1)
  - Analog supply voltage range from 3.3 V to 5 V (single supply)
- 4 different FADC input channels
  - channels with impedance control and overlaid with ADC1 inputs
  - Extreme fast conversion, 21 cycles of f_{FADC} clock
  - 10-bit A/D conversion (higher resolution can be achieved by averaging of consecutive conversions in digital data reduction filter)
- 86 digital general purpose I/O lines (GPIO), 4 input lines
- Digital I/O ports with 3.3 V capability
- On-chip debug support for OCDS Level 1 (CPU, PCP, DMA, On Chip Bus)
- Dedicated Emulation Device chip available (TC1782ED)
  - multi-core debugging, real time tracing, and calibration
  - four/five wire JTAG (IEEE 1149.1) or two wire DAP (Device Access Port) interface
- Power Management System
- Clock Generation Unit with PLL

Summary of Features

The **SAK-TC1782F-320F160HR** / **SAK-TC1782F-320F160HL** has the following features:

- High-performance 32-bit super-scalar TriCore V1.3.1 CPU with 4-stage pipeline
  - Superior real-time performance
  - Strong bit handling
  - Fully integrated DSP capabilities
  - Single precision Floating Point Unit (FPU)
  - 160 MHz operation at full temperature range
- 32-bit Peripheral Control Processor with single cycle instruction (PCP2)
  - 16 Kbyte Parameter Memory (PRAM)
  - 32 Kbyte Code Memory (CMEM)
  - 160 MHz operation at full temperature range
- Multiple on-chip memories
  - 2.5 Mbyte Program Flash Memory (PFLASH) with ECC
  - 128 Kbyte Data Flash Memory (DFLASH) usable for EEPROM emulation
  - 128 Kbyte Data Memory (LDRAM)
  - Instruction Cache: up to 16 Kbyte (ICACHE, configurable)
  - 40 Kbyte Code Scratchpad Memory (SPRAM)
  - Data Cache: up to 4 Kbyte (DCACHE, configurable)
  - 8 Kbyte Overlay Memory (OVRAM)
  - 16 Kbyte BootROM (BROM)
- 16-Channel DMA Controller
- Sophisticated interrupt system with 2×255 hardware priority arbitration levels serviced by CPU or PCP2
- High performing on-chip bus structure
  - 64-bit Local Memory Buses between CPU, Flash and Data Memory
  - 32-bit System Peripheral Bus (SPB) for on-chip peripheral and functional units
  - One bus bridge (LFI Bridge)
- Versatile On-chip Peripheral Units
  - Two Asynchronous/Synchronous Serial Channels (ASC) with baud rate generator, parity, framing and overrun error detection
  - Three High-Speed Synchronous Serial Channels (SSC) with programmable data length and shift direction
  - One serial Micro Second Bus interface (MSC) for serial port expansion to external power devices
  - One High-Speed Micro Link interface (MLI) for serial inter-processor communication
  - One MultiCAN Module with 3 CAN nodes and 128 free assignable message objects for high efficiency data handling via FIFO buffering and gateway data transfer (one CAN node supports TTCAN functionality)
  - One FlexRay™ module with 2 channels (E-Ray).

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  - Extreme fast conversion, 21 cycles of f_{FADC} clock
  - 10-bit A/D conversion (higher resolution can be achieved by averaging of consecutive conversions in digital data reduction filter)
- 86 digital general purpose I/O lines (GPIO), 4 input lines
- Digital I/O ports with 3.3 V capability
- On-chip debug support for OCDS Level 1 (CPU, PCP, DMA, On Chip Bus)
- Dedicated Emulation Device chip available (TC1782ED)
  - multi-core debugging, real time tracing, and calibration
  - four/five wire JTAG (IEEE 1149.1) or two wire DAP (Device Access Port) interface
- Power Management System
- Clock Generation Unit with PLL

The **SAK-TC1782N-320F160HR** / **SAK-TC1782N-320F160HL** has the following features:

- High-performance 32-bit super-scalar TriCore V1.3.1 CPU with 4-stage pipeline
  - Superior real-time performance
  - Strong bit handling
  - Fully integrated DSP capabilities
  - Single precision Floating Point Unit (FPU)
  - 160 MHz operation at full temperature range
- 32-bit Peripheral Control Processor with single cycle instruction (PCP2)
  - 16 Kbyte Parameter Memory (PRAM)
  - 32 Kbyte Code Memory (CMEM)
  - 160 MHz operation at full temperature range
- Multiple on-chip memories
  - 2.5 Mbyte Program Flash Memory (PFLASH) with ECC
  - 128 Kbyte Data Flash Memory (DFLASH) usable for EEPROM emulation
  - 128 Kbyte Data Memory (LDRAM)
  - Instruction Cache: up to 16 Kbyte (ICACHE, configurable)
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  - Data Cache: up to 4 Kbyte (DCACHE, configurable)
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  - 16 Kbyte BootROM (BROM)
- 16-Channel DMA Controller
- Sophisticated interrupt system with 2×255 hardware priority arbitration levels serviced by CPU or PCP2
- High performing on-chip bus structure
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  - One bus bridge (LFI Bridge)
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  - One General Purpose Timer Array Module (GPTA) with additional Local Timer Cell Array (LTCA2) providing a powerful set of digital signal filtering and timer functionality to realize autonomous and complex Input/Output management
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- On-chip debug support for OCDS Level 1 (CPU, PCP, DMA, On Chip Bus)
- Dedicated Emulation Device chip available (TC1782ED)
  - multi-core debugging, real time tracing, and calibration
  - four/five wire JTAG (IEEE 1149.1) or two wire DAP (Device Access Port) interface
- Power Management System
- Clock Generation Unit with PLL

Ordering Information

The ordering code for Infineon microcontrollers provides an exact reference to the required product. This ordering code identifies:

- The derivative itself, i.e. its function set, the temperature range, and the supply voltage
- The package and the type of delivery.

For the available ordering codes for the TC1782 please refer to the **"Product Catalog Microcontrollers"**, which summarizes all available microcontroller variants.

This document describes the derivatives of the device.The **Table 1** enumerates these derivatives and summarizes the differences.

Table 1 TC1782 Derivative Synopsis

Derivative	Ambient Temperature Range	Package
SAK-TC1782F-320F180HR	T_A = -40°C to +125°C	PG-LQFP-176-20
SAK-TC1782F-320F180HL	T_A = -40°C to +125°C	PG-LQFP-176-10
SAK-TC1782N-320F180HR	T_A = -40°C to +125°C	PG-LQFP-176-20
SAK-TC1782N-320F180HL	T_A = -40°C to +125°C	PG-LQFP-176-10
SAK-TC1782N-256F133HR	T_A = -40°C to +125°C	PG-LQFP-176-20
SAK-TC1782N-256F133HL	T_A = -40°C to +125°C	PG-LQFP-176-10
SAK-TC1782F-320F160HR	T_A = -40°C to +125°C	PG-LQFP-176-20
SAK-TC1782F-320F160HL	T_A = -40°C to +125°C	PG-LQFP-176-10
SAK-TC1782N-320F160HR	T_A = -40°C to +125°C	PG-LQFP-176-20
SAK-TC1782N-320F160HL	T_A = -40°C to +125°C	PG-LQFP-176-10

2 System Overview of the TC1782

The TC1782 combines three powerful technologies within one silicon die, achieving new levels of power, speed, and economy for embedded applications:

- Reduced Instruction Set Computing (RISC) processor architecture
- Digital Signal Processing (DSP) operations and addressing modes
- On-chip memories and peripherals

DSP operations and addressing modes provide the computational power necessary to efficiently analyze complex real-world signals. The RISC load/store architecture provides high computational bandwidth with low system cost. On-chip memory and peripherals are designed to support even the most demanding high-bandwidth real-time embedded control-systems tasks.

Additional high-level features of the TC1782 include:

- Efficient memory organization: instruction and data scratch memories, caches
- Serial communication interfaces – flexible synchronous and asynchronous modes
- Peripheral Control Processor – standalone data operations and interrupt servicing
- DMA Controller – DMA operations and interrupt servicing
- General-purpose timers
- High-performance on-chip buses
- On-chip debugging and emulation facilities
- Flexible interconnections to external components
- Flexible power-management

The TC1782 is a high-performance microcontroller with TriCore CPU, program and data memories, buses, bus arbitration, an interrupt controller, a peripheral control processor and a DMA controller and several on-chip peripherals. The TC1782 is designed to meet the needs of the most demanding embedded control systems applications where the competing issues of price/performance, real-time responsiveness, computational power, data bandwidth, and power consumption are key design elements.

The TC1782 offers several versatile on-chip peripheral units such as serial controllers, timer units, and Analog-to-Digital converters. Within the TC1782, all these peripheral units are connected to the TriCore CPU/system via the Flexible Peripheral Interconnect (FPI) Bus and the Local Memory Bus (LMB). Several I/O lines on the TC1782 ports are reserved for these peripheral units to communicate with the external world.

2.1 Block Diagrams

Figure 1 shows the block diagram of the **SAK-TC1782-320F180HR / SAK-TC1782-320F180HL / SAK-TC1782-320F160HR / SAK-TC1782-320F160HL**.

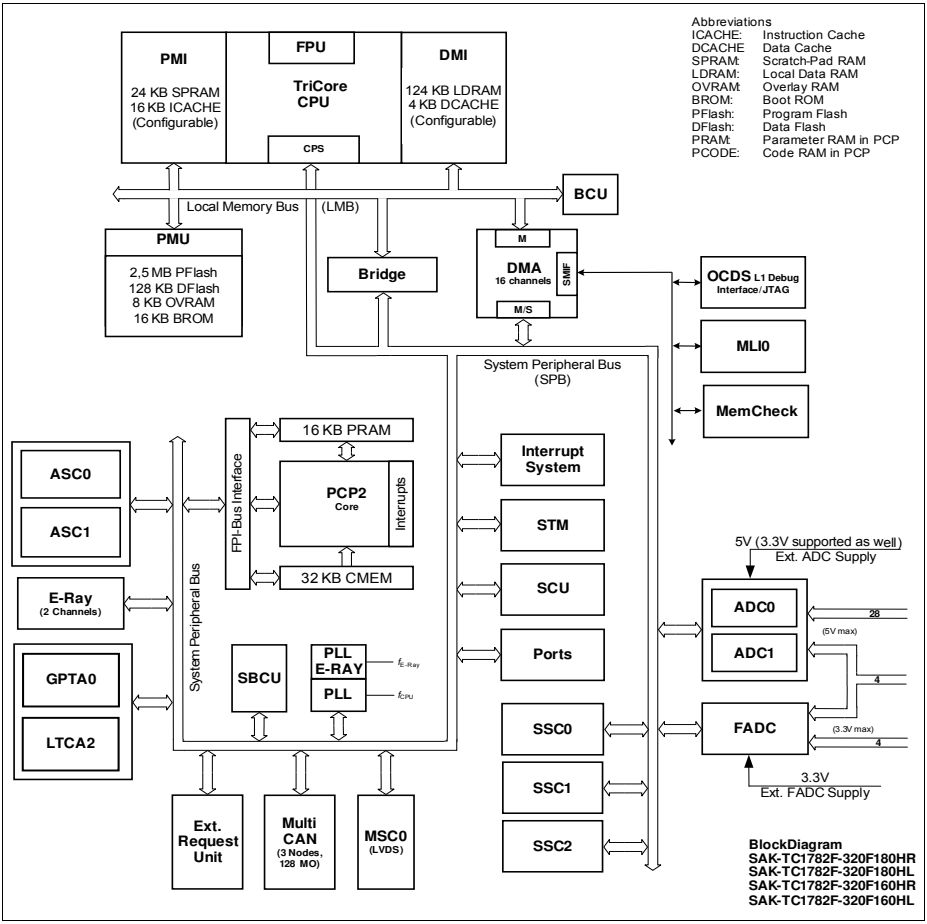

Figure 1 SAK-TC1782-320F180HR / SAK-TC1782-320F180HL / SAK-TC1782-320F160HR / SAK-TC1782-320F160HL Block Diagram

Figure 2 shows the block diagram of the **SAK-TC1782N-320F180HR** / **SAK-TC1782N-320F180HL** / **SAK-TC1782N-320F160HR** / **SAK-TC1782N-320F160HL**.

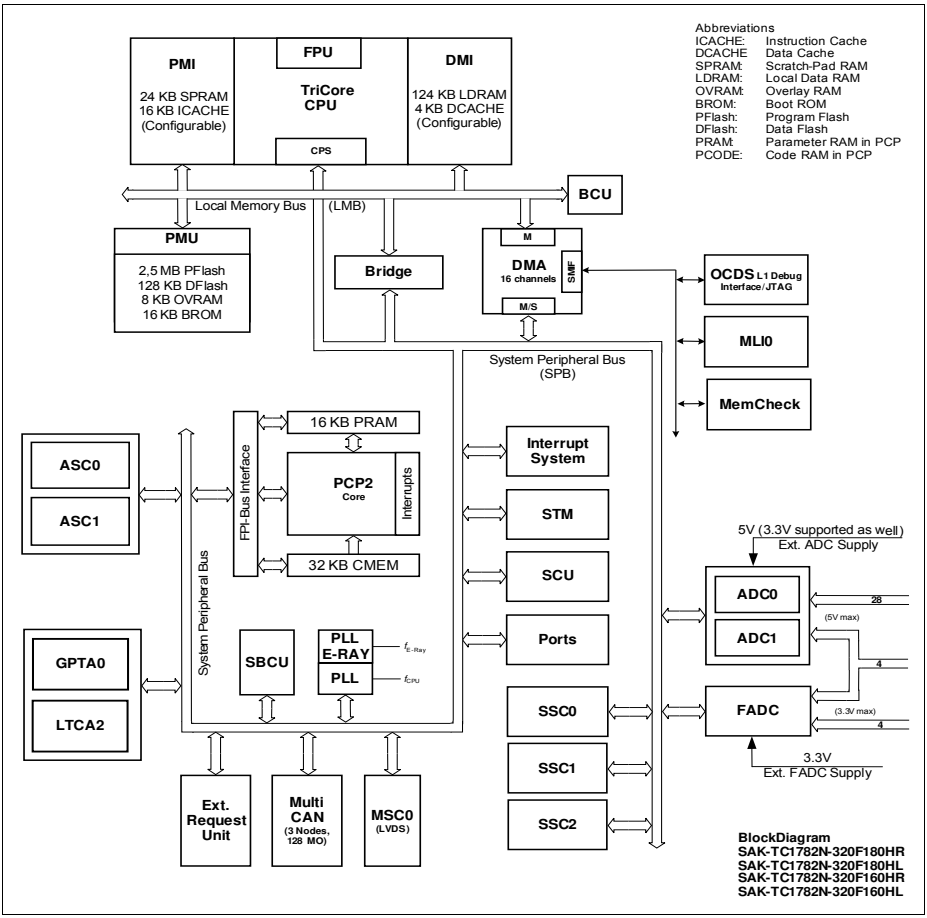

Figure 2 SAK-TC1782N-320F180HR / SAK-TC1782N-320F180HL / SAK-TC1782N-320F160HR / SAK-TC1782N-320F160HL / Block Diagram

Figure 3 shows the block diagram of the **SAK-TC1782N-256F133HR** / **SAK-TC1782N-256F133HL**.

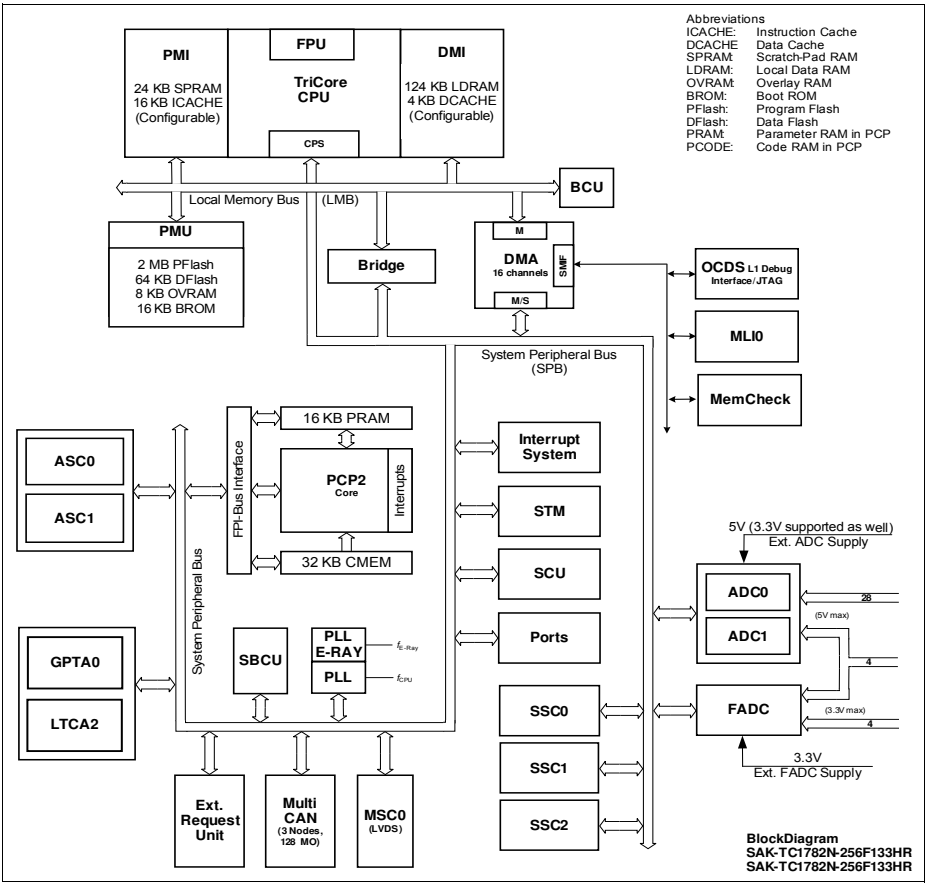

Figure 3 SAK-TC1782N-256F133HR / SAK-TC1782N-256F133HL Block Diagram

3 Pinning

Figure 4 is showing the TC1782 Logic Symbol.

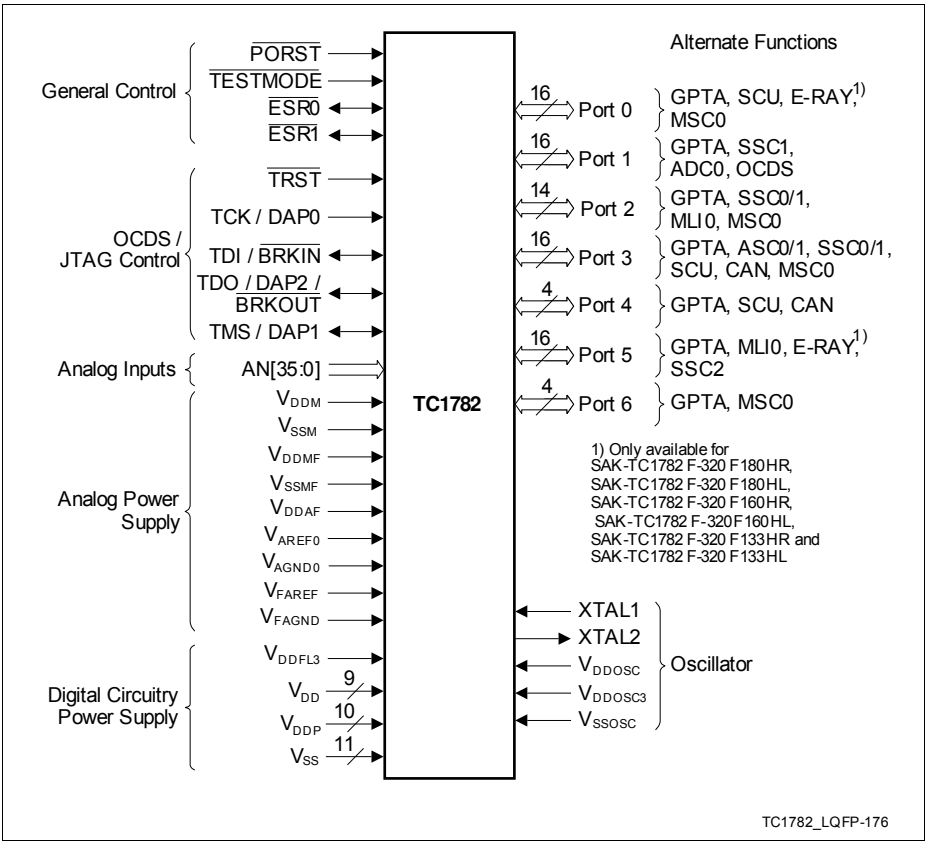

Figure 4 TC1782 Logic Symbol

3.1 TC1782 Pin Configuration

This chapter shows the pin configuration of the TC1782 package PG-LQFP-176-10 / PG-LQFP-176-20.

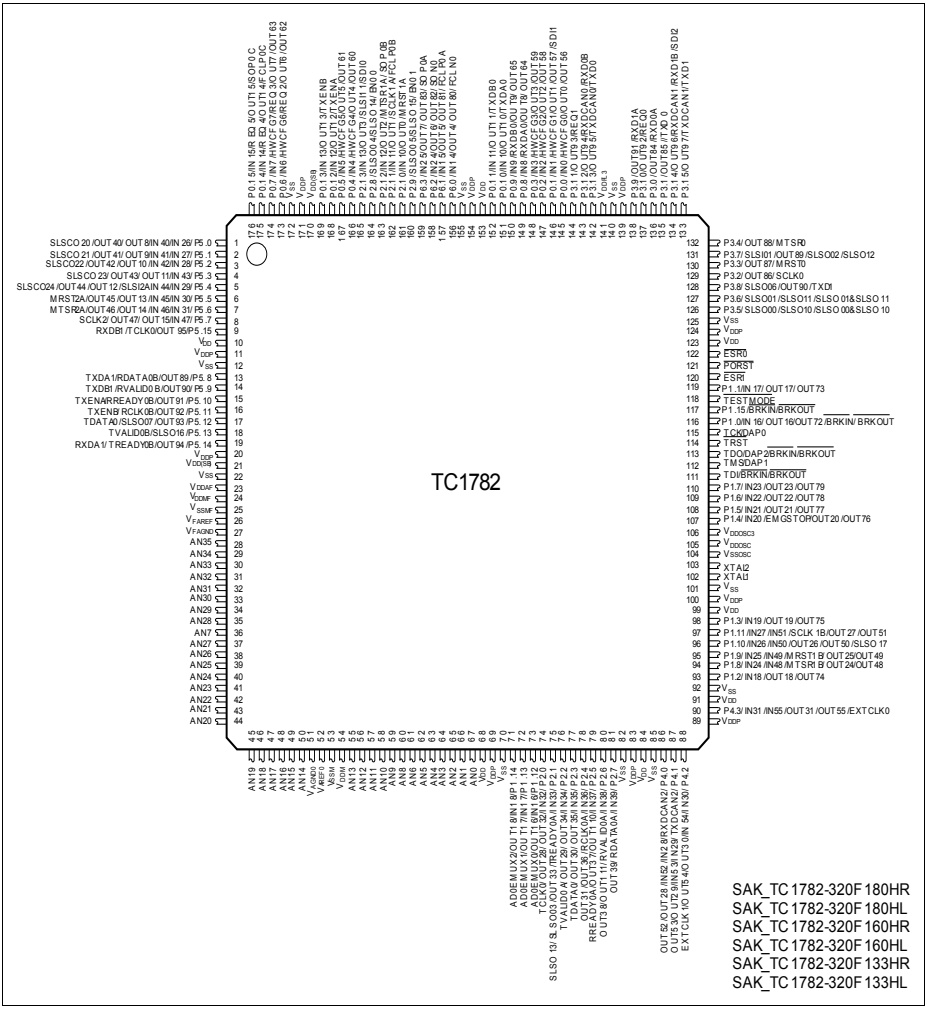

Figure 5 SAK-TC1782F-320F180HR / SAK-TC1782F-320F180HL / SAK-TC1782F-320F160HR / SAK-TC1782F-320F160HL Pinning

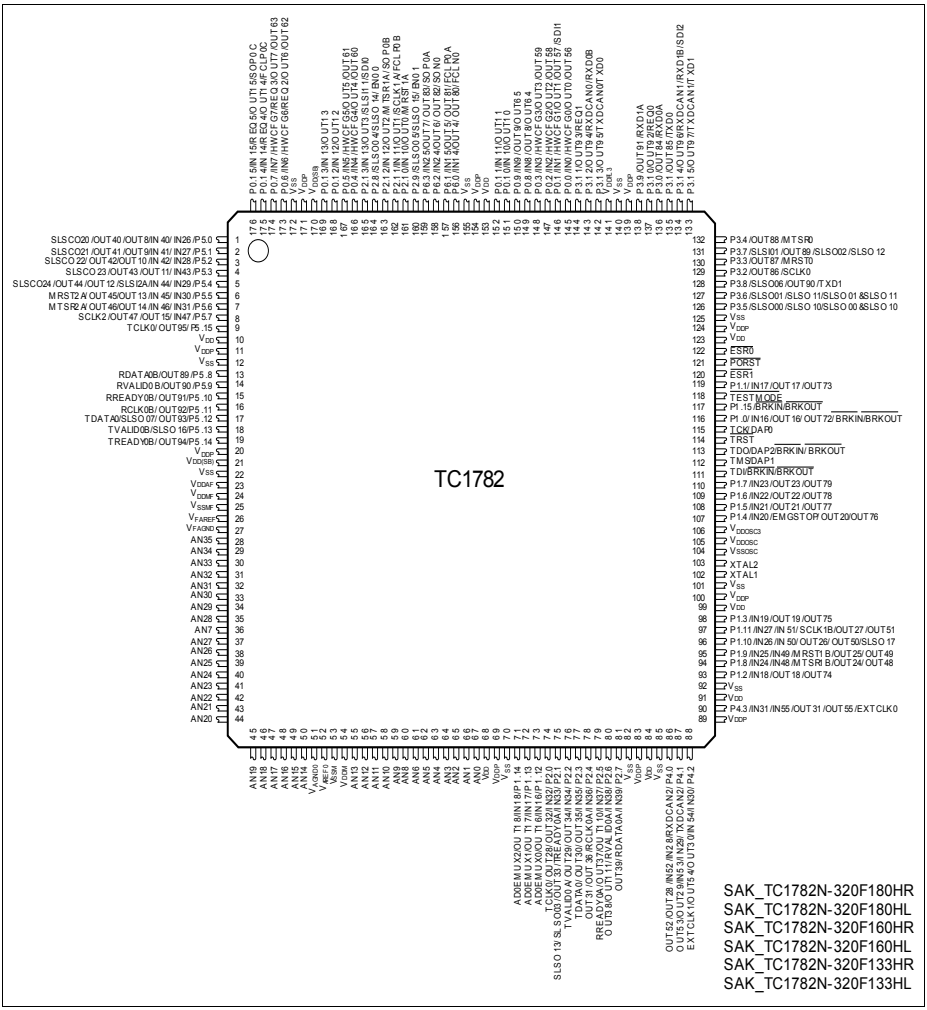

Figure 6 SAK-TC1782N-320F180HR / SAK-TC1782N-320F180HL / SAK-TC1782N-320F160HR / SAK-TC1782N-320F160HL / SAK-TC1782N-256F133HR / SAK-TC1782N-256F133HL / Pinning