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32-Bit

Microcontroller

TC1793

32-Bit Single-Chip Microcontroller

Data Sheet

V 1.2 2014-05

Microcontrollers

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V 1.2 2014-05

Microcontrollers

Table of Contents

1 Summary of Features

The **SAK-TC1793F-512F270EF** has the following features:

- High-performance 32-bit super-scalar TriCore V1.6 CPU with 6-stage pipeline
  - Superior real-time performance
  - Strong bit handling
  - Fully integrated DSP capabilities
  - Multiply-accumulate unit able to sustain 2 MAC operations per cycle
  - Fully pipelined Floating point unit (FPU)
  - 270 MHz operation at full temperature range
- 32-bit Peripheral Control Processor with single cycle instruction (PCP2)
  - 16 Kbyte Parameter Memory (PRAM)
  - 32 Kbyte Code Memory (CMEM)
  - 200 MHz operation at full temperature range
- Multiple on-chip memories
  - 4 Mbyte Program Flash Memory (PFLASH) with ECC
  - 192 Kbyte Data Flash Memory (DFLASH) usable for EEPROM emulation
  - 2 x 8 Kbyte Key Flash
  - 128 Kbyte Data Scratch-Pad RAM (DSPR)
  - 16 Kbyte Instruction Cache (ICACHE)
  - 32 Kbyte Instruction Scratch-Pad RAM (PSPR)
  - 16 Kbyte Data Cache (DACHE)
  - 128 Kbyte Memory (SRAM)
  - 16 Kbyte BootROM (BROM)
- 16-Channel DMA Controller
- 8-Channel Safe DMA (SDMA) Controller
- Sophisticated interrupt system with 2×255 hardware priority arbitration levels serviced by CPU or PCP2
- High performing on-chip bus structure
  - 64-bit Cross Bar Interconnect between CPU, Flash and Data Memory
  - 32-bit System Peripheral Bus (SPB) for on-chip peripheral and functional units
  - One bus bridge (SFI Bridge)
- Versatile On-chip Peripheral Units
  - Two Asynchronous/Synchronous Serial Channels (ASC) with baud rate generator, parity, framing and overrun error detection
  - Four High-Speed Synchronous Serial Channels (SSC) with programmable data length and shift direction
  - Four SSC Guardian (SSCG) modules, one for each SSC
  - Two serial Micro Second Bus interfaces (MSC) for serial port expansion to external power devices
  - Two High-Speed Micro Link interfaces (MLI) for serial inter-processor communication

  - One External Bus Interface (EBU) supporting different memories: asynchronous memories e.g. SRAM, peripheral devices; synchronous devices e.g. burst NOR flash, PSRAM; and DDR NOR flash e.g. LPDDR-NVM (Jedec 42.2), ONFI 2.0 (limited frequency at 1.8 V I/O supply)
  - One MultiCAN Module with 4 CAN nodes and 128 free assignable message objects for high efficiency data handling via FIFO buffering and gateway data transfer (one CAN node supports TTCAN functionality)
  - One FlexRay™ module with 2 channels (E-Ray).
  - Two General Purpose Timer Array Modules (GPTA) with additional Local Timer Cell Array (LTCA2) providing a powerful set of digital signal filtering and timer functionality to realize autonomous and complex Input/Output management
  - Two Capture / Compare 6 modules
  - Two General Purpose 12 Timer Units (GPT120 and GPT121)
- 44 analog input lines for ADC
  - 4 independent kernels (ADC0, ADC1, and ADC2)
  - Analog supply voltage range from 3.3 V to 5 V (single supply)
- 4 different FADC input channels
  - channels with impedance control and overlaid with ADC1 inputs
  - Extreme fast conversion, 21 cycles of f_{FADC} clock
  - 10-bit A/D conversion (higher resolution can be achieved by averaging of consecutive conversions in digital data reduction filter)
- 8 digital input lines for SENT
  - communication according to the SENT specification J2716 FEB2008
- 221 digital general purpose I/O lines (GPIO)
- Digital I/O ports with 3.3 V capability
- On-chip debug support for OCDS Level 1 (CPU, PCP, DMA, On Chip Buses)
- Dedicated Emulation Device chip available (TC1793ED)
  - multi-core debugging, real time tracing, and calibration
  - four/five wire JTAG (IEEE 1149.1) or two wire DAP (Device Access Port) interface
- Power Management System
- Clock Generation Unit with PLL and PLL_ERAY
- Flexible CRC Engine (FCE)
  - IEEE 802.3 CRC32 ethernet polynomial: 0x82608EDB (CRC kernel 0)
  - CRC32C Castagnoli: 0xD419CC15 (CRC kernel 1)

The **SAK-TC1793F-512F200EB** / **SAK-TC1793F-512F200EF** has the following features:

- High-performance 32-bit super-scalar TriCore V1.6 CPU with 6-stage pipeline
  - Superior real-time performance
  - Strong bit handling
  - Fully integrated DSP capabilities
  - Multiply-accumulate unit able to sustain 2 MAC operations per cycle
  - Fully pipelined Floating point unit (FPU)

  - 200 MHz operation at full temperature range
- 32-bit Peripheral Control Processor with single cycle instruction (PCP2)
  - 16 Kbyte Parameter Memory (PRAM)
  - 32 Kbyte Code Memory (CMEM)
  - 200 MHz operation at full temperature range
- Multiple on-chip memories
  - 4 Mbyte Program Flash Memory (PFLASH) with ECC
  - 192 Kbyte Data Flash Memory (DFLASH) usable for EEPROM emulation
  - 2 x 8 Kbyte Key Flash
  - 128 Kbyte Data Scratch-Pad RAM (DSPR)
  - 16 Kbyte Instruction Cache (ICACHE)
  - 32 Kbyte Instruction Scratch-Pad RAM (PSPR)
  - 16 Kbyte Data Cache (DACHE)
  - 128 Kbyte Memory (SRAM)
  - 16 Kbyte BootROM (BROM)
- 16-Channel DMA Controller
- 8-Channel Safe DMA (SDMA) Controller
- Sophisticated interrupt system with 2×255 hardware priority arbitration levels serviced by CPU or PCP2
- High performing on-chip bus structure
  - 64-bit Cross Bar Interconnect between CPU, Flash and Data Memory
  - 32-bit System Peripheral Bus (SPB) for on-chip peripheral and functional units
  - One bus bridge (SFI Bridge)
- Versatile On-chip Peripheral Units
  - Two Asynchronous/Synchronous Serial Channels (ASC) with baud rate generator, parity, framing and overrun error detection
  - Four High-Speed Synchronous Serial Channels (SSC) with programmable data length and shift direction
  - Four SSC Guardian (SSCG) modules, one for each SSC
  - Two serial Micro Second Bus interfaces (MSC) for serial port expansion to external power devices
  - Two High-Speed Micro Link interfaces (MLI) for serial inter-processor communication
  - One External Bus Interface (EBU) supporting different memories: asynchronous memories e.g. SRAM, peripheral devices; synchronous devices e.g. burst NOR flash, PSRAM; and DDR NOR flash e.g. LPDDR-NVM (Jedec 42.2), ONFI 2.0 (limited frequency at 1.8 V I/O supply)
  - One MultiCAN Module with 4 CAN nodes and 128 free assignable message objects for high efficiency data handling via FIFO buffering and gateway data transfer (one CAN node supports TTCAN functionality)
  - One FlexRay™ module with 2 channels (E-Ray).

  - Two General Purpose Timer Array Modules (GPTA) with additional Local Timer Cell Array (LTCA2) providing a powerful set of digital signal filtering and timer functionality to realize autonomous and complex Input/Output management
  - Two Capture / Compare 6 modules
  - Two General Purpose 12 Timer Units (GPT120 and GPT121)
- 44 analog input lines for ADC
  - 4 independent kernels (ADC0, ADC1, and ADC2)
  - Analog supply voltage range from 3.3 V to 5 V (single supply)
- 4 different FADC input channels
  - channels with impedance control and overlaid with ADC1 inputs
  - Extreme fast conversion, 21 cycles of f_{FADC} clock
  - 10-bit A/D conversion (higher resolution can be achieved by averaging of consecutive conversions in digital data reduction filter)
- 8 digital input lines for SENT
  - communication according to the SENT specification J2716 FEB2008
- 221 digital general purpose I/O lines (GPIO)
- Digital I/O ports with 3.3 V capability
- On-chip debug support for OCDS Level 1 (CPU, PCP, DMA, On Chip Buses)
- Dedicated Emulation Device chip available (TC1793ED)
  - multi-core debugging, real time tracing, and calibration
  - four/five wire JTAG (IEEE 1149.1) or two wire DAP (Device Access Port) interface
- Power Management System
- Clock Generation Unit with PLL and PLL_ERAY
- Flexible CRC Engine (FCE)
  - IEEE 802.3 CRC32 ethernet polynomial: 0x82608EDB (CRC kernel 0)
  - CRC32C Castagnoli: 0xD419CC15 (CRC kernel 1)

The **SAK-TC1793N-512F270EF** has the following features:

- High-performance 32-bit super-scalar TriCore V1.6 CPU with 6-stage pipeline
  - Superior real-time performance
  - Strong bit handling
  - Fully integrated DSP capabilities
  - Multiply-accumulate unit able to sustain 2 MAC operations per cycle
  - Fully pipelined Floating point unit (FPU)
  - 270 MHz operation at full temperature range
- 32-bit Peripheral Control Processor with single cycle instruction (PCP2)
  - 16 Kbyte Parameter Memory (PRAM)
  - 32 Kbyte Code Memory (CMEM)
  - 200 MHz operation at full temperature range
- Multiple on-chip memories
  - 4 Mbyte Program Flash Memory (PFLASH) with ECC
  - 192 Kbyte Data Flash Memory (DFLASH) usable for EEPROM emulation
  - 2 x 8 Kbyte Key Flash

  - 128 Kbyte Data Scratch-Pad RAM (DSPR)
  - 16 Kbyte Instruction Cache (ICACHE)
  - 32 Kbyte Instruction Scratch-Pad RAM (PSPR)
  - 16 Kbyte Data Cache (DACHE)
  - 128 Kbyte Memory (SRAM)
  - 16 Kbyte BootROM (BROM)
- 16-Channel DMA Controller
- 8-Channel Safe DMA (SDMA) Controller
- Sophisticated interrupt system with 2×255 hardware priority arbitration levels serviced by CPU or PCP2
- High performing on-chip bus structure
  - 64-bit Cross Bar Interconnect between CPU, Flash and Data Memory
  - 32-bit System Peripheral Bus (SPB) for on-chip peripheral and functional units
  - One bus bridge (SFI Bridge)
- Versatile On-chip Peripheral Units
  - Two Asynchronous/Synchronous Serial Channels (ASC) with baud rate generator, parity, framing and overrun error detection
  - Four High-Speed Synchronous Serial Channels (SSC) with programmable data length and shift direction
  - Four SSC Guardian (SSCG) modules, one for each SSC
  - Two serial Micro Second Bus interfaces (MSC) for serial port expansion to external power devices
  - Two High-Speed Micro Link interfaces (MLI) for serial inter-processor communication
  - One External Bus Interface (EBU) supporting different memories: asynchronous memories e.g. SRAM, peripheral devices; synchronous devices e.g. burst NOR flash, PSRAM; and DDR NOR flash e.g. LPDDR-NVM (Jedec 42.2), ONFI 2.0 (limited frequency at 1.8 V I/O supply)
  - One MultiCAN Module with 4 CAN nodes and 128 free assignable message objects for high efficiency data handling via FIFO buffering and gateway data transfer (one CAN node supports TTCAN functionality)
  - Two General Purpose Timer Array Modules (GPTA) with additional Local Timer Cell Array (LTCA2) providing a powerful set of digital signal filtering and timer functionality to realize autonomous and complex Input/Output management
  - Two Capture / Compare 6 modules
  - Two General Purpose 12 Timer Units (GPT120 and GPT121)
- 44 analog input lines for ADC
  - 4 independent kernels (ADC0, ADC1, and ADC2)
  - Analog supply voltage range from 3.3 V to 5 V (single supply)
- 4 different FADC input channels
  - channels with impedance control and overlaid with ADC1 inputs
  - Extreme fast conversion, 21 cycles of f_{FADC} clock

  - 10-bit A/D conversion (higher resolution can be achieved by averaging of consecutive conversions in digital data reduction filter)
- 8 digital input lines for SENT
  - communication according to the SENT specification J2716 FEB2008
- 221 digital general purpose I/O lines (GPIO)
- Digital I/O ports with 3.3 V capability
- On-chip debug support for OCDS Level 1 (CPU, PCP, DMA, On Chip Buses)
- Dedicated Emulation Device chip available (TC1793ED)
  - multi-core debugging, real time tracing, and calibration
  - four/five wire JTAG (IEEE 1149.1) or two wire DAP (Device Access Port) interface
- Power Management System
- Clock Generation Unit with PLL and PLL_ERAY
- Flexible CRC Engine (FCE)
  - IEEE 802.3 CRC32 ethernet polynomial: 0x82608EDB (CRC kernel 0)
  - CRC32C Castagnoli: 0xD419CC15 (CRC kernel 1)

The **SAK-TC1793S-512F270EF** has the following features:

- High-performance 32-bit super-scalar TriCore V1.6 CPU with 6-stage pipeline
  - Superior real-time performance
  - Strong bit handling
  - Fully integrated DSP capabilities
  - Multiply-accumulate unit able to sustain 2 MAC operations per cycle
  - Fully pipelined Floating point unit (FPU)
  - 270 MHz operation at full temperature range
- 32-bit Peripheral Control Processor with single cycle instruction (PCP2)
  - 16 Kbyte Parameter Memory (PRAM)
  - 32 Kbyte Code Memory (CMEM)
  - 200 MHz operation at full temperature range
- Multiple on-chip memories
  - 4 Mbyte Program Flash Memory (PFLASH) with ECC
  - 192 Kbyte Data Flash Memory (DFLASH) usable for EEPROM emulation
  - 2 x 8 Kbyte Key Flash
  - 128 Kbyte Data Scratch-Pad RAM (DSPR)
  - 16 Kbyte Instruction Cache (ICACHE)
  - 32 Kbyte Instruction Scratch-Pad RAM (PSPR)
  - 16 Kbyte Data Cache (DACHE)
  - 128 Kbyte Memory (SRAM)
  - 16 Kbyte BootROM (BROM)
- 16-Channel DMA Controller
- 8-Channel Safe DMA (SDMA) Controller
- Sophisticated interrupt system with 2×255 hardware priority arbitration levels serviced by CPU or PCP2
- High performing on-chip bus structure

  - 64-bit Cross Bar Interconnect between CPU, Flash and Data Memory
  - 32-bit System Peripheral Bus (SPB) for on-chip peripheral and functional units
  - One bus bridge (SFI Bridge)
- Versatile On-chip Peripheral Units
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  - Four High-Speed Synchronous Serial Channels (SSC) with programmable data length and shift direction
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  - Two serial Micro Second Bus interfaces (MSC) for serial port expansion to external power devices
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  - One External Bus Interface (EBU) supporting different memories: asynchronous memories e.g. SRAM, peripheral devices; synchronous devices e.g. burst NOR flash, PSRAM; and DDR NOR flash e.g. LPDDR-NVM (Jedec 42.2), ONFI 2.0 (limited frequency at 1.8 V I/O supply)
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  - One FlexRay™ module with 2 channels (E-Ray).
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- 221 digital general purpose I/O lines (GPIO)
- Digital I/O ports with 3.3 V capability
- On-chip debug support for OCDS Level 1 (CPU, PCP, DMA, On Chip Buses)
- Dedicated Emulation Device chip available (TC1793ED)
  - multi-core debugging, real time tracing, and calibration
  - four/five wire JTAG (IEEE 1149.1) or two wire DAP (Device Access Port) interface
- Power Management System

- Clock Generation Unit with PLL and PLL_ERAY
- Flexible CRC Engine (FCE)
  - IEEE 802.3 CRC32 ethernet polynomial: 0x82608EDB (CRC kernel 0)
  - CRC32C Castagnoli: 0xD419CC15 (CRC kernel 1)
- Secure Hardware Extension (SHE)
  - For further information please contact your Infineon representative

Ordering Information

The ordering code for Infineon microcontrollers provides an exact reference to the required product. This ordering code identifies:

- The derivative itself, i.e. its function set, the temperature range, and the supply voltage
- The package and the type of delivery.

For the available ordering codes for the TC1793 please refer to the **"Product Catalog Microcontrollers"**, which summarizes all available microcontroller variants.

This document describes the derivatives of the device.The **Table 1** enumerates these derivatives and summarizes the differences.

Table 1 TC1793 Derivative Synopsis

Derivative	Ambient Temperature Range
SAK-TC1793F-512F270EF	T_A = -40°C to +125°C
SAK-TC1793F-512F200EF	T_A = -40°C to +125°C
SAK-TC1793F-512F200EB	T_A = -40°C to +125°C
SAK-TC1793N-512F270EF	T_A = -40°C to +125°C
SAK-TC1793S-512F270EF	T_A = -40°C to +125°C

2 System Overview of the TC1793

The TC1793 combines three powerful technologies within one silicon die, achieving new levels of power, speed, and economy for embedded applications:

- Reduced Instruction Set Computing (RISC) processor architecture
- Digital Signal Processing (DSP) operations and addressing modes
- On-chip memories and peripherals

DSP operations and addressing modes provide the computational power necessary to efficiently analyze complex real-world signals. The RISC load/store architecture provides high computational bandwidth with low system cost. On-chip memory and peripherals are designed to support even the most demanding high-bandwidth real-time embedded control-systems tasks.

Additional high-level features of the TC1793 include:

- Efficient memory organization: instruction and data scratch memories, caches
- Serial communication interfaces – flexible synchronous and asynchronous modes
- Peripheral Control Processor – standalone data operations and interrupt servicing
- DMA Controller – DMA operations and interrupt servicing
- General-purpose timers
- High-performance on-chip buses
- On-chip debugging and emulation facilities
- Flexible interconnections to external components
- Flexible power-management

The TC1793 is a high-performance microcontroller with TriCore CPU, program and data memories, buses, bus arbitration, an interrupt controller, a peripheral control processor and a DMA controller and several on-chip peripherals. The TC1793 is designed to meet the needs of the most demanding embedded control systems applications where the competing issues of price/performance, real-time responsiveness, computational power, data bandwidth, and power consumption are key design elements.

The TC1793 offers several versatile on-chip peripheral units such as serial controllers, timer units, and Analog-to-Digital converters. Within the TC1793, all these peripheral units are connected to the TriCore CPU/system via the Flexible Peripheral Interconnect (FPI) Bus and the Cross Bar Interconnect (SRI). Several I/O lines on the TC1793 ports are reserved for these peripheral units to communicate with the external world.

2.1 Block Diagram

Figure 1 shows the block diagram of the **SAK-TC1793F-512F270EF** / **SAK-TC1793F-512F200EF** / **SAK-TC1793F-512F200EB**.

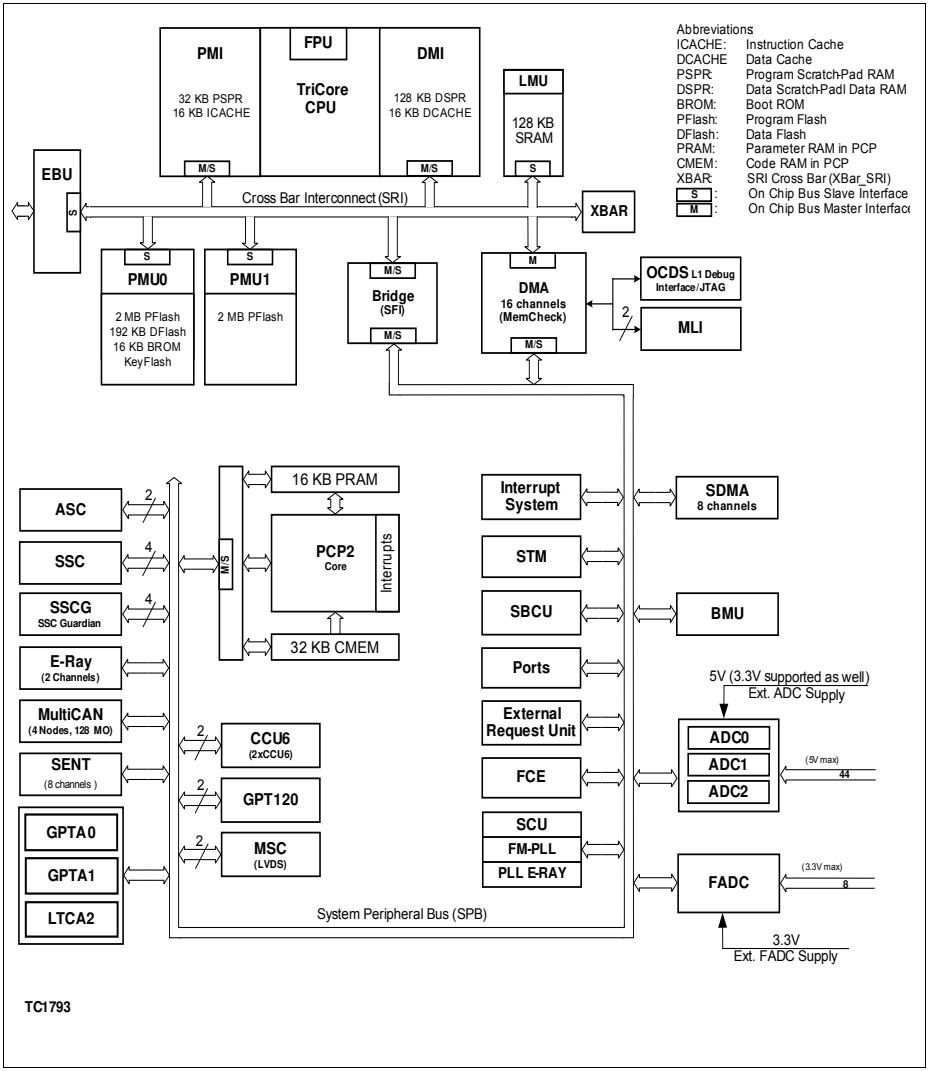

Figure 1 Block Diagram

Figure 2 shows the block diagram of the **SAK-TC1793N-512F270EF**.

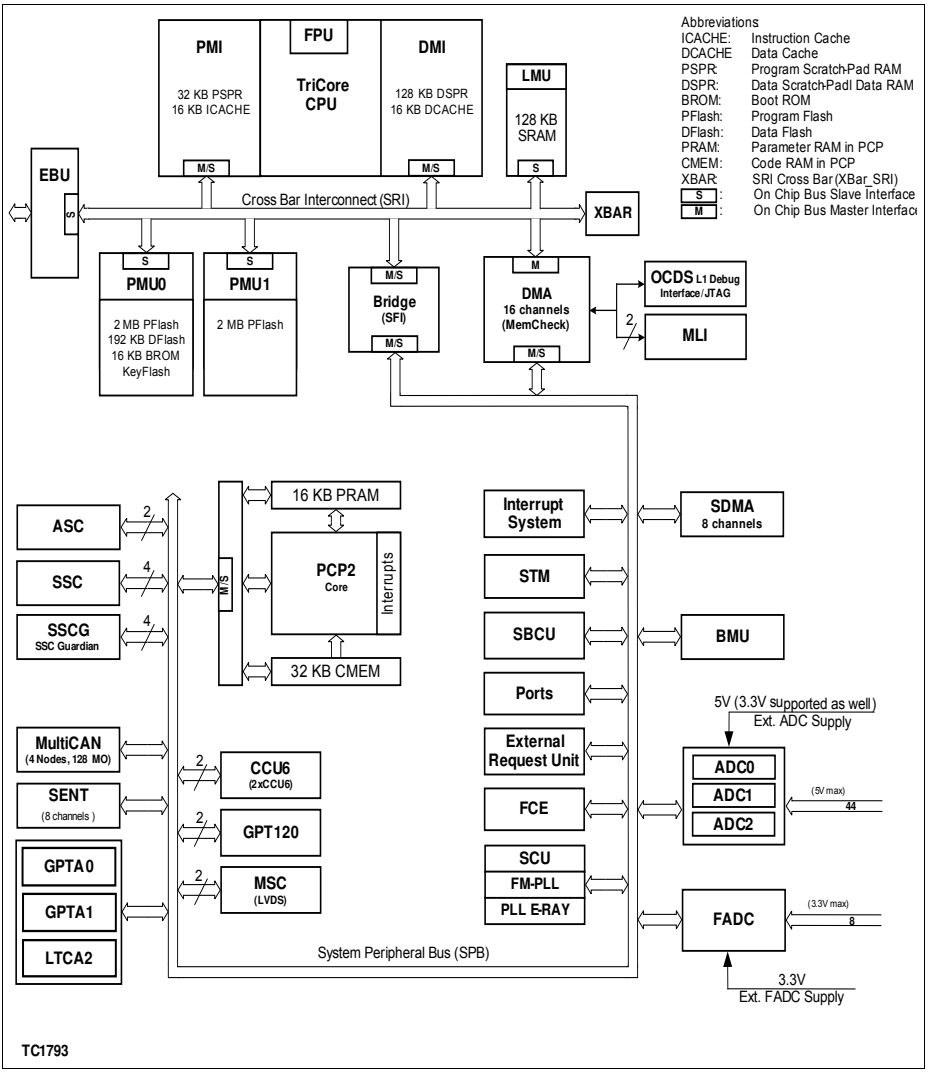

Figure 2 Block Diagram

Figure 3 shows the block diagram of the **SAK-TC1793S-512F270EF**.

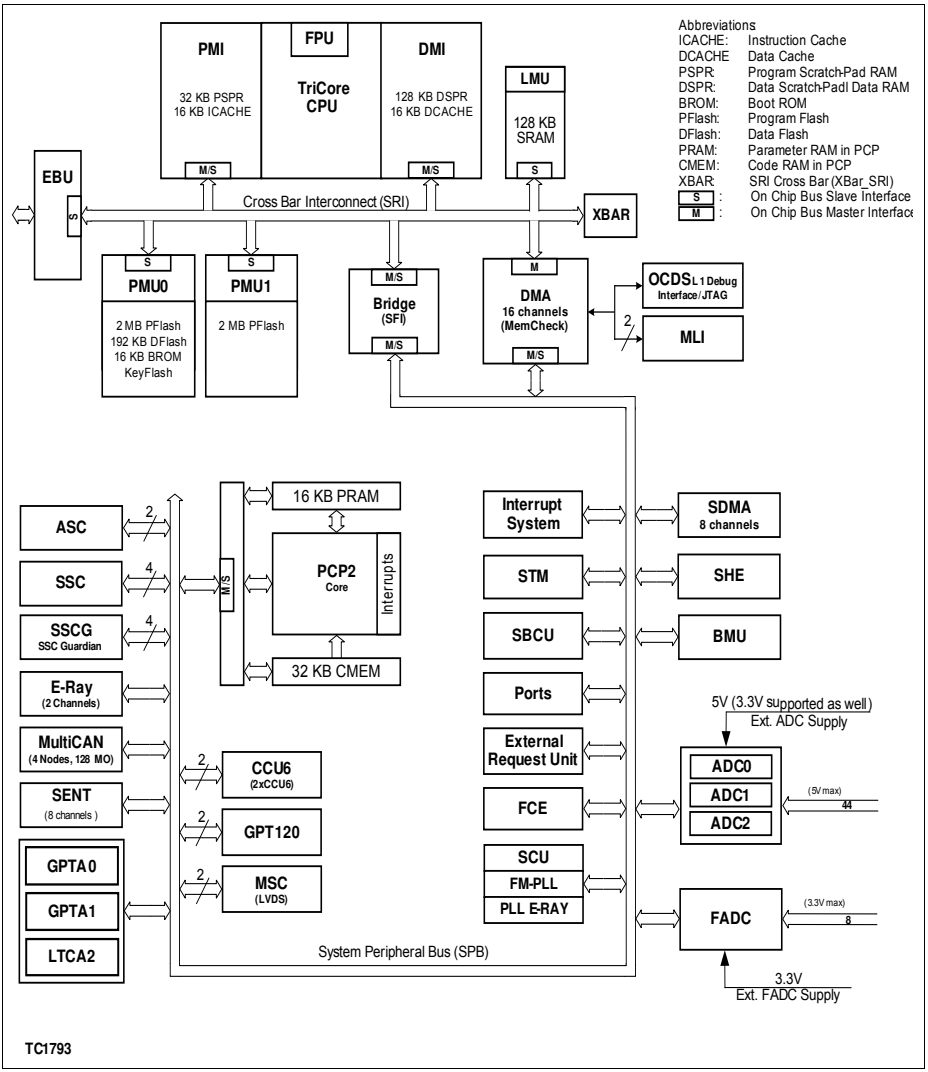

Figure 3 Block Diagram

3 Pinning

Figure 4 is showing the TC1793 Logic Symbol.

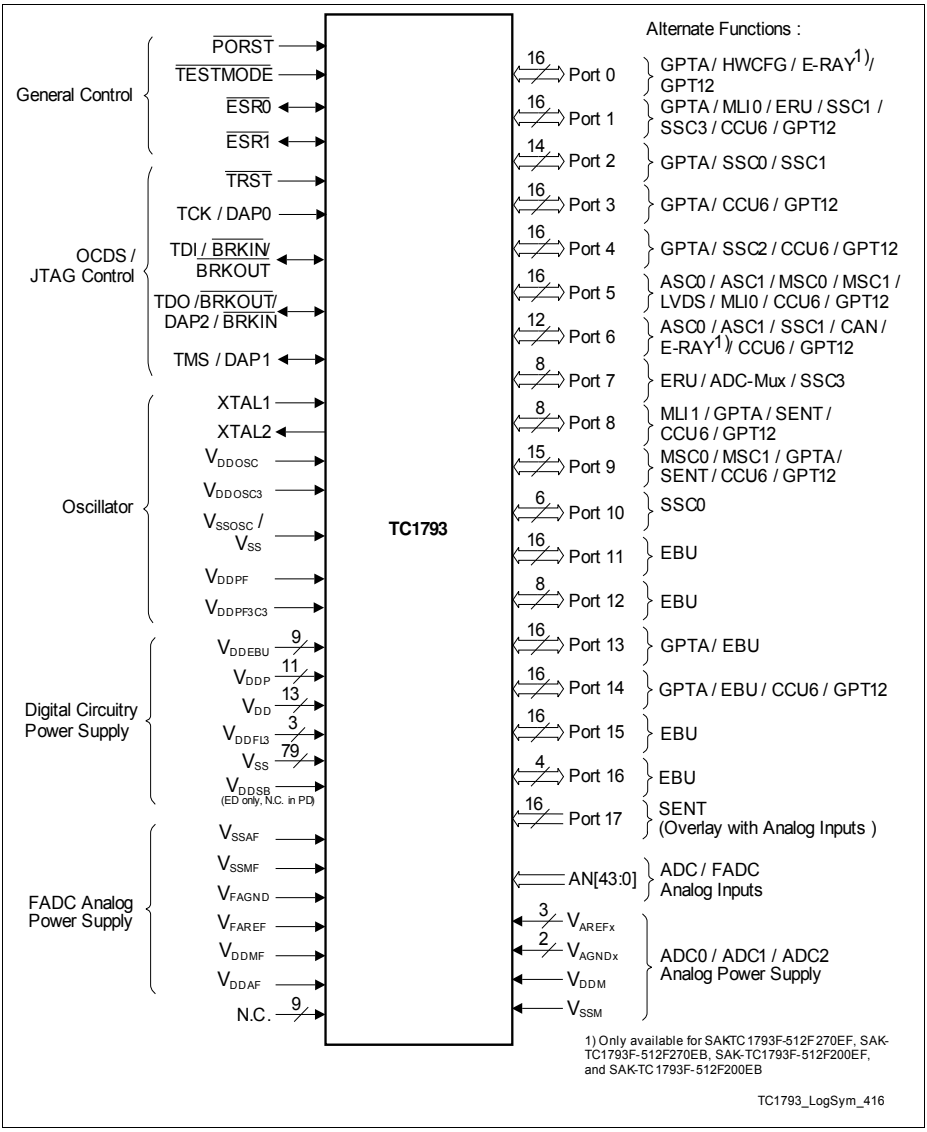

Figure 4 TC1793 Logic Symbol

3.1 TC1793 Pin Configuration

This chapter shows the pin configuration of the TC1793 package PG-BGA- 416.

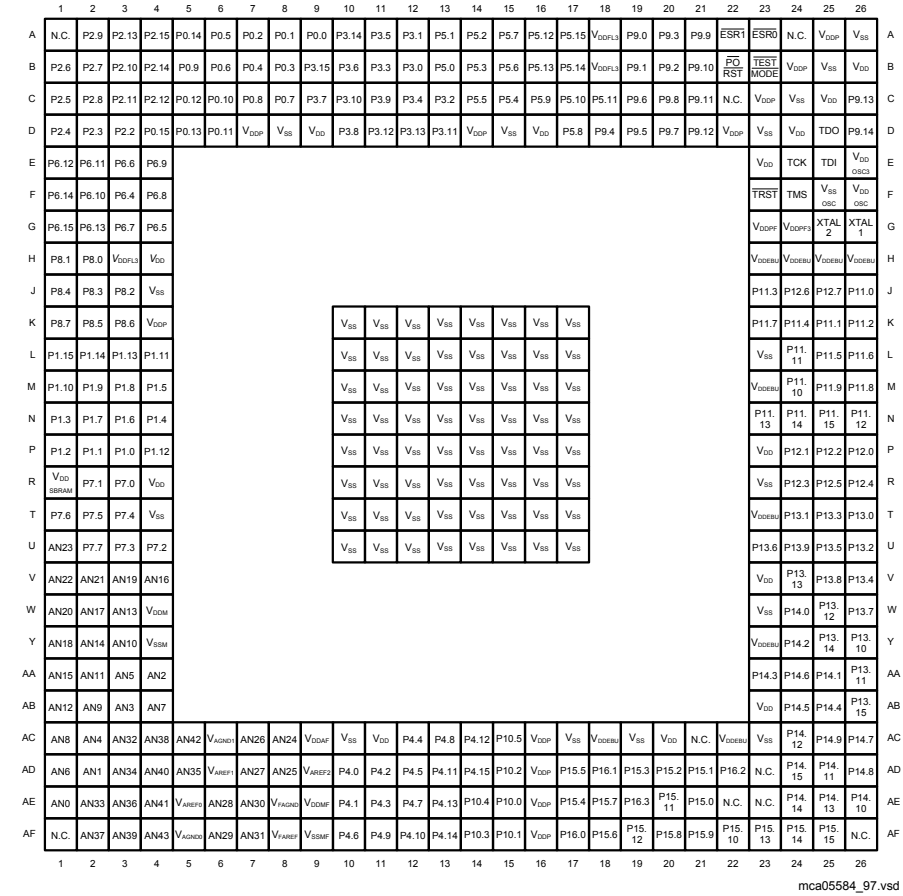

Figure 5 TC1793 Pinning for PG-BGA- 416 Package

Table 2 Pin Definitions and Functions

Pin	Symbol	Ctrl.	Type	Function
Port 0				
A9	P0.0	I/O	A1+/ PU	**Port 0 General Purpose I/O Line 0**
	HWCFG0	I		**Hardware Configuration Input 0**
	OUT56	O1		**OUT56 Line of GPTA0**
	OUT56	O2		**OUT56 Line of GPTA1**
	OUT80	O3		**OUT80 Line of LTCA2**
A8	P0.1	I/O	A1/ PU	**Port 0 General Purpose I/O Line 1**
	HWCFG1	I		**Hardware Configuration Input 1**
	OUT57	O1		**OUT57 Line of GPTA0**
	OUT57	O2		**OUT57 Line of GPTA1**
	OUT81	O3		**OUT81 Line of LTCA2**
A7	P0.2	I/O	A2/ PU	**Port 0 General Purpose I/O Line 2**
	HWCFG2	I		**Hardware Configuration Input 2**
	OUT58	O1		**OUT58 Line of GPTA0**
	OUT58	O2		**OUT58 Line of GPTA1**
	OUT82	O3		**OUT82 Line of LTCA2**
B8	P0.3	I/O	A1/ PU	**Port 0 General Purpose I/O Line 3**
	HWCFG3	I		**Hardware Configuration Input 3**
	OUT59	O1		**OUT59 Line of GPTA0**
	OUT59	O2		**OUT59 Line of GPTA1**
	OUT83	O3		**OUT83 Line of LTCA2**

Table 2 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
B7	P0.4	I/O	A1/ PU	**Port 0 General Purpose I/O Line 4**
	HWCFG4	I		**Hardware Configuration Input 4**
	OUT60	O1		**OUT60 Line of GPTA0**
	OUT60	O2		**OUT60 Line of GPTA1**
	EVTO0	O3		**MCDS Output Event 0**[1)]
A6	P0.5	I/O	A1/ PU	**Port 0 General Purpose I/O Line 5**
	HWCFG5	I		**Hardware Configuration Input 5**
	OUT61	O1		**OUT61 Line of GPTA0**
	OUT61	O2		**OUT61 Line of GPTA1**
	EVTO1	O3		**MCDS Output Event 1**[1)]
B6	P0.6	I/O	A2/ PU	**Port 0 General Purpose I/O Line 6**
	HWCFG6	I		**Hardware Configuration Input 6**
	OUT62	O1		**OUT62 Line of GPTA0**
	OUT62	O2		**OUT62 Line of GPTA1**
	EVTO2	O3		**MCDS Output Event 2**[1)]
C8	P0.7	I/O	A1/ PU	**Port 0 General Purpose I/O Line 7**
	HWCFG7	I		**Hardware Configuration Input 7**
	OUT63	O1		**OUT63 Line of GPTA0**
	OUT63	O2		**OUT63 Line of GPTA1**
	EVTO3	O3		**MCDS Output Event 3**[1)]
C7	P0.8	I/O	A1/ PU	**Port 0 General Purpose I/O Line 8**
	Reserved	O1		**-**
	Reserved	O2		**-**
	Reserved	O3		**-**

Table 2 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
B5	P0.9	I/O	A1/ PU	**Port 0 General Purpose I/O Line 9**
	RXDA0	I		**E-Ray Channel A Receive Data Input 0** [2]
	Reserved	O1		-
	Reserved	O2		-
	Reserved	O3		-
C6	P0.10	I/O	A2/ PU	**Port 0 General Purpose I/O Line 10**
	TXENA	O1		**E-Ray Channel A transmit Data Output enable** [2]
	Reserved	O2		-
	Reserved	O3		-
D6	P0.11	I/O	A2/ PU	**Port 0 General Purpose I/O Line 11**
	T5INB	I		**GPT120**
	T5INA	I		**GPT121**
	TXENB	O1		**E-Ray Channel B transmit Data Output enable** [2]
	Reserved	O2		-
	Reserved	O3		-
C5	P0.12	I/O	A2/ PU	**Port 0 General Purpose I/O Line 12**
	T5EUDA	I		**GPT120**
	T5EUDB	I		**GPT121**
	TXDB	O1		**E-Ray Channel B transmit Data Output** [2]
	Reserved	O2		-
	Reserved	O3		-