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Tel: +86-755-8981 8866 Fax: +86-755-8427 6832

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Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China



# 32-Bit

Microcontroller

# TC1793

32-Bit Single-Chip Microcontroller

Data Sheet

V 1.2 2014-05

Microcontrollers

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# 32-Bit

Microcontroller

# TC1793

32-Bit Single-Chip Microcontroller

Data Sheet

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# 1 Summary of Features

The **SAK-TC1793F-512F270EF** has the following features:

- High-performance 32-bit super-scalar TriCore V1.6 CPU with 6-stage pipeline
  - Superior real-time performance
  - Strong bit handling
  - Fully integrated DSP capabilities
  - Multiply-accumulate unit able to sustain 2 MAC operations per cycle
  - Fully pipelined Floating point unit (FPU)
  - 270 MHz operation at full temperature range
- 32-bit Peripheral Control Processor with single cycle instruction (PCP2)
  - 16 Kbyte Parameter Memory (PRAM)
  - 32 Kbyte Code Memory (CMEM)
  - 200 MHz operation at full temperature range
- Multiple on-chip memories
  - 4 Mbyte Program Flash Memory (PFLASH) with ECC
  - 192 Kbyte Data Flash Memory (DFLASH) usable for EEPROM emulation
  - 2 x 8 Kbyte Key Flash
  - 128 Kbyte Data Scratch-Pad RAM (DSPR)
  - 16 Kbyte Instruction Cache (ICACHE)
  - 32 Kbyte Instruction Scratch-Pad RAM (PSPR)
  - 16 Kbyte Data Cache (DACHE)
  - 128 Kbyte Memory (SRAM)
  - 16 Kbyte BootROM (BROM)
- 16-Channel DMA Controller
- 8-Channel Safe DMA (SDMA) Controller
- Sophisticated interrupt system with  $2 \times 255$  hardware priority arbitration levels serviced by CPU or PCP2
- High performing on-chip bus structure
  - 64-bit Cross Bar Interconnect between CPU, Flash and Data Memory
  - 32-bit System Peripheral Bus (SPB) for on-chip peripheral and functional units
  - One bus bridge (SFI Bridge)
- Versatile On-chip Peripheral Units
  - Two Asynchronous/Synchronous Serial Channels (ASC) with baud rate generator, parity, framing and overrun error detection
  - Four High-Speed Synchronous Serial Channels (SSC) with programmable data length and shift direction
  - Four SSC Guardian (SSCG) modules, one for each SSC
  - Two serial Micro Second Bus interfaces (MSC) for serial port expansion to external power devices
  - Two High-Speed Micro Link interfaces (MLI) for serial inter-processor communication

---

**Summary of Features**

- One External Bus Interface (EBU) supporting different memories: asynchronous memories e.g. SRAM, peripheral devices; synchronous devices e.g. burst NOR flash, PSRAM; and DDR NOR flash e.g. LPDDR-NVM (Jedec 42.2), ONFI 2.0 (limited frequency at 1.8 V I/O supply)
- One MultiCAN Module with 4 CAN nodes and 128 free assignable message objects for high efficiency data handling via FIFO buffering and gateway data transfer (one CAN node supports TTCAN functionality)
- One FlexRay™ module with 2 channels (E-Ray).
- Two General Purpose Timer Array Modules (GPTA) with additional Local Timer Cell Array (LTCA2) providing a powerful set of digital signal filtering and timer functionality to realize autonomous and complex Input/Output management
- Two Capture / Compare 6 modules
- Two General Purpose 12 Timer Units (GPT120 and GPT121)
- 44 analog input lines for ADC
  - 4 independent kernels (ADC0, ADC1, and ADC2)
  - Analog supply voltage range from 3.3 V to 5 V (single supply)
- 4 different FADC input channels
  - channels with impedance control and overlaid with ADC1 inputs
  - Extreme fast conversion, 21 cycles of  $f_{FADC}$  clock
  - 10-bit A/D conversion (higher resolution can be achieved by averaging of consecutive conversions in digital data reduction filter)
- 8 digital input lines for SENT
  - communication according to the SENT specification J2716 FEB2008
- 221 digital general purpose I/O lines (GPIO)
- Digital I/O ports with 3.3 V capability
- On-chip debug support for OCDS Level 1 (CPU, PCP, DMA, On Chip Buses)
- Dedicated Emulation Device chip available (TC1793ED)
  - multi-core debugging, real time tracing, and calibration
  - four/five wire JTAG (IEEE 1149.1) or two wire DAP (Device Access Port) interface
- Power Management System
- Clock Generation Unit with PLL and PLL\_ERAY
- Flexible CRC Engine (FCE)
  - IEEE 802.3 CRC32 ethernet polynomial: 0x82608EDB (CRC kernel 0)
  - CRC32C Castagnoli: 0xD419CC15 (CRC kernel 1)

The **SAK-TC1793F-512F200EB / SAK-TC1793F-512F200EF** has the following features:

- High-performance 32-bit super-scalar TriCore V1.6 CPU with 6-stage pipeline
  - Superior real-time performance
  - Strong bit handling
  - Fully integrated DSP capabilities
  - Multiply-accumulate unit able to sustain 2 MAC operations per cycle
  - Fully pipelined Floating point unit (FPU)

---

**Summary of Features**

- 200 MHz operation at full temperature range
- 32-bit Peripheral Control Processor with single cycle instruction (PCP2)
  - 16 Kbyte Parameter Memory (PRAM)
  - 32 Kbyte Code Memory (CMEM)
  - 200 MHz operation at full temperature range
- Multiple on-chip memories
  - 4 Mbyte Program Flash Memory (PFLASH) with ECC
  - 192 Kbyte Data Flash Memory (DFLASH) usable for EEPROM emulation
  - 2 x 8 Kbyte Key Flash
  - 128 Kbyte Data Scratch-Pad RAM (DSPR)
  - 16 Kbyte Instruction Cache (ICACHE)
  - 32 Kbyte Instruction Scratch-Pad RAM (PSPR)
  - 16 Kbyte Data Cache (DACHE)
  - 128 Kbyte Memory (SRAM)
  - 16 Kbyte BootROM (BROM)
- 16-Channel DMA Controller
- 8-Channel Safe DMA (SDMA) Controller
- Sophisticated interrupt system with 2 × 255 hardware priority arbitration levels serviced by CPU or PCP2
- High performing on-chip bus structure
  - 64-bit Cross Bar Interconnect between CPU, Flash and Data Memory
  - 32-bit System Peripheral Bus (SPB) for on-chip peripheral and functional units
  - One bus bridge (SFI Bridge)
- Versatile On-chip Peripheral Units
  - Two Asynchronous/Synchronous Serial Channels (ASC) with baud rate generator, parity, framing and overrun error detection
  - Two High-Speed Synchronous Serial Channels (SSC) with programmable data length and shift direction
  - Four SSC Guardian (SSCG) modules, one for each SSC
  - Two serial Micro Second Bus interfaces (MSC) for serial port expansion to external power devices
  - Two High-Speed Micro Link interfaces (MLI) for serial inter-processor communication
  - One External Bus Interface (EBU) supporting different memories: asynchronous memories e.g. SRAM, peripheral devices; synchronous devices e.g. burst NOR flash, PSRAM; and DDR NOR flash e.g. LPDDR-NVM (Jedec 42.2), ONFI 2.0 (limited frequency at 1.8 V I/O supply)
  - One MultiCAN Module with 4 CAN nodes and 128 free assignable message objects for high efficiency data handling via FIFO buffering and gateway data transfer (one CAN node supports TTCAN functionality)
  - One FlexRay™ module with 2 channels (E-Ray).

---

## Summary of Features

- Two General Purpose Timer Array Modules (GPTA) with additional Local Timer Cell Array (LTCA2) providing a powerful set of digital signal filtering and timer functionality to realize autonomous and complex Input/Output management
- Two Capture / Compare 6 modules
- Two General Purpose 12 Timer Units (GPT120 and GPT121)
- 44 analog input lines for ADC
  - 4 independent kernels (ADC0, ADC1, and ADC2)
  - Analog supply voltage range from 3.3 V to 5 V (single supply)
- 4 different FADC input channels
  - channels with impedance control and overlaid with ADC1 inputs
  - Extreme fast conversion, 21 cycles of  $f_{\text{FADC}}$  clock
  - 10-bit A/D conversion (higher resolution can be achieved by averaging of consecutive conversions in digital data reduction filter)
- 8 digital input lines for SENT
  - communication according to the SENT specification J2716 FEB2008
- 221 digital general purpose I/O lines (GPIO)
- Digital I/O ports with 3.3 V capability
- On-chip debug support for OCDS Level 1 (CPU, PCP, DMA, On Chip Buses)
- Dedicated Emulation Device chip available (TC1793ED)
  - multi-core debugging, real time tracing, and calibration
  - four/five wire JTAG (IEEE 1149.1) or two wire DAP (Device Access Port) interface
- Power Management System
- Clock Generation Unit with PLL and PLL\_ERAY
- Flexible CRC Engine (FCE)
  - IEEE 802.3 CRC32 ethernet polynomial: 0x82608EDB (CRC kernel 0)
  - CRC32C Castagnoli: 0xD419CC15 (CRC kernel 1)

The **SAK-TC1793N-512F270EF** has the following features:

- High-performance 32-bit super-scalar TriCore V1.6 CPU with 6-stage pipeline
  - Superior real-time performance
  - Strong bit handling
  - Fully integrated DSP capabilities
  - Multiply-accumulate unit able to sustain 2 MAC operations per cycle
  - Fully pipelined Floating point unit (FPU)
  - 270 MHz operation at full temperature range
- 32-bit Peripheral Control Processor with single cycle instruction (PCP2)
  - 16 Kbyte Parameter Memory (PRAM)
  - 32 Kbyte Code Memory (CMEM)
  - 200 MHz operation at full temperature range
- Multiple on-chip memories
  - 4 Mbyte Program Flash Memory (PFLASH) with ECC
  - 192 Kbyte Data Flash Memory (DFLASH) usable for EEPROM emulation
  - 2 x 8 Kbyte Key Flash

---

**Summary of Features**

- 128 Kbyte Data Scratch-Pad RAM (DSPR)
- 16 Kbyte Instruction Cache (ICACHE)
- 32 Kbyte Instruction Scratch-Pad RAM (PSPR)
- 16 Kbyte Data Cache (DACHE)
- 128 Kbyte Memory (SRAM)
- 16 Kbyte BootROM (BROM)
- 16-Channel DMA Controller
- 8-Channel Safe DMA (SDMA) Controller
- Sophisticated interrupt system with  $2 \times 255$  hardware priority arbitration levels serviced by CPU or PCP2
- High performing on-chip bus structure
  - 64-bit Cross Bar Interconnect between CPU, Flash and Data Memory
  - 32-bit System Peripheral Bus (SPB) for on-chip peripheral and functional units
  - One bus bridge (SFI Bridge)
- Versatile On-chip Peripheral Units
  - Two Asynchronous/Synchronous Serial Channels (ASC) with baud rate generator, parity, framing and overrun error detection
  - Four High-Speed Synchronous Serial Channels (SSC) with programmable data length and shift direction
  - Four SSC Guardian (SSCG) modules, one for each SSC
  - Two serial Micro Second Bus interfaces (MSC) for serial port expansion to external power devices
  - Two High-Speed Micro Link interfaces (MLI) for serial inter-processor communication
  - One External Bus Interface (EBU) supporting different memories: asynchronous memories e.g. SRAM, peripheral devices; synchronous devices e.g. burst NOR flash, PSRAM; and DDR NOR flash e.g. LPDDR-NVM (Jedec 42.2), ONFI 2.0 (limited frequency at 1.8 V I/O supply)
  - One MultiCAN Module with 4 CAN nodes and 128 free assignable message objects for high efficiency data handling via FIFO buffering and gateway data transfer (one CAN node supports TTCAN functionality)
  - Two General Purpose Timer Array Modules (GPTA) with additional Local Timer Cell Array (LTCA2) providing a powerful set of digital signal filtering and timer functionality to realize autonomous and complex Input/Output management
  - Two Capture / Compare 6 modules
  - Two General Purpose 12 Timer Units (GPT120 and GPT121)
- 44 analog input lines for ADC
  - 4 independent kernels (ADC0, ADC1, and ADC2)
  - Analog supply voltage range from 3.3 V to 5 V (single supply)
- 4 different FADC input channels
  - channels with impedance control and overlaid with ADC1 inputs
  - Extreme fast conversion, 21 cycles of  $f_{FADC}$  clock

---

**Summary of Features**

- 10-bit A/D conversion (higher resolution can be achieved by averaging of consecutive conversions in digital data reduction filter)
- 8 digital input lines for SENT
  - communication according to the SENT specification J2716 FEB2008
- 221 digital general purpose I/O lines (GPIO)
- Digital I/O ports with 3.3 V capability
- On-chip debug support for OCDS Level 1 (CPU, PCP, DMA, On Chip Buses)
- Dedicated Emulation Device chip available (TC1793ED)
  - multi-core debugging, real time tracing, and calibration
  - four/five wire JTAG (IEEE 1149.1) or two wire DAP (Device Access Port) interface
- Power Management System
- Clock Generation Unit with PLL and PLL\_ERAY
- Flexible CRC Engine (FCE)
  - IEEE 802.3 CRC32 ethernet polynomial: 0x82608EDB (CRC kernel 0)
  - CRC32C Castagnoli: 0xD419CC15 (CRC kernel 1)

The **SAK-TC1793S-512F270EF** has the following features:

- High-performance 32-bit super-scalar TriCore V1.6 CPU with 6-stage pipeline
  - Superior real-time performance
  - Strong bit handling
  - Fully integrated DSP capabilities
  - Multiply-accumulate unit able to sustain 2 MAC operations per cycle
  - Fully pipelined Floating point unit (FPU)
  - 270 MHz operation at full temperature range
- 32-bit Peripheral Control Processor with single cycle instruction (PCP2)
  - 16 Kbyte Parameter Memory (PRAM)
  - 32 Kbyte Code Memory (CMEM)
  - 200 MHz operation at full temperature range
- Multiple on-chip memories
  - 4 Mbyte Program Flash Memory (PFLASH) with ECC
  - 192 Kbyte Data Flash Memory (DFLASH) usable for EEPROM emulation
  - 2 x 8 Kbyte Key Flash
  - 128 Kbyte Data Scratch-Pad RAM (DSPR)
  - 16 Kbyte Instruction Cache (ICACHE)
  - 32 Kbyte Instruction Scratch-Pad RAM (PSPR)
  - 16 Kbyte Data Cache (DACHE)
  - 128 Kbyte Memory (SRAM)
  - 16 Kbyte BootROM (BROM)
- 16-Channel DMA Controller
- 8-Channel Safe DMA (SDMA) Controller
- Sophisticated interrupt system with 2 × 255 hardware priority arbitration levels serviced by CPU or PCP2
- High performing on-chip bus structure

---

**Summary of Features**

- 64-bit Cross Bar Interconnect between CPU, Flash and Data Memory
- 32-bit System Peripheral Bus (SPB) for on-chip peripheral and functional units
- One bus bridge (SFI Bridge)
- Versatile On-chip Peripheral Units
  - Two Asynchronous/Synchronous Serial Channels (ASC) with baud rate generator, parity, framing and overrun error detection
  - Four High-Speed Synchronous Serial Channels (SSC) with programmable data length and shift direction
  - Four SSC Guardian (SSCG) modules, one for each SSC
  - Two serial Micro Second Bus interfaces (MSC) for serial port expansion to external power devices
  - Two High-Speed Micro Link interfaces (MLI) for serial inter-processor communication
  - One External Bus Interface (EBU) supporting different memories: asynchronous memories e.g. SRAM, peripheral devices; synchronous devices e.g. burst NOR flash, PSRAM; and DDR NOR flash e.g. LPDDR-NVM (Jedec 42.2), ONFI 2.0 (limited frequency at 1.8 V I/O supply)
  - One MultiCAN Module with 4 CAN nodes and 128 free assignable message objects for high efficiency data handling via FIFO buffering and gateway data transfer (one CAN node supports TTCAN functionality)
  - One FlexRay™ module with 2 channels (E-Ray).
  - Two General Purpose Timer Array Modules (GPTA) with additional Local Timer Cell Array (LTCA2) providing a powerful set of digital signal filtering and timer functionality to realize autonomous and complex Input/Output management
  - Two Capture / Compare 6 modules
  - Two General Purpose 12 Timer Units (GPT120 and GPT121)
- 44 analog input lines for ADC
  - 4 independent kernels (ADC0, ADC1, and ADC2)
  - Analog supply voltage range from 3.3 V to 5 V (single supply)
- 4 different FADC input channels
  - channels with impedance control and overlaid with ADC1 inputs
  - Extreme fast conversion, 21 cycles of  $f_{FADC}$  clock
  - 10-bit A/D conversion (higher resolution can be achieved by averaging of consecutive conversions in digital data reduction filter)
- 8 digital input lines for SENT
  - communication according to the SENT specification J2716 FEB2008
- 221 digital general purpose I/O lines (GPIO)
- Digital I/O ports with 3.3 V capability
- On-chip debug support for OCDS Level 1 (CPU, PCP, DMA, On Chip Buses)
- Dedicated Emulation Device chip available (TC1793ED)
  - multi-core debugging, real time tracing, and calibration
  - four/five wire JTAG (IEEE 1149.1) or two wire DAP (Device Access Port) interface
- Power Management System

---

**Summary of Features**

- Clock Generation Unit with PLL and PLL\_ERAY
- Flexible CRC Engine (FCE)
  - IEEE 802.3 CRC32 ethernet polynomial: 0x82608EDB (CRC kernel 0)
  - CRC32C Castagnoli: 0xD419CC15 (CRC kernel 1)
- Secure Hardware Extension (SHE)
  - For further information please contact your Infineon representative



Summary of Features

**Ordering Information**

The ordering code for Infineon microcontrollers provides an exact reference to the required product. This ordering code identifies:

- The derivative itself, i.e. its function set, the temperature range, and the supply voltage
- The package and the type of delivery.

For the available ordering codes for the TC1793 please refer to the “**Product Catalog Microcontrollers**”, which summarizes all available microcontroller variants.

This document describes the derivatives of the device. The **Table 1** enumerates these derivatives and summarizes the differences.

**Table 1 TC1793 Derivative Synopsis**

Derivative	Ambient Temperature Range
SAK-TC1793F-512F270EF	$T_A = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$
SAK-TC1793F-512F200EF	$T_A = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$
SAK-TC1793F-512F200EB	$T_A = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$
SAK-TC1793N-512F270EF	$T_A = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$
SAK-TC1793S-512F270EF	$T_A = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$

## **2 System Overview of the TC1793**

The TC1793 combines three powerful technologies within one silicon die, achieving new levels of power, speed, and economy for embedded applications:

- Reduced Instruction Set Computing (RISC) processor architecture
- Digital Signal Processing (DSP) operations and addressing modes
- On-chip memories and peripherals

DSP operations and addressing modes provide the computational power necessary to efficiently analyze complex real-world signals. The RISC load/store architecture provides high computational bandwidth with low system cost. On-chip memory and peripherals are designed to support even the most demanding high-bandwidth real-time embedded control-systems tasks.

Additional high-level features of the TC1793 include:

- Efficient memory organization: instruction and data scratch memories, caches
- Serial communication interfaces – flexible synchronous and asynchronous modes
- Peripheral Control Processor – standalone data operations and interrupt servicing
- DMA Controller – DMA operations and interrupt servicing
- General-purpose timers
- High-performance on-chip buses
- On-chip debugging and emulation facilities
- Flexible interconnections to external components
- Flexible power-management

The TC1793 is a high-performance microcontroller with TriCore CPU, program and data memories, buses, bus arbitration, an interrupt controller, a peripheral control processor and a DMA controller and several on-chip peripherals. The TC1793 is designed to meet the needs of the most demanding embedded control systems applications where the competing issues of price/performance, real-time responsiveness, computational power, data bandwidth, and power consumption are key design elements.

The TC1793 offers several versatile on-chip peripheral units such as serial controllers, timer units, and Analog-to-Digital converters. Within the TC1793, all these peripheral units are connected to the TriCore CPU/system via the Flexible Peripheral Interconnect (FPI) Bus and the Cross Bar Interconnect (SRI). Several I/O lines on the TC1793 ports are reserved for these peripheral units to communicate with the external world.

System Overview of the TC1793Block Diagram

2.1 Block Diagram

Figure 1 shows the block diagram of the SAK-TC1793F-512F270EF / SAK-TC1793F-512F200EF / SAK-TC1793F-512F200EB.

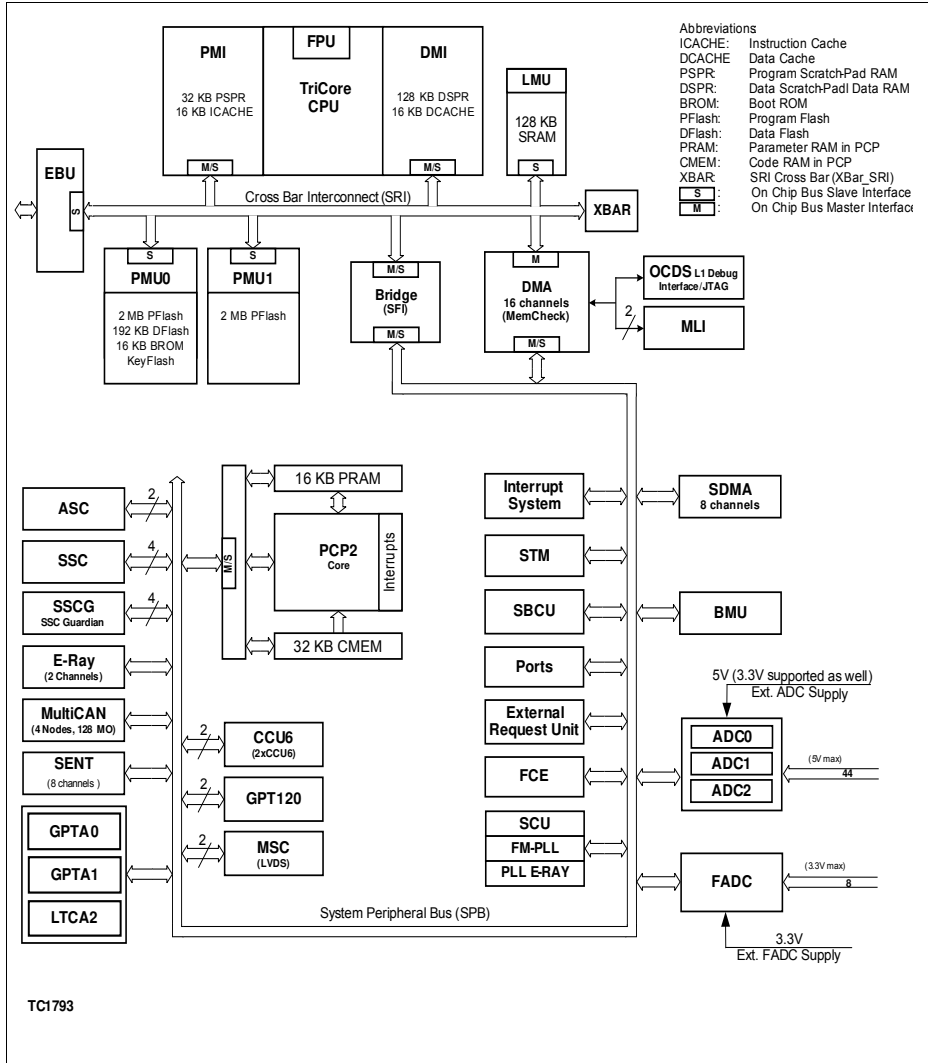


Figure 1 Block Diagram

System Overview of the TC1793Block Diagram

Figure 2 shows the block diagram of the SAK-TC1793N-512F270EF.

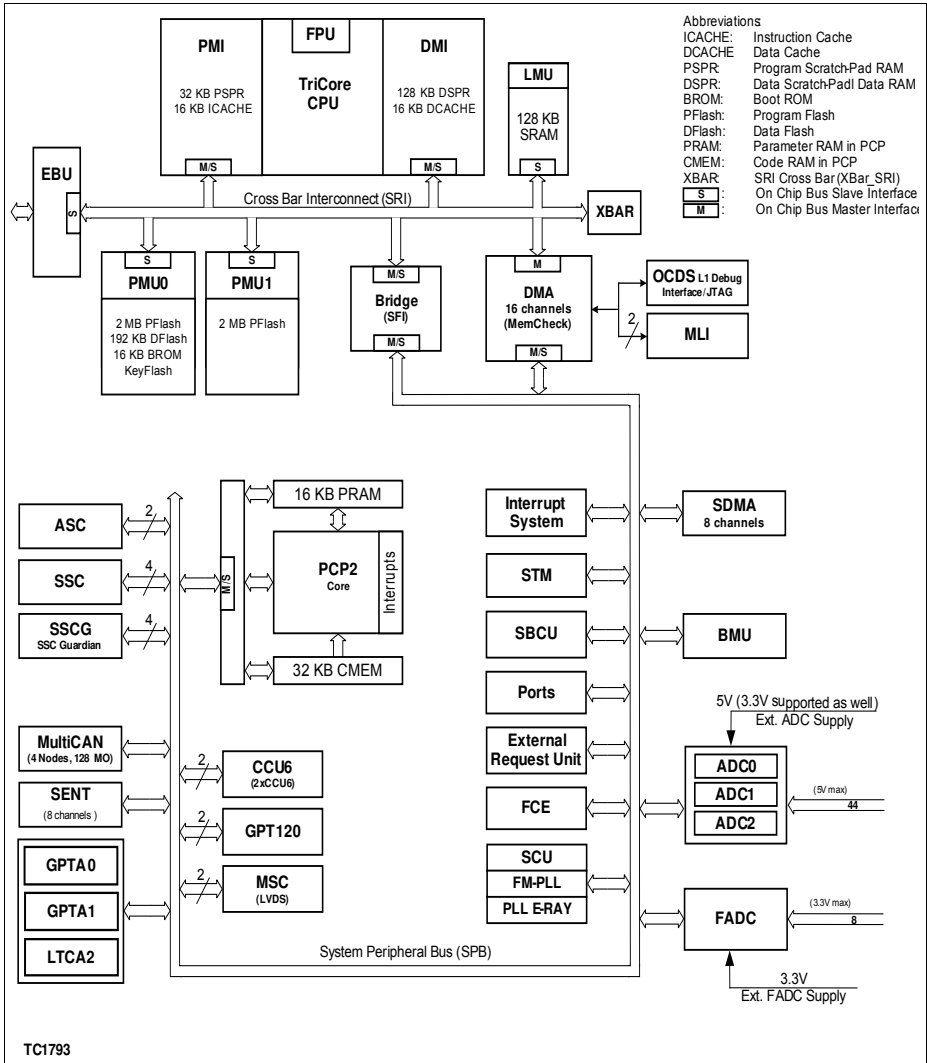


Figure 2 Block Diagram

System Overview of the TC1793Block Diagram

Figure 3 shows the block diagram of the SAK-TC1793S-512F270EF.

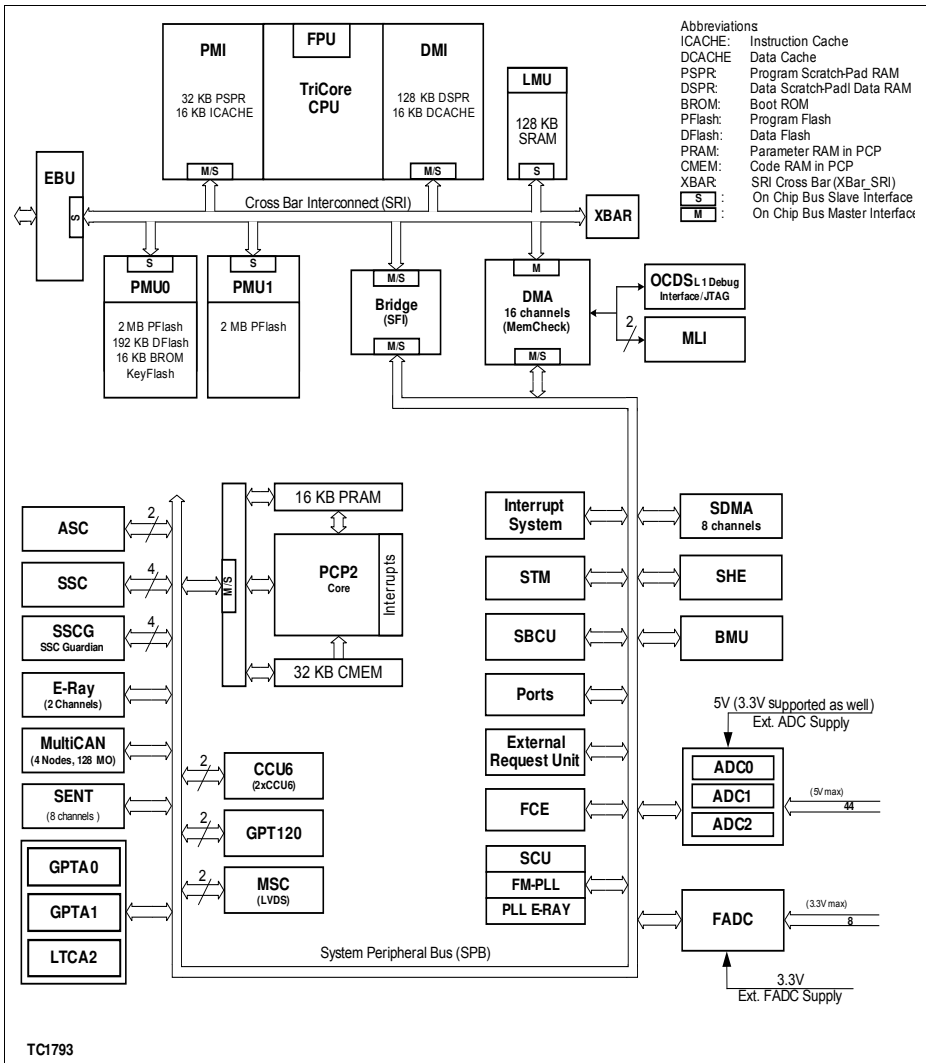


Figure 3 Block Diagram

### 3 Pinning

Figure 4 is showing the TC1793 Logic Symbol.

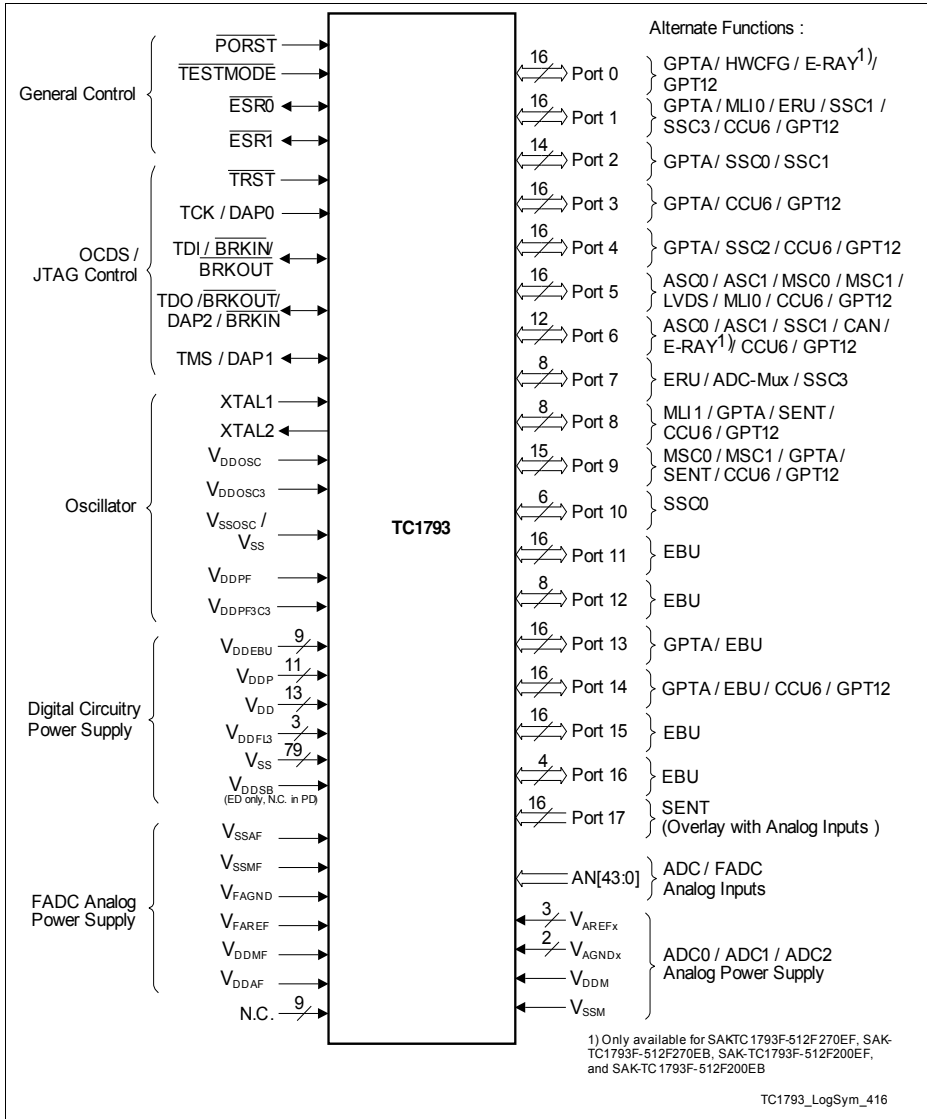


Figure 4 TC1793 Logic Symbol

Pinning TC1793 Pin Configuration

3.1 TC1793 Pin Configuration

This chapter shows the pin configuration of the TC1793 package PG-BGA- 416.

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26			
A	N.C.	P2.9	P2.13	P2.15	P0.14	P0.5	P0.2	P0.1	P0.0	P3.14	P3.5	P3.1	P5.1	P5.2	P5.7	P5.12	P5.15	V <sub>DDFL3</sub>	P9.0	P9.3	P9.9	ESR1	ESR0	N.C.	V <sub>DDP</sub>	V <sub>SS</sub>	A		
B	P2.6	P2.7	P2.10	P2.14	P0.9	P0.6	P0.4	P0.3	P3.15	P3.6	P3.3	P3.0	P5.0	P5.3	P5.6	P5.13	P5.14	V <sub>DDFL3</sub>	P9.1	P9.2	P9.10	PD RST	TEST MODE	V <sub>DDP</sub>	V <sub>SS</sub>	V <sub>DD</sub>	B		
C	P2.5	P2.8	P2.11	P2.12	P0.12	P0.10	P0.8	P0.7	P3.7	P3.10	P3.9	P3.4	P3.2	P5.5	P5.4	P5.9	P5.10	P5.11	P9.6	P9.8	P9.11	N.C.	V <sub>DDP</sub>	V <sub>SS</sub>	V <sub>DD</sub>	P9.13	C		
D	P2.4	P2.3	P2.2	P0.15	P0.13	P0.11	V <sub>DDP</sub>	V <sub>SS</sub>	V <sub>DD</sub>	P3.8	P3.12	P3.13	P3.11	V <sub>DDP</sub>	V <sub>SS</sub>	V <sub>DD</sub>	P5.8	P9.4	P9.5	P9.7	P9.12	V <sub>DDP</sub>	V <sub>SS</sub>	V <sub>DD</sub>	TDO	P9.14	D		
E	P6.12	P6.11	P6.6	P6.9																			V <sub>DD</sub>	TCK	TDI	V <sub>DD</sub>	osc3	E	
F	P6.14	P6.10	P6.4	P6.8																			TRST	TMS	V <sub>SS</sub>	osc	V <sub>DD</sub>	osc	F
G	P6.15	P6.13	P6.7	P6.5																			V <sub>DDP</sub>	V <sub>DDP</sub> F3	XTAL	2	XTAL	1	G
H	P8.1	P8.0	V <sub>DDFL3</sub>	V <sub>DD</sub>																			V <sub>DD</sub> DEBU	V <sub>DD</sub> DEBU	V <sub>DD</sub> DEBU	V <sub>DD</sub> DEBU	H		
J	P8.4	P8.3	P8.2	V <sub>SS</sub>																			P11.3	P12.6	P12.7	P11.0	J		
K	P8.7	P8.5	P8.6	V <sub>DDP</sub>	V <sub>SS</sub>																P11.7	P11.4	P11.1	P11.2	K				
L	P1.15	P1.14	P1.13	P1.11	V <sub>SS</sub>																V <sub>SS</sub>	P11.11	P11.5	P11.6	L				
M	P1.10	P1.9	P1.8	P1.5	V <sub>SS</sub>																V <sub>DD</sub> DEBU	P11.10	P11.9	P11.8	M				
N	P1.3	P1.7	P1.6	P1.4	V <sub>SS</sub>																P11.13	P11.14	P11.15	P11.12	N				
P	P1.2	P1.1	P1.0	P1.12	V <sub>SS</sub>																V <sub>DD</sub>	P12.1	P12.2	P12.0	P				
R	V <sub>DD</sub> SBRAM	P7.1	P7.0	V <sub>DD</sub>	V <sub>SS</sub>																V <sub>SS</sub>	P12.3	P12.5	P12.4	R				
T	P7.6	P7.5	P7.4	V <sub>SS</sub>	V <sub>SS</sub>																V <sub>DD</sub> DEBU	P13.1	P13.3	P13.0	T				
U	AN23	P7.7	P7.3	P7.2	V <sub>SS</sub>																P13.6	P13.9	P13.5	P13.2	U				
V	AN22	AN21	AN19	AN16																			V <sub>DD</sub>	P13.13	P13.8	P13.4	V		
W	AN20	AN17	AN13	V <sub>DDIM</sub>																			V <sub>SS</sub>	P14.0	P13.12	P13.7	W		
Y	AN18	AN14	AN10	V <sub>SSIM</sub>																			V <sub>DD</sub> DEBU	P14.2	P13.14	P13.10	Y		
AA	AN15	AN11	AN5	AN2																			P14.3	P14.6	P14.1	P13.11	AA		
AB	AN12	AN9	AN3	AN7																			V <sub>DD</sub>	P14.5	P14.4	P13.15	AB		
AC	AN8	AN4	AN32	AN38	AN42	V <sub>AREN1</sub>	AN26	AN24	V <sub>DDAF</sub>	V <sub>SS</sub>	V <sub>DD</sub>	P4.4	P4.8	P4.12	P10.5	V <sub>DDP</sub>	V <sub>SS</sub>	V <sub>DD</sub> DEBU	V <sub>SS</sub>	V <sub>DD</sub>	N.C.	V <sub>DD</sub> DEBU	V <sub>SS</sub>	P14.12	P14.9	P14.7	AC		
AD	AN6	AN1	AN34	AN40	AN35	V <sub>AREF1</sub>	AN27	AN25	V <sub>AREF2</sub>	P4.0	P4.2	P4.5	P4.11	P4.15	P10.2	V <sub>DDP</sub>	P15.5	P16.1	P15.3	P15.2	P15.1	P16.2	N.C.	P14.15	P14.11	P14.8	AD		
AE	AN0	AN33	AN36	AN41	V <sub>AREF0</sub>	AN28	AN30	V <sub>AREF2</sub>	V <sub>DDAF</sub>	P4.1	P4.3	P4.7	P4.13	P10.4	P10.0	V <sub>DDP</sub>	P15.4	P15.7	P16.3	P15.11	P15.0	N.C.	N.C.	P14.14	P14.13	P14.10	AE		
AF	N.C.	AN37	AN39	AN43	V <sub>AREF0</sub>	AN29	AN31	V <sub>AREF</sub>	V <sub>SSIM</sub>	P4.6	P4.9	P4.10	P4.14	P10.3	P10.1	V <sub>DDP</sub>	P16.0	P15.6	P15.12	P15.8	P15.9	P15.10	P15.13	P15.14	P15.15	N.C.	AF		
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26			

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Figure 5 TC1793 Pinning for PG-BGA- 416 Package

**Table 2 Pin Definitions and Functions**

Pin	Symbol	Ctrl.	Type	Function
<b>Port 0</b>				
A9	P0.0	I/O	A1+/ PU	<b>Port 0 General Purpose I/O Line 0</b>
	HWCFG0	I		<b>Hardware Configuration Input 0</b>
	OUT56	O1		<b>OUT56 Line of GPTA0</b>
	OUT56	O2		<b>OUT56 Line of GPTA1</b>
	OUT80	O3		<b>OUT80 Line of LTCA2</b>
A8	P0.1	I/O	A1/ PU	<b>Port 0 General Purpose I/O Line 1</b>
	HWCFG1	I		<b>Hardware Configuration Input 1</b>
	OUT57	O1		<b>OUT57 Line of GPTA0</b>
	OUT57	O2		<b>OUT57 Line of GPTA1</b>
	OUT81	O3		<b>OUT81 Line of LTCA2</b>
A7	P0.2	I/O	A2/ PU	<b>Port 0 General Purpose I/O Line 2</b>
	HWCFG2	I		<b>Hardware Configuration Input 2</b>
	OUT58	O1		<b>OUT58 Line of GPTA0</b>
	OUT58	O2		<b>OUT58 Line of GPTA1</b>
	OUT82	O3		<b>OUT82 Line of LTCA2</b>
B8	P0.3	I/O	A1/ PU	<b>Port 0 General Purpose I/O Line 3</b>
	HWCFG3	I		<b>Hardware Configuration Input 3</b>
	OUT59	O1		<b>OUT59 Line of GPTA0</b>
	OUT59	O2		<b>OUT59 Line of GPTA1</b>
	OUT83	O3		<b>OUT83 Line of LTCA2</b>



**Pinning TC1793 Pin Configuration**
**Table 2 Pin Definitions and Functions (cont'd)**

<b>Pin</b>	<b>Symbol</b>	<b>Ctrl.</b>	<b>Type</b>	<b>Function</b>
B7	P0.4	I/O	A1/ PU	<b>Port 0 General Purpose I/O Line 4</b>
	HWCFG4	I		<b>Hardware Configuration Input 4</b>
	OUT60	O1		<b>OUT60 Line of GPTA0</b>
	OUT60	O2		<b>OUT60 Line of GPTA1</b>
	EVTO0	O3		<b>MCDS Output Event 0<sup>1)</sup></b>
A6	P0.5	I/O	A1/ PU	<b>Port 0 General Purpose I/O Line 5</b>
	HWCFG5	I		<b>Hardware Configuration Input 5</b>
	OUT61	O1		<b>OUT61 Line of GPTA0</b>
	OUT61	O2		<b>OUT61 Line of GPTA1</b>
	EVTO1	O3		<b>MCDS Output Event 1<sup>1)</sup></b>
B6	P0.6	I/O	A2/ PU	<b>Port 0 General Purpose I/O Line 6</b>
	HWCFG6	I		<b>Hardware Configuration Input 6</b>
	OUT62	O1		<b>OUT62 Line of GPTA0</b>
	OUT62	O2		<b>OUT62 Line of GPTA1</b>
	EVTO2	O3		<b>MCDS Output Event 2<sup>1)</sup></b>
C8	P0.7	I/O	A1/ PU	<b>Port 0 General Purpose I/O Line 7</b>
	HWCFG7	I		<b>Hardware Configuration Input 7</b>
	OUT63	O1		<b>OUT63 Line of GPTA0</b>
	OUT63	O2		<b>OUT63 Line of GPTA1</b>
	EVTO3	O3		<b>MCDS Output Event 3<sup>1)</sup></b>
C7	P0.8	I/O	A1/ PU	<b>Port 0 General Purpose I/O Line 8</b>
	Reserved	O1		-
	Reserved	O2		-
	Reserved	O3		-

## Pinning TC1793 Pin Configuration

**Table 2 Pin Definitions and Functions (cont'd)**

Pin	Symbol	Ctrl.	Type	Function
B5	P0.9	I/O	A1/ PU	<b>Port 0 General Purpose I/O Line 9</b>
	RXDA0	I		<b>E-Ray Channel A Receive Data Input 0<sup>2)</sup></b>
	Reserved	O1		-
	Reserved	O2		-
	Reserved	O3		-
C6	P0.10	I/O	A2/ PU	<b>Port 0 General Purpose I/O Line 10</b>
	TXENA	O1		<b>E-Ray Channel A transmit Data Output enable<sup>2)</sup></b>
	Reserved	O2		-
	Reserved	O3		-
D6	P0.11	I/O	A2/ PU	<b>Port 0 General Purpose I/O Line 11</b>
	T5INB	I		<b>GPT120</b>
	T5INA	I		<b>GPT121</b>
	TXENB	O1		<b>E-Ray Channel B transmit Data Output enable<sup>2)</sup></b>
	Reserved	O2		-
	Reserved	O3		-
C5	P0.12	I/O	A2/ PU	<b>Port 0 General Purpose I/O Line 12</b>
	T5EUDA	I		<b>GPT120</b>
	T5EUDB	I		<b>GPT121</b>
	TXDB	O1		<b>E-Ray Channel B transmit Data Output<sup>2)</sup></b>
	Reserved	O2		-
	Reserved	O3		-