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TC1796

32-Bit Single-Chip Microcontroller

TriCore

Microcontrollers

Never stop thinking

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TC1796 Data Sheet

Revision History: V1.0, 2008-04

Previous Version: V1.0, 2008-04 “Preliminary”	
Page	Subjects (major changes since last revision)
	“Preliminary” status removed. No changes in content.
Changes from V0.7, 2006-03 to V1.0, 2008-04 Preliminary	
32	The list of not connected pins (N.C.) improved by adding several formerly as V_{SS} labeled pins.
69	Watchdog timer, double reset detection, description corrected.
80	RTID register updated for the design step BE.
85	The description of the inactive device current improved.
96	ADC parameters sample and conversion time moved to a dedicated table.
107	The description of the power supply sequence improved..
115	BFCLKO clock, duty cycle description extended.
126	MLI timing, maximum operating frequency limit extended, t31 added.
131	The drawing of the package updated. Green package variant included.
133	Example of a temperature profile corrected.

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Table of Contents

1 Summary of Features

- High-performance 32-bit super-scalar TriCore V1.3 CPU with 4-stage pipeline
  - Superior real-time performance
  - Strong bit handling
  - Fully integrated DSP capabilities
  - Single precision Floating Point Unit (FPU)
  - 150 MHz operation at full temperature range
- 32-bit Peripheral Control Processor with single cycle instruction (PCP2)
  - 16 Kbyte Parameter Memory (PRAM)
  - 32 Kbyte Code Memory (CMEM)
- Multiple on-chip memories
  - 2 Mbyte Program Flash Memory (PFLASH) with ECC
  - 128 Kbyte Data Flash Memory (DFLASH) usable for EEPROM emulation
  - 136 Kbyte Data Memory (LDRAM, SRAM, SBRAM)
  - 8 Kbyte Dual-Ported Memory (DPRAM)
  - 48 Kbyte Code Scratchpad Memory (SPRAM)
  - 16 Kbyte Instruction Cache (ICACHE)
  - 16 Kbyte BootROM (BROM)
- 16-Channel DMA Controller
- 32-bit External Bus Interface Unit (EBU) with
  - 75 dedicated address/data bus, clock, and control lines
  - Synchronous burst Flash access capability
- Sophisticated interrupt system with 2×255 hardware priority arbitration levels serviced by CPU or PCP2
- High performing on-chip bus structure
  - Two 64-bit Local Memory Buses between EBU, Flash and Data Memory
  - 32-bit System Peripheral Bus (SPB) for on-chip peripheral and functional units
  - 32-bit Remote Peripheral Bus (RPB) for high-speed on-chip peripheral units
  - Two bus bridges (LFI Bridge, DMA Controller)
- Peripheral Control Processor with single cycle instruction (PCP2)
  - 16 Kbyte Parameter Memory (PRAM)
  - 32 Kbyte Code Memory (CMEM)
- Versatile On-chip Peripheral Units
  - Two Asynchronous/Synchronous Serial Channels (ASC) with baud rate generator, parity, framing and overrun error detection
  - Two High-Speed Synchronous Serial Channels (SSC) with programmable data length and shift direction
  - Two serial Micro Second Bus interfaces (MSC) for serial port expansion to external power devices
  - Two High-Speed Micro Link interfaces (MLI) for serial inter-processor communication

  - One MultiCAN Module with four CAN nodes and 128 free assignable message objects for high efficiency data handling via FIFO buffering and gateway data transfer (one CAN node supports TTCAN functionality)
  - Two General Purpose Timer Array Modules (GPTA) with additional Local Timer Cell Array (LTCA2) providing a powerful set of digital signal filtering and timer functionality to realize autonomous and complex Input/Output management
  - Two 16-channel Analog-to-Digital Converter units (ADC) with selectable 8-bit, 10-bit, or 12-bit resolution
  - One 4-channel Fast Analog-to-Digital Converter unit (FADC) with concatenated comb filters for hardware data reduction: supporting 10-bit resolution, min. conversion time of 280ns
- 44 analog input lines for ADC and FADC
- 123 digital general purpose I/O lines, 4 input lines
- Digital I/O ports with 3.3 V capability
- On-chip debug support for OCDS Level 1 and 2 (CPU, PCP3, DMA)
- Dedicated Emulation Device chip for multi-core debugging, tracing, and calibration via USB V1.1 interface available (TC1796ED)
- Power Management System
- Clock Generation Unit with PLL
- Core supply voltage of 1.5 V
- I/O voltage of 3.3 V
- Full automotive temperature range: -40° to +125°C
- P/PG-BGA-416-4 package

Ordering Information

The ordering code for Infineon microcontrollers provides an exact reference to the required product. This ordering code identifies:

- The derivative itself, i.e. its function set, the temperature range, and the supply voltage
- The package and the type of delivery.

For the available ordering codes for the TC1796 please refer to the **“Product Catalog Microcontrollers”**, which summarizes all available microcontroller variants.

This document describes the derivatives of the device.The **Table 1** enumerates these derivatives and summarizes the differences.

Table 1 TC1796 Derivative Synopsis

Derivative	Ambient Temperature Range
SAK-TC1796-256F150E	T_A = -40°C to +125°C

2 General Device Information

2.1 TC1796 Block Diagram

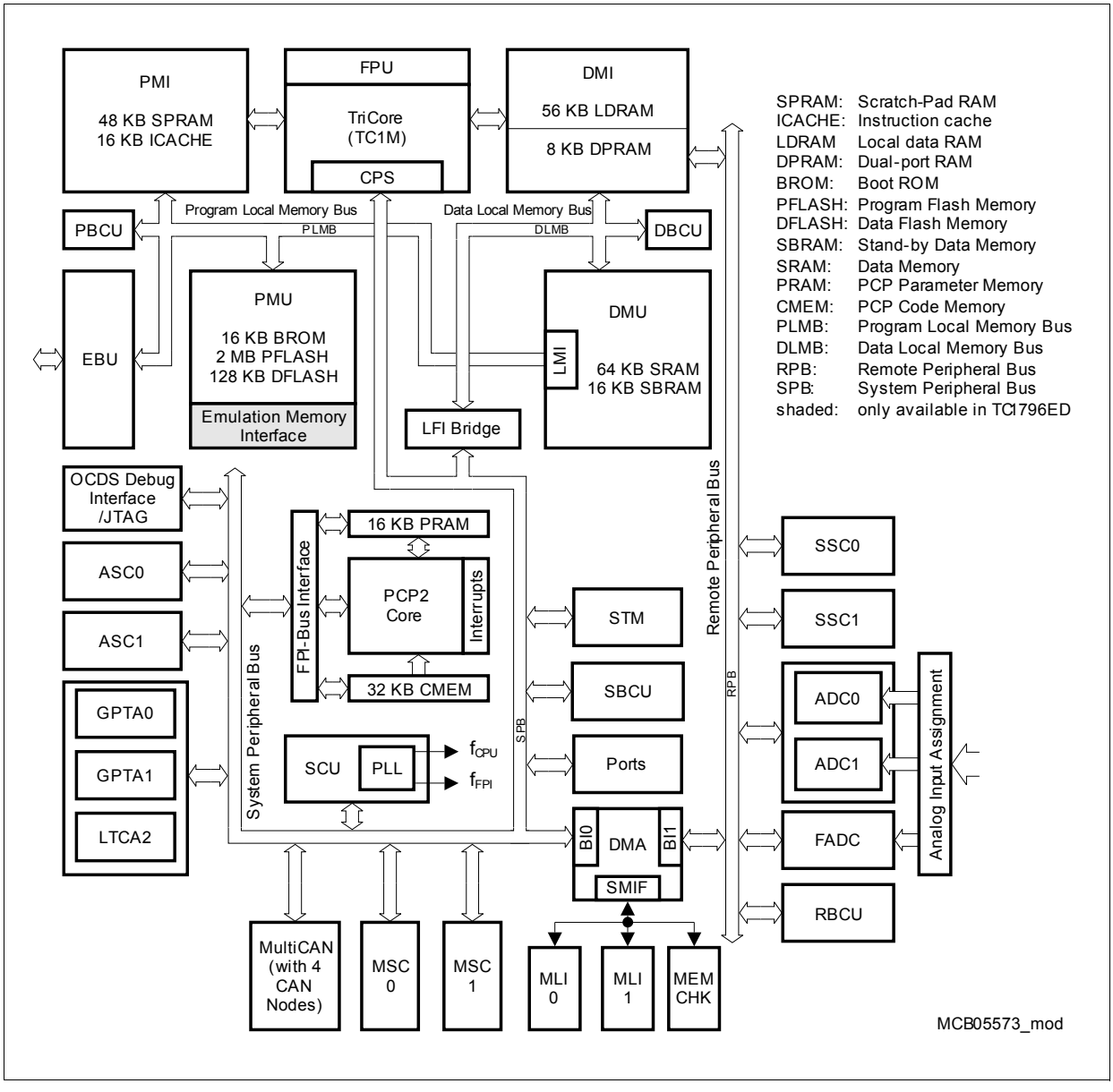

Figure 1 TC1796 Block Diagram

2.2 Logic Symbol

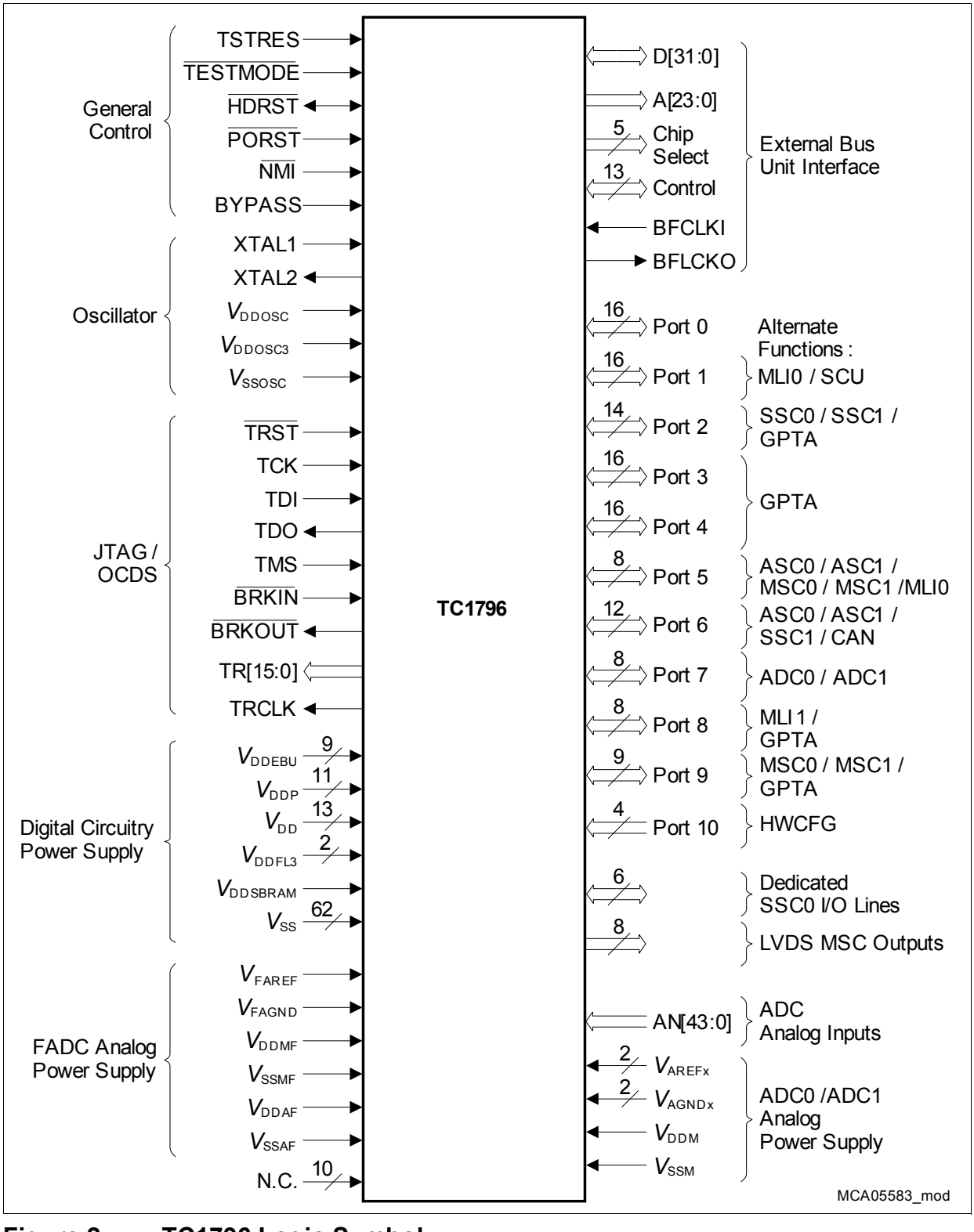

Figure 2 TC1796 Logic Symbol

2.3 Pin Configuration

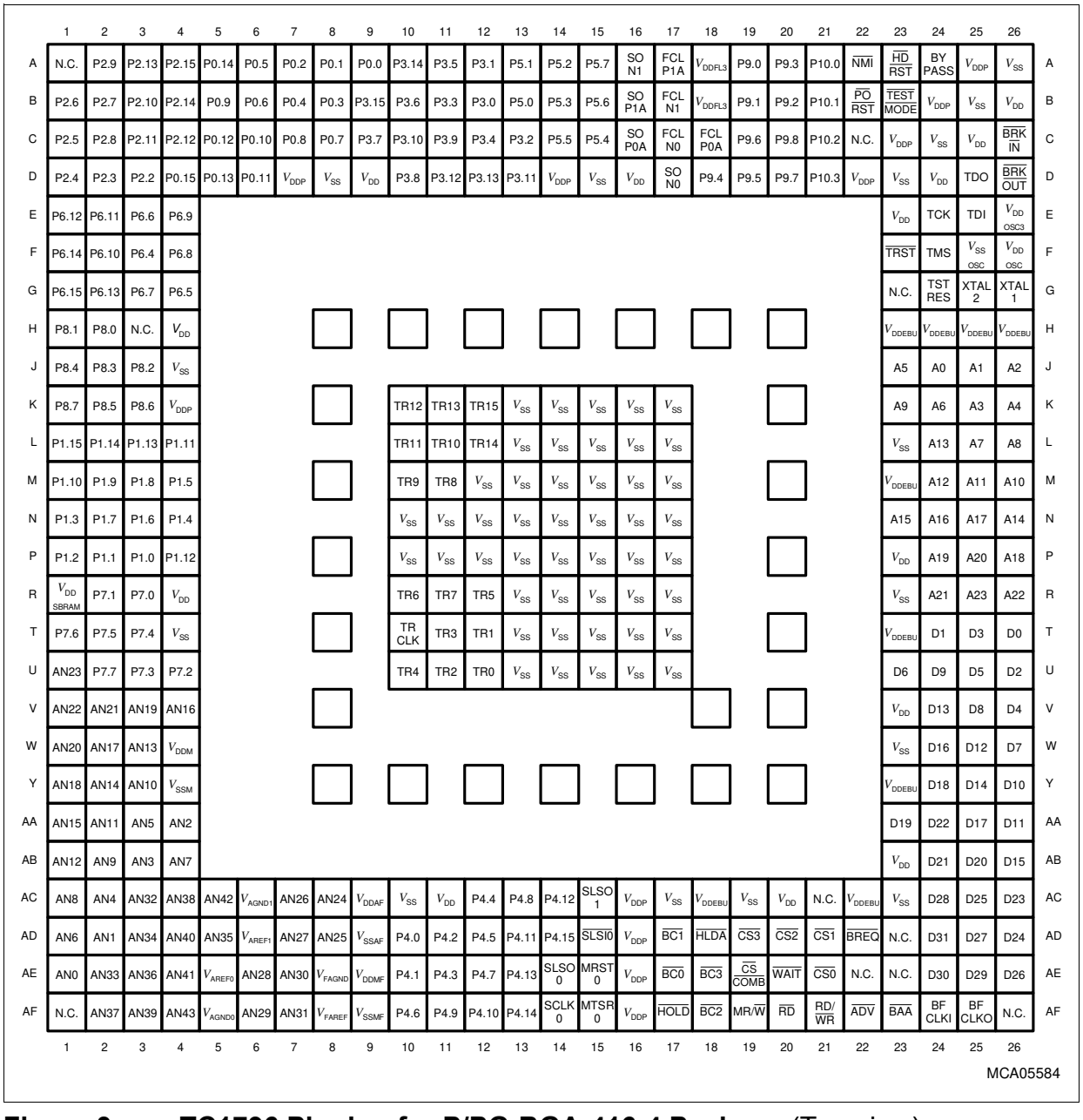

Figure 3 TC1796 Pinning for P/PG-BGA-416-4 Package (Top view)

2.4 Pad Driver and Input Classes Overview

The TC1796 provides different types and classes of input and output lines. For understanding of the abbreviations in **Table 2** starting at the next page, **Table 4** gives an overview on the pad type and class types.

2.5 Pin Definitions and Functions

Table 2 Pin Definitions and Functions

Symbol	Pins	I/O	Pad Class	Power Supply	Functions
External Bus Interface Lines (EBU)					
D[31:0]		I/O	B1	V_{DDEBU}	**EBU Data Bus Lines** The EBU Data Bus Lines D[31:0] serve as external data bus.
D0	T26	I/O			Data bus line 0
D1	T24	I/O			Data bus line 1
D2	U26	I/O			Data bus line 2
D3	T25	I/O			Data bus line 3
D4	V26	I/O			Data bus line 4
D5	U25	I/O			Data bus line 5
D6	U23	I/O			Data bus line 6
D7	W26	I/O			Data bus line 7
D8	V25	I/O			Data bus line 8
D9	U24	I/O			Data bus line 9
D10	Y26	I/O			Data bus line 10
D11	AA26	I/O			Data bus line 11
D12	W25	I/O			Data bus line 12
D13	V24	I/O			Data bus line 13
D14	Y25	I/O			Data bus line 14
D15	AB26	I/O			Data bus line 15
D16	W24	I/O			Data bus line 16
D17	AA25	I/O			Data bus line 17
D18	Y24	I/O			Data bus line 18
D19	AA23	I/O			Data bus line 19
D20	AB25	I/O			Data bus line 20
D21	AB24	I/O			Data bus line 21
D22	AA24	I/O			Data bus line 22
D23	AC26	I/O			Data bus line 23
D24	AD26	I/O			Data bus line 24
D25	AC25	I/O			Data bus line 25
D26	AE26	I/O			Data bus line 26
D27	AD25	I/O			Data bus line 27
D28	AC24	I/O			Data bus line 28
D29	AE25	I/O			Data bus line 29
D30	AE24	I/O			Data bus line 30
D31	AD24	I/O			Data bus line 31

Table 2 Pin Definitions and Functions (cont'd)

Symbol	Pins	I/O	Pad Class	Power Supply	Functions
A[23:0]		O	B1	V_{DDEBU}	**EBU Address Bus Lines A[23:0]** The EBU Address Bus Lines serve as external address bus.
A0	J24	O			Address bus line 0
A1	J25	O			Address bus line 1
A2	J26	O			Address bus line 2
A3	K25	O			Address bus line 3
A4	K26	O			Address bus line 4
A5	J23	O			Address bus line 5
A6	K24	O			Address bus line 6
A7	L25	O			Address bus line 7
A8	L26	O			Address bus line 8
A9	K23	O			Address bus line 9
A10	M26	O			Address bus line 10
A11	M25	O			Address bus line 11
A12	M24	O			Address bus line 12
A13	L24	O			Address bus line 13
A14	N26	O			Address bus line 14
A15	N23	O			Address bus line 15
A16	N24	O			Address bus line 16
A17	N25	O			Address bus line 17
A18	P26	O			Address bus line 18
A19	P24	O			Address bus line 19
A20	P25	O			Address bus line 20
A21	R24	O			Address bus line 21
A22	R26	O			Address bus line 22
A23	R25	O			Address bus line 23
			B1	V_{DDEBU}	**Chip Select Output Lines**
$\overline{CS0}$	AE21	O			Chip select output line 0
$\overline{CS1}$	AD21	O			Chip select output line 1
$\overline{CS2}$	AD20	O			Chip select output line 2
$\overline{CS3}$	AD19	O			Chip select output line 3
$\overline{CS}$ COMB	AE19	O	B1	V_{DDEBU}	**Combined Chip Select Output for Global Select / Emulator Memory Region/Emulator Overlay Memory**

Table 2 Pin Definitions and Functions (cont'd)

Symbol	Pins	I/O	Pad Class	Power Supply	Functions
BFCLKO	AF25	O	B2	V_{DDEBU}	**Burst Mode Flash Clock Output (non-differential)**
BFCLKI	AF24	I	B1		**Burst Mode Flash Clock Input** (feedback clock)
$\overline{RD}$	AF20	O	B1		**Read Control Line**
RD/$\overline{WR}$	AF21	O	B1		**Write Control Line**
$\overline{ADV}$	AF22	O	B1		Address Valid Output
MR/$\overline{W}$	AF19	O	B1		**Motorola-style Read/Write Control Signal**
			B1		**Byte Control Lines**
$\overline{BC0}$	AE17	O			Byte control line 0
$\overline{BC1}$	AD17	O			Byte control line 1
$\overline{BC2}$	AF18	O			Byte control line 2
$\overline{BC3}$	AE18	O			Byte control line 3
$\overline{WAIT}$	AE20	I	B1		**Wait Input for inserting Wait-States**
$\overline{BAA}$	AF23	O	B1		**Burst Address Advance Output**
$\overline{HOLD}$	AF17	I	B1		**Hold Request Input**
$\overline{HLDA}$	AD18	O	B1		**Hold Acknowledge Output**
$\overline{BREQ}$	AD22	O	B1		**Bus Request Output**

Table 2 Pin Definitions and Functions (cont'd)

Symbol	Pins	I/O	Pad Class	Power Supply	Functions
Parallel Ports					
P0		I/O	A1	V_{DDP}	**Port 0** Port 0 is a 16-bit bidirectional general-purpose I/O port.
P0.0	A9	I/O			Port 0 I/O line 0
P0.1	A8	I/O			Port 0 I/O line 1
P0.2	A7	I/O			Port 0 I/O line 2
P0.3	B8	I/O			Port 0 I/O line 3
P0.4	B7	I/O			Port 0 I/O line 4
P0.5	A6	I/O			Port 0 I/O line 5
P0.6	B6	I/O			Port 0 I/O line 6
P0.7	C8	I/O			Port 0 I/O line 7
P0.8	C7	I/O			Port 0 I/O line 8
P0.9	B5	I/O			Port 0 I/O line 9
P0.10	C6	I/O			Port 0 I/O line 10
P0.11	D6	I/O			Port 0 I/O line 11
P0.12	C5	I/O			Port 0 I/O line 12
P0.13	D5	I/O			Port 0 I/O line 13
P0.14	A5	I/O			Port 0 I/O line 14
P0.15	D4	I/O			Port 0 I/O line 15 The states of the Port 0 pins are latched into the software configuration input register SCU_SCILR at the rising edge of $\overline{\text{HDRST}}$. Therefore, Port 0 pins can be used for operating mode selections by software.

Table 2 Pin Definitions and Functions (cont'd)

Symbol	Pins	I/O	Pad Class	Power Supply	Functions	
P1		I/O	A1/A2	V_{DDP}	**Port 1** Port 1 is a 16-bit bi-directional general-purpose I/O port which can be alternatively used for the MLI0 interface or as external trigger input lines.	
P1.0	P3	I	A1		REQ0	External trigger input 0
P1.1	P2	I	A1		REQ1	External trigger input 1
P1.2	P1	I	A1		REQ2	External trigger input 3
P1.3	N1	I	A1		REQ3	External trigger input 2
		I	A1		TREADY0B	MLI0 transmit channel ready input B
P1.4	N4	O	A2		TCLK0	MLI0 transmit channel clock output
P1.5	M4	I	A1		TREADY0A	MLI0 transmit channel ready input A
P1.6	N3	O	A2		TVALID0A	MLI0 transmit channel valid output A
P1.7	N2	O	A2		TDATA0	MLI0 transmit channel data output
P1.8	M3	I	A1		RCLK0A	MLI0 receive channel clock input A
P1.9	M2	O	A2		RREADY0A	MLI0 receive channel ready output A
P1.10	M1	I	A1		RVALID0A	MLI0 receive channel valid input A
P1.11	L4	I	A1		RDATA0A	MLI0 receive channel data input A
P1.12	P4	O	A2		SYSCLK	System clock output
P1.13	L3	I	A1		RCLK0B	MLI0 receive channel clock input B
P1.14	L2	I	A1		RVALID0B	MLI0 receive channel valid input B
P1.15	L1	I	A1		RDATA0B	MLI0 receive channel data input B

Table 2 Pin Definitions and Functions (cont'd)

Symbol	Pins	I/O	Pad Class	Power Supply	Functions
P2		I/O	A1/A2	V_{DDP}	**Port 2** Port 2 is a 14-bit bi-directional general-purpose I/O port which can be used alternatively for the six upper SSC slave select outputs or for GPTA I/O lines.
P2.2	D3	O	A2		SLSO2 Slave select output line 2
P2.3	D2	O	A2		SLSO3 Slave select output line 3
P2.4	D1	O	A2		SLSO4 Slave select output line 4
P2.5	C1	O	A2		SLSO5 Slave select output line 5
P2.6	B1	O	A2		SLSO6 Slave select output line 6
P2.7	B2	O	A2		SLSO7 Slave select output line 7
P2.8	C2	I/O	A1		IN0 / OUT0 line of GPTA
P2.9	A2	I/O	A1		IN1 / OUT1 line of GPTA
P2.10	B3	I/O	A1		IN2 / OUT2 line of GPTA
P2.11	C3	I/O	A1		IN3 / OUT3 line of GPTA
P2.12	C4	I/O	A1		IN4 / OUT4 line of GPTA
P2.13	A3	I/O	A1		IN5 / OUT5 line of GPTA
P2.14	B4	I/O	A1		IN6 / OUT6 line of GPTA
P2.15	A4	I/O	A1		IN7 / OUT7 line of GPTA

Table 2 Pin Definitions and Functions (cont'd)

Symbol	Pins	I/O	Pad Class	Power Supply	Functions
P3		I/O	A1	V_{DDP}	**Port 3** Port 3 is a 16-bit bi-directional general-purpose I/O port which can be alternatively used for GPTA I/O lines.
P3.0	B12				IN8 / OUT8 line of GPTA
P3.1	A12				IN9 / OUT9 line of GPTA
P3.2	C13				IN10 / OUT10 line of GPTA
P3.3	B11				IN11 / OUT11 line of GPTA
P3.4	C12				IN12 / OUT12 line of GPTA
P3.5	A11				IN13 / OUT13 line of GPTA
P3.6	B10				IN14 / OUT14 line of GPTA
P3.7	C9				IN15 / OUT15 line of GPTA
P3.9	D10				IN16 / OUT16 line of GPTA
P3.8	C11				IN17 / OUT17 line of GPTA
P3.10	C10				IN18 / OUT18 line of GPTA
P3.11	D13				IN19 / OUT19 line of GPTA
P3.12	D11				IN20 / OUT20 line of GPTA
P3.13	D12				IN21 / OUT21 line of GPTA
P3.14	A10				IN22 / OUT22 line of GPTA
P3.15.	B9				IN23 / OUT23 line of GPTA

Table 2 Pin Definitions and Functions (cont'd)

Symbol	Pins	I/O	Pad Class	Power Supply	Functions
P4		I/O	A1/A2	V_{DDP}	**Port 4** Port 4 is a 16-bit bi-directional general-purpose I/O port which can be alternatively used for GPTA I/O lines.
P4.0	AD10	I/O	A2[1)]		IN24 / OUT24 line of GPTA
P4.1	AE10	I/O	A2[1)]		IN25 / OUT25 line of GPTA
P4.2	AD11	I/O	A2[1)]		IN26 / OUT26 line of GPTA
P4.3	AE11	I/O	A2[1)]		IN27 / OUT27 line of GPTA
P4.4	AC12	I/O	A2[1)]		IN28 / OUT28 line of GPTA
P4.5	AD12	I/O	A2[1)]		IN29 / OUT29 line of GPTA
P4.6	AF10	I/O	A2[1)]		IN30 / OUT30 line of GPTA
P4.7	AE12	I/O	A2[1)]		IN31 / OUT31 line of GPTA
P4.8	AC13	I/O	A1		IN32 / OUT32 line of GPTA
P4.9	AF11	I/O	A1		IN33 / OUT33 line of GPTA
P4.10	AF12	I/O	A1		IN34 / OUT34 line of GPTA
P4.11	AD13	I/O	A1		IN35 / OUT35 line of GPTA
P4.12	AC14	I/O	A1		IN36 / OUT36 line of GPTA
P4.13	AE13	I/O	A1		IN37 / OUT37 line of GPTA
P4.14	AF13	I/O	A1		IN38 / OUT38 line of GPTA
P4.15	AD14	I/O	A1		IN39 / OUT39 line of GPTA

Table 2 Pin Definitions and Functions (cont'd)

Symbol	Pins	I/O	Pad Class	Power Supply	Functions	
P5		I/O	A2	V_{DDP}	**Port 5** Port 5 is an 8-bit bi-directional general-purpose I/O port which can be alternatively used for ASC0/1 or MSC0/1 lines.	
P5.0	B13	I/O			RXD0A	ASC0 receiver input / output A
P5.1	A13	O			TXD0A	ASC0 transmitter output A
P5.2	A14	I/O			RXD1A	ASC1 receiver input / output A
P5.3	B14	O			TXD1A	ASC1 transmitter output A P5.3 is latched with the rising edge of $\overline{\text{PORST}}$ if BYPASS = 1 and stored in inverted state as bit OSC_CON.MOSC.
P5.4	C15	O			EN00	MSC0 device select output 0
		O			RREADY0B	MLI0 receive channel ready output B
P5.5	C14	I			SDI0	MSC0 serial data input
P5.6	B15	O			EN10	MSC1 device select output 0
		O			TVALID0B	MLI0 transmit channel valid output B
P5.7	A15	I			SDI1	MSC1 serial data input

Table 2 Pin Definitions and Functions (cont'd)

Symbol	Pins	I/O	Pad Class	Power Supply	Functions	
P6		I/O	A2	V_{DDP}	**Port 6** Port 6 is a 12-bit bi-directional general-purpose I/O port which can be alternatively used for SSC1, ASC0/1, and CAN I/O lines.	
P6.4	F3	O I			MTSR1	SSC1 master transmit output / SSC1 slave receive input
P6.5	G4	I O			MRST1	SSC1 master receive input / SSC1 slave transmit output
P6.6	E3	I/O			SCLK1	SSC1 clock input / output
P6.7	G3	I			SLSI1	SSC1 slave select input
P6.8	F4	I I/O			RXDCAN0 RXD0B	CAN node 0 receiver input ASC0 receiver input / output B
P6.9	E4	O O			TXDCAN0 TXD0B	CAN node 0 transmitter output ASC0 transmitter output B
P6.10	F2	I I/O			RXDCAN1 RXD1B	CAN node 1 receiver input ASC1 receiver input / output B
P6.11	E2	O O			TXDCAN1 TXD1B	CAN node 1 transmitter output ASC1 transmitter output B
P6.12	E1	I			RXDCAN2	CAN node 2 receiver input
P6.13	G2	O			TXDCAN2	CAN node 2 transmitter output
P6.14	F1	I			RXDCAN3	CAN node 3 receiver input
P6.15	G1	O			TXDCAN3	CAN node 3 transmitter output

Table 2 Pin Definitions and Functions (cont'd)

Symbol	Pins	I/O	Pad Class	Power Supply	Functions	
P7		I/O	A1	V_{DDP}	**Port 7** Port 7 is an 8-bit bi-directional general-purpose I/O port which can be alternatively used as external trigger input lines and for ADC0/1 external multiplexer control.	
P7.0	R3	I			REQ4	External trigger input 4
P7.1	R2	I			REQ5	External trigger input 5
		O			AD0EMUX2	ADC0 external multiplexer control output 2
P7.2	U4	O			AD0EMUX0	ADC0 external multiplexer control output 0
P7.3	U3	O			AD0EMUX2	ADC0 external multiplexer control output 1
P7.4	T3	I			REQ6	External trigger input 6
P7.5	T2	I			REQ7	External trigger input 7
P7.6	T1	O			AD1EMUX0	ADC1 external multiplexer control output 0
P7.7	U2	O			AD1EMUX1	ADC1 external multiplexer control output 1

Table 2 Pin Definitions and Functions (cont'd)

Symbol	Pins	I/O	Pad Class	Power Supply	Functions	
P8		I/O	A1/A2	V_{DDP}	**Port 8** Port 8 is an 8-bit bi-directional general-purpose I/O port which can be alternatively used for the MLI1 interface or as GPTA I/O lines.	
P8.0	H2	O	A2		TCLK1	MLI1 transmit channel clock output
		I/O	A2		IN40/OUT40	I/O line of GPTA
P8.1	H1	I	A1		TREADY1A	MLI1 transmit channel ready input A
		I/O	A1		IN41/OUT41	I/O line of GPTA
P8.2	J3	O	A2		TVALID1A	MLI1 transmit channel valid output A
		I/O	A2		IN42/OUT42	I/O line of GPTA
P8.3	J2	O	A2		TDATA1	MLI1 transmit channel data output
		I/O	A2		IN43/OUT43	I/O line of GPTA
P8.4	J1	I	A1		RCLK1A	MLI1 receive channel clock input A
		I/O	A1		IN44/OUT44	I/O line of GPTA
P8.5	K2	O	A2		RREADY1A	MLI1 receive channel ready output A
		I/O	A2		IN45/OUT45	I/O line of GPTA
P8.6	K3	I	A1		RVALID1A	MLI1 receive channel validinput A
		I/O	A1		IN46/OUT46	I/O line of GPTA
P8.7	K1	I	A1		RDATA1A	MLI1 receive channel data input A
		I/O	A1		IN47/OUT47	I/O line of GPTA