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32-Bit

Microcontroller

TC290 / TC297 / TC298 / TC299

32-Bit Single-Chip Micocontroller
BB-Step

32-Bit Single-Chip Micocontroller

Data Sheet

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Microcontrollers

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Table of Contents

1 Summary of Features

The **TC29x** product family has the following features:

- High Performance Microcontroller with three CPU cores
- One 32-bit super-scalar TriCore CPUs (TC1.6P), having the following features:
  - Superior real-time performance
  - Strong bit handling
  - Fully integrated DSP capabilities
  - Multiply-accumulate unit able to sustain 2 MAC operations per cycle
  - up to 300 MHz operation at full temperature range
  - up to 120 / 240 Kbyte Data Scratch-Pad RAM (DSPR)
  - up to 32 Kbyte Instruction Scratch-Pad RAM (PSPR)
  - 16 / 32 Kbyte Instruction Cache (ICACHE)
  - 8 Kbyte Data Cache (DCACHE)
- Lockstepped shadow core for TC1.6P core 1
- Multiple on-chip memories
  - All embedded NVM and SRAM are ECC protected
  - up to 8 Mbyte Program Flash Memory (PFLASH)
  - up to 768 Kbyte Data Flash Memory (DFLASH) usable for EEPROM emulation
  - 32 Kbyte Memory (LMU)
  - BootROM (BROM)
- 128-Channel DMA Controller with safe data transfer
- Sophisticated interrupt system (ECC protected)
- High performance on-chip bus structure
  - 64-bit Cross Bar Interconnect (SRI) giving fast parallel access between busmasters, CPUs and memories
  - 32-bit System Peripheral Bus (SPB) for on-chip peripheral and functional units
  - One bus bridge (SFI Bridge)
- Safety Management Unit (SMU) handling safety monitor alarms
- Memory Test Unit with ECC, Memory Initialization and MBIST functions (MTU)
- Hardware I/O Monitor (IOM) for checking of digital I/O
- Versatile On-chip Peripheral Units
  - Four Asynchronous/Synchronous Serial Channels (ASCLIN) with hardware LIN support (V1.3, V2.0, V2.1 and J2602) up to 50 MBaud
  - Six Queued SPI Interface Channels (QSPI) with master and slave capability upto 50 Mbit/s
  - High Speed Serial Link (HSSL) for serial inter-processor communication up to 320Mbit/s
  - Two serial Micro Second Bus interfaces (MSC) for serial port expansion to external power devices
  - Two MultiCAN+ Module with 6 CAN nodes and 384 free assignable messageobjects for high efficiency data handling via FIFO buffering and gateway data transfer
  - 15 Single Edge Nibble Transmission (SENT) channels for connection to sensors
  - Up to two FlexRay™module with 2 channels (E-Ray) supporting V2.1
  - One Generic Timer Module (GTM) providing a powerful set of digital signal filteringand timer functionality to realize autonomous and complex Input/Output management
  - One Capture / Compare 6 module (Two kernels CCU60 and CCU61)

  - One General Purpose 12 Timer Unit (GPT120)
  - Five channel Peripheral Sensor Interface conforming to V1.3 (PSI5)
  - Peripheral Sensor Interface with Serial PHY (PSI5-S)
  - Inter-Integrated Circuit Bus Interface (I2C) conforming to V2.1
  - Optional IEEE802.3 Ethernet MAC with RMII and MII interfaces (ETH)
- Versatile Successive Approximation ADC (VADC)
  - Cluster of 11 independent ADC kernels
  - Input voltage range from 0 V to 5.5V (ADC supply)
- Delta-Sigma ADC (DSADC)
  - ten channels
- Digital programmable I/O ports
- On-chip debug support for OCDS Level 1 (CPUs , DMA, On Chip Buses)
- Dedicated Emulation Device chip available (ED)
  - multi-core debugging, real time tracing, and calibration
  - Aurora Gigabit Trace Port (AGBT) on some variants (See below)
  - four/five wire JTAG (IEEE 1149.1) or DAP (Device Access Port) interface
- Power Management System and on-chip regulators
- Clock Generation Unit with System PLL and Flexray PLL
- Embedded Voltage Regulator

Ordering Information

The ordering code for Infineon microcontrollers provides an exact reference to the required product. This ordering code identifies:

- The derivative itself, i.e. its function set, the temperature range, and the supply voltage
- The package and the type of delivery.

For the available ordering codes for the TC290 / TC297 / TC298 / TC299 please refer to the **“AURIX TC29x Microcontrollers Variant Overview”**, which summarizes all available variants.

Table 1-1 Overview of TC29x Functions

Feature		
CPU Core	Type	TC1.6P
	P Cores / Checker Cores	3 / 1
	Max. Freq.	300 MHz
	FPU	yes
Program Flash	Size	8 Mbyte
Data Flash	Size	768 Kbyte
Cache	Instruction	16/ 32 / 32 Kbyte
	Data	8 Kbyte

Table 1-1 Overview of TC29x Functions

Feature		
SRAM	Size TC1.6P (DPSR/PSPR)	120 Kbyte / 32 Kbyte[1) 2)] 240 Kbyte / 32 Kbyte 240 Kbyte / 32 Kbyte
	Size LMU	32 Kbyte
DMA	Channels	128
ADC	Channels	72 + 12
	Converter	11
DSADC	Channels	10
GTM	TIM	6
	TOM	5
	ATOM / MCS	9 / 6
	CMU / ICM	1 / 1
	PSM	2
	TBU	1
	SPE	4
	CMP / MON	1 / 1
	BRC / DPLL	1 / 1
Timer	GPT12	1
	CCU6	2
STM	Modules	3
FlexRay	Modules	2
	Channels	4
CAN	Nodes	6
	Message Objects	384
QSPI	Channels	6
ASCLIN	Interfaces	4
I2C	Interfaces	2
SENT	Modules	15
PSI5	Channels	5
PSI5-S	Modules	1
HSSL	Channels	1
MSC	Channels	3
Ethernet	Channels	1
ASIL	Level	up to ASIL-D
FCE	Modules	1
Safety Support	SMU	1
	IOM	1

Table 1-1 Overview of TC29x Functions

Feature		
ADAS		Yes
Embedded Voltage Regulator	DCDC from 5 V/ 3.3 V to 1.3 V	Yes
Embedded Voltage Regulator	LDO from 5 V / 3.3 V to 1.3 V	Yes
Embedded Voltage Regulator	LDO from 5 V to 3.3 V	Yes
Low Power Features	Standby RAM	Yes
Packages	Type	LF-BGA-292-6 / PG-BGA-416-26 / PG-LFBGA-516-5
I/O	Type	5 V CMOS / 3.3 V CMOS / LVDS
$T_{ambient}$	Range	-40 ... + 125°C / + 150°C / + 170°C

1) Address range starts at lowest address defined in the User's Manual. For reference see the Memory Maps chapter of the User's Manual.

2) To ensure the processor cores are provided with a constant stream of instructions the Instruction Fetch Units will speculatively fetch instructions from the up to 64 bytes ahead of the current PC.
If the current PC is within 64 bytes of the top of an instruction memory the Instruction Fetch Unit may attempt to speculatively fetch instruction from beyond the physical range. This may then lead to error conditions and alarms being triggered by the bus and memory systems.
It is therefore recommended that the upper 64 bytes of any memory be unused for instruction storage.

2 Package and Pinning Definitions

This chapter gives a pinning of the different packages of the TC290 / TC297 / TC298 / TC299.

2.1 TC299x Pin Definition and Functions: BGA516

Figure 2-1 is showing the TC299x Logic Symbol for the package variant: BGA516.

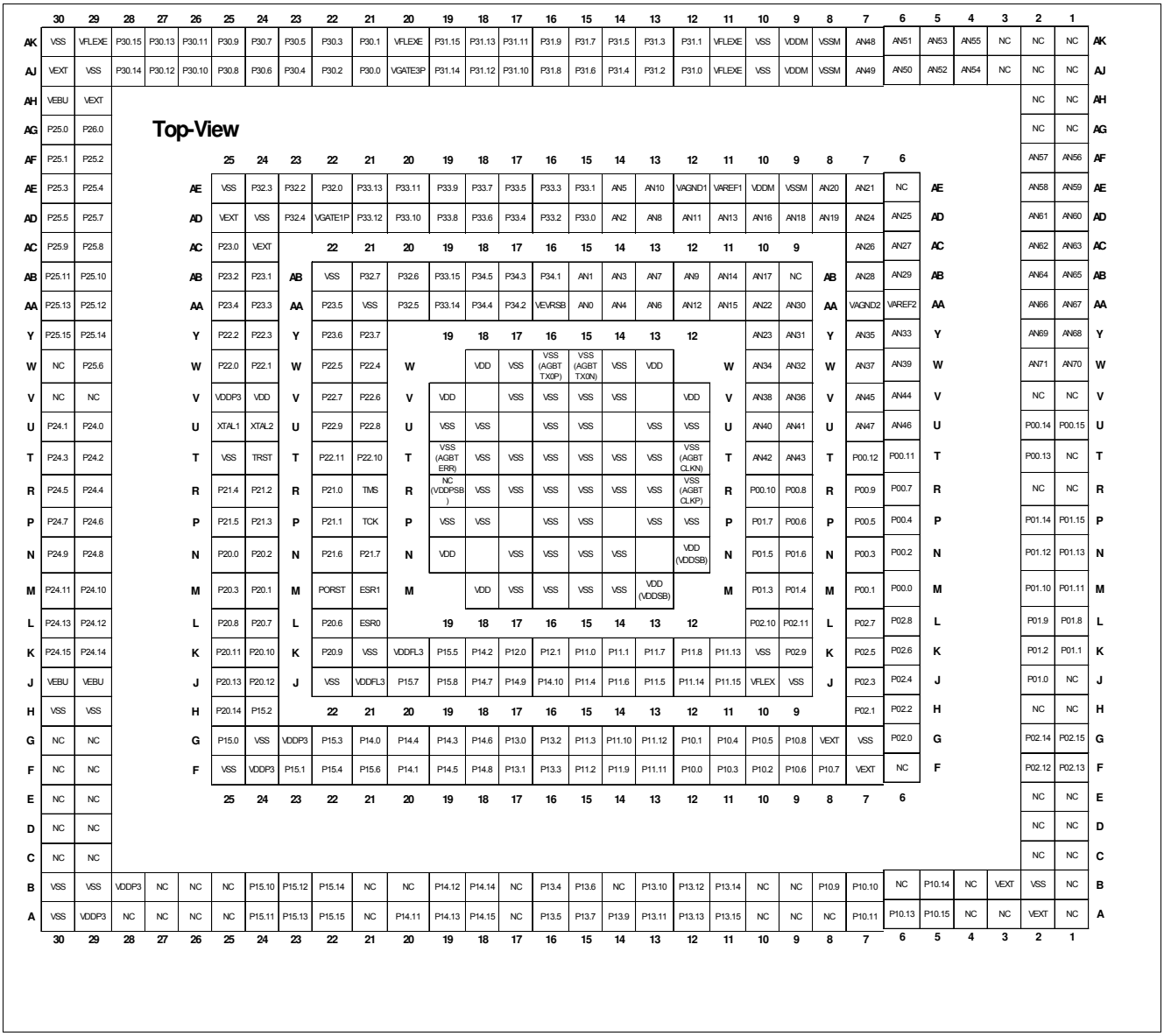

Figure 2-1 TC299x Logic Symbol for the package variant BGA516.

2.1.1 TC299x BGA516 Package Variant Pin Configuration

Table 2-1 Port 00 Functions

Pin	Symbol	Ctrl	Type	Function
M6	P00.0	I	**MP** / **PU1** / **VEXT**	General-purpose input
	TIN9			GTM input
	$\overline{\text{CTRAPA}}$			CCU61 input
	T12HRE			CCU60 input
	INJ00			MSC0 input
	CIFD9			CIF input
	P00.0	O0		General-purpose output
	TOUT9	O1		GTM output
	ASCLK3	O2		ASCLIN3 output
	ATX3	O3		ASCLIN3 output
	–	O4		Reserved
	TXDCAN1	O5		CAN node 1 output
	–	O6		Reserved
	COUT63	O7		CCU60 output
	ETHMDIOA	HWOUT		ETH input/output

Table 2-1 Port 00 Functions (cont'd)

Pin	Symbol	Ctrl	Type	Function
M7	P00.1	I	**LP** / **PU1** / **VEXT**	General-purpose input
	TIN10			GTM input
	ARX3E			ASCLIN3 input
	RXDCAN1D			CAN node 1 input
	PSIRX0A			PSI5 input
	SENT0B			SENT input
	CC60INB			CCU60 input
	CC60INA			CCU61 input
	DSCIN5A			DSADC channel 5 input
	DS5NA			DSADC positive analog input of channel channel 5, pin A
	DSCIN7B			DSADC channel 7 input
	VADCG7.5			VADC analog input channel 5 of group 7
	CIFD10			CIF input
	P00.1	O0		General-purpose output
	TOUT10	O1		GTM output
	ATX3	O2		ASCLIN3 output
	–	O3		Reserved
	DSCOUT5	O4		DSADC channel 5 output
	DSCOUT7	O5		DSADC channel 7 output
	SPC0	O6		SENT output
	CC60	O7		CCU61 output
N6	P00.2	I	**LP** / **PU1** / **VEXT**	General-purpose input
	TIN11			GTM input
	SENT1B			SENT input
	DSDIN5A			DSADC channel 5 input
	DSDIN7B			DSADC channel 7 input
	DS5PA			DSADC negative analog input of channel 5, pin A
	VADCG7.4			VADC analog input channel 4 of group 7
	CIFD11			CIF input
	P00.2	O0		General-purpose output
	TOUT11	O1		GTM output
	ASCLK3	O2		ASCLIN3 output
	TXDCANr1	O3		CAN node 1 output (MultiCANr+)
	PSITX0	O4		PSI5 output
	TXDCAN3	O5		CAN node 3 output
	SLSO34	O6		QSPI3 output
	COUT60	O7		CCU61 output

Table 2-1 Port 00 Functions (cont'd)

Pin	Symbol	Ctrl	Type	Function
N7	P00.3	I	**LP** / **PU1** / **VEXT**	General-purpose input
	TIN12			GTM input
	RXDCAN3A			CAN node 3 input
	RXDCANr1A			CAN node 1 input (MultiCANr+)
	PSIRX1A			PSI5 input
	PSISRXA			PSI5-S input
	SENT2B			SENT input
	CC61INB			CCU60 input
	CC61INA			CCU61 input
	DSCIN3A			DSADC channel 3 input
	VADCG7.3			VADC analog input channel 3 of group 7
	DSITR5F			DSADC channel 5 input
	CIFD12			CIF input
	P00.3	O0		General-purpose output
	TOUT12	O1		GTM output
	ASLSO3	O2		ASCLIN3 output
	–	O3		Reserved
	DSCOUT3	O4		DSADC channel 3 output
	–	O5		Reserved
	SPC2	O6		SENT output
	CC61	O7		CCU61 output
P6	P00.4	I	**LP** / **PU1** / **VEXT**	General-purpose input
	TIN13			GTM input
	REQ7			SCU input
	SENT3B			SENT input
	DSDIN3A			DSADC channel 3 input
	DSSGNA			DSADC channel input
	VADCG7.2			VADC analog input channel 2 of group 7 (MD)
	CIFD13			CIF input
	P00.4	O0		General-purpose output
	TOUT13	O1		GTM output
	PSISTX	O2		PSI5-S output
	–	O3		Reserved
	PSITX1	O4		PSI5 output
	VADCG4BFL0	O5		VADC output
	SPC3	O6		SENT output
	COUT61	O7		CCU61 output

Table 2-1 Port 00 Functions (cont'd)

Pin	Symbol	Ctrl	Type	Function
P7	P00.5	I	**LP** / **PU1** / **VEXT**	General-purpose input
	TIN14			GTM input
	PSIRX2A			PSI5 input
	SENT4B			SENT input
	CC62INB			CCU60 input
	CC62INA			CCU61 input
	DSCIN2A			DSADC channel 2 input
	VADCG7.1			VADC analog input channel 1 of group 7 (MD)
	CIFD14			CIF input
	P00.5	O0		General-purpose output
	TOUT14	O1		GTM output
	DSCGPWMN	O2		DSADC output
	SLSO33	O3		QSPI3 output
	DSCOUT2	O4		DSADC channel 2 output
	VADCG4BFL1	O5		VADC output
	SPC4	O6		SENT output
	CC62	O7		CCU61 output
P9	P00.6	I	**LP** / **PU1** / **VEXT**	General-purpose input
	TIN15			GTM input
	SENT5B			SENT input
	DSDIN2A			DSADC channel 2 input A
	VADCG7.0			VADC analog input channel 0 of group 7 (with pull down diagnostics)
	DSITR4F			DSADC channel 4 input F
	CIFD15			CIF input
	P00.6	O0		General-purpose output
	TOUT15	O1		GTM output
	DSCGPWMP	O2		DSADC output
	VADCG4BFL2	O3		VADC output
	PSITX2	O4		PSI5 output
	VADCEMUX10	O5		VADC output
	SPC5	O6		SENT output
	COUT62	O7		CCU61 output

Table 2-1 Port 00 Functions (cont'd)

Pin	Symbol	Ctrl	Type	Function
R6	P00.7	I	**LP** / **PU1** / **VEXT**	General-purpose input
	TIN16			GTM input
	SENT6B			SENT input
	CC60INC			CCU61 input
	CCPOS0A			CCU61 input
	T12HRB			CCU60 input
	T2INA			GPT120 input
	DSCIN4A			DSADC channel 4 input A
	DS4NA			DSADC negative analog input channel 4, pin A
	VADCG6.5			VADC analog input channel 5 of group 6
	CIFCLK			CIF input
	P00.7	O0		General-purpose output
	TOUT16	O1		GTM output
	–	O2		Reserved
	VADCG4BFL3	O3		VADC output
	DSCOUT4	O4		DSADC channel 4 output
	VADCEMUX11	O5		VADC output
	SPC6	O6		SENT output
	CC60	O7		CCU61 output
R9	P00.8	I	**LP** / **PU1** / **VEXT**	General-purpose input
	TIN17			GTM input
	SENT7B			SENT input
	CC61INC			CCU61 input
	CCPOS1A			CCU61 input
	T13HRB			CCU60 input
	T2EUDA			GPT120 input
	DSDIN4A			DSADC channel 4 input A
	DS4PA			DSADC positive analog input of channel 4, pin A
	VADCG6.4			VADC analog input channel 4 of group 6
	CIFVSNC			CIF input
	P00.8	O0		General-purpose output
	TOUT17	O1		GTM output
	SLSO36	O2		QSPI3 output
	–	O3		Reserved
	–	O4		Reserved
	VADCEMUX12	O5		VADC output
	SPC7	O6		SENT output
	CC61	O7		CCU61 output

Table 2-1 Port 00 Functions (cont'd)

Pin	Symbol	Ctrl	Type	Function
R7	P00.9	I	**LP** / **PU1** / **VEXT**	General-purpose input
	TIN18			GTM input
	SENT8B			SENT input
	CC62INC			CCU61 input
	CCPOS2A			CCU61 input
	T13HRC			CCU60 input
	T12HRC			CCU60 input
	T4EUDA			GPT120 input
	DSCIN1A			DSADC channel 1 input A
	VADCG6.3			VADC analog input channel 3 of group 6
	DSITR3F			DSADC channel 3 input F
	CIFHSNC			CIF input
	P00.9	O0		General-purpose output
	TOUT18	O1		GTM output
	SLSO37	O2		QSPI3 output
	ARTS3	O3		ASCLIN3 output
	DSCOUT1	O4		DSADC channel 1 output
	–	O5		Reserved
	SPC8	O6		SENT output
	CC62	O7		CCU61 output
R10	P00.10	I	**LP** / **PU1** / **VEXT**	General-purpose input
	TIN19			GTM input
	SENT9B			SENT input
	DSDIN1A			DSADC channel 1 input A
	VADCG6.2			VADC analog input channel 2 of group 6 (MD)
	P00.10	O0		General-purpose output
	TOUT19	O1		GTM output
	–	O2		Reserved
	–	O3		Reserved
	–	O4		Reserved
	–	O5		Reserved
	SPC9	O6		SENT output
	COUT63	O7		CCU61 output

Table 2-1 Port 00 Functions (cont'd)

Pin	Symbol	Ctrl	Type	Function
T6	P00.11	I	**LP** / **PU1** / **VEXT**	General-purpose input
	TIN20			GTM input
	CTRAPA			CCU60 input
	T12HRE			CCU61 input
	DSCIN0A			DSADC channel 0 input A
	VADCG6.1			VADC analog input channel 1 of group 6 (MD)
	P00.11	O0		General-purpose output
	TOUT20	O1		GTM output
	–	O2		Reserved
	–	O3		Reserved
	DSCOUT0	O4		DSADC channel 0 output
	–	O5		Reserved
	–	O6		Reserved
	–	O7		Reserved
T7	P00.12	I	**LP** / **PU1** / **VEXT**	General-purpose input
	TIN21			GTM input
	ACTS3A			ASCLIN3 input
	DSDIN0A			DSADC channel 0 input A
	VADCG6.0			VADC analog input channel 0 of group 6
	P00.12	O0		General-purpose output
	TOUT21	O1		GTM output
	–	O2		Reserved
	–	O3		Reserved
	–	O4		Reserved
	–	O5		Reserved
	–	O6		Reserved
	COUT63	O7		CCU61 output
T2	P00.13	I	**MP+** / **PU1** / **VEXT**	General-purpose input
	TIN167			GTM input
	DSDIN6A			DSADC channel 6 input A
	P00.13	O0		General-purpose output
	TOUT167	O1		GTM output
	–	O2		Reserved
	–	O3		Reserved
	EXTCLK1	O4		SCU output
	–	O5		Reserved
	–	O6		Reserved
	–	O7		Reserved

Table 2-1 Port 00 Functions (cont'd)

Pin	Symbol	Ctrl	Type	Function
U2	P00.14	I	**LP** / **PU1** / **VEXT**	General-purpose input
	TIN166			GTM input
	DSCIN6A			DSADC channel 6 input A
	P00.14	O0		General-purpose output
	TOUT166	O1		GTM output
	–	O2		Reserved
	–	O3		Reserved
	DSCOUT6	O4		DSADC channel 6 output
	–	O5		Reserved
	–	O6		Reserved
	–	O7		Reserved
U1	P00.15	I	**MP+** / **PU1** / **VEXT**	General-purpose input
	TIN168			GTM input
	DSITR6F			DSADC channel 6 input F
	P00.15	O0		General-purpose output
	TOUT168	O1		GTM output
	–	O2		Reserved
	–	O3		Reserved
	EXTCLK0	O4		SCU output
	–	O5		Reserved
	–	O6		Reserved
	–	O7		Reserved

Table 2-2 Port 01 Functions

Pin	Symbol	Ctrl	Type	Function
J2	P01.0	I	**LP** / **PU1** / **VEXT**	General-purpose input
	TIN155			GTM input
	DSITR6E			DSADC channel 6 input E
	RXDCAN3F			CAN node 3 input
	RXDCANr1E			CAN node 1 input (MultiCANr+)
	P01.0	O0		General-purpose output
	TOUT155	O1		GTM output
	–	O2		Reserved
	–	O3		Reserved
	–	O4		Reserved
	–	O5		Reserved
	–	O6		Reserved
	–	O7		Reserved

Table 2-2 Port 01 Functions (cont'd)

Pin	Symbol	Ctrl	Type	Function
K1	P01.1	I	**LP** / **PU1** / **VEXT**	General-purpose input
	TIN159			GTM input
	DSITR8E			DSADC channel 8 input E
	RXD1A1			ERAY1 input
	SENT10B			SENT input
	P01.1	O0		General-purpose output
	TOUT159	O1		GTM output
	–	O2		Reserved
	–	O3		Reserved
	–	O4		Reserved
	–	O5		Reserved
	–	O6		Reserved
	–	O7		Reserved
K2	P01.2	I	**LP** / **PU1** / **VEXT**	General-purpose input
	TIN156			GTM input
	DSCIN7A			DSADC channel 7 input A
	P01.2	O0		General-purpose output
	TOUT156	O1		GTM output
	–	O2		Reserved
	TXDCAN3	O3		CAN node 3 output
	–	O4		Reserved
	TXDCANr1	O5		CAN node 1 output (MultiCANr+)
	DSCOUT7	O6		DSADC channel 7 output
	–	O7		Reserved
M10	P01.3	I	**LP** / **PU1** / **VEXT**	General-purpose input
	TIN111			GTM input
	$\overline{\text{SLSI3B}}$			QSPI3 input
	DSITR7F			DSADC channel 7 input F
	P01.3	O0		General-purpose output
	TOUT111	O1		GTM output
	–	O2		Reserved
	–	O3		Reserved
	SLSO39	O4		QSPI3 output
	TXDCAN1	O5		CAN node 1 output
	–	O6		Reserved
	–	O7		Reserved

Table 2-2 Port 01 Functions (cont'd)

Pin	Symbol	Ctrl	Type	Function
M9	P01.4	I	**LP** / **PU1** / **VEXT**	General-purpose input
	TIN112			GTM input
	RXDCAN1C			CAN node 1 input
	DSITR7E			DSADC channel 7 input E
	P01.4	O0		General-purpose output
	TOUT112	O1		GTM output
	–	O2		Reserved
	–	O3		Reserved
	SLSO310	O4		QSPI3 output
	–	O5		Reserved
	–	O6		Reserved
	–	O7		Reserved
N10	P01.5	I	**LP** / **PU1** / **VEXT**	General-purpose input
	TIN113			GTM input
	MRST3C			QSPI3 input
	DSCIN8A			DSADC channel 8 input A
	P01.5	O0		General-purpose output
	TOUT113	O1		GTM output
	–	O2		Reserved
	–	O3		Reserved
	MRST3	O4		QSPI3 output
	–	O5		Reserved
	DSCOUT8	O6		DSADC channel 8 output
	–	O7		Reserved
N9	P01.6	I	**MP** / **PU1** / **VEXT**	General-purpose input
	TIN114			GTM input
	MTSR3C			QSPI3 input
	DSDIN8A			DSADC channel 8 input A
	P01.6	O0		General-purpose output
	TOUT114	O1		GTM output
	–	O2		Reserved
	–	O3		Reserved
	MTSR3	O4		QSPI3 output
	–	O5		Reserved
	–	O6		Reserved
	–	O7		Reserved

Table 2-2 Port 01 Functions (cont'd)

Pin	Symbol	Ctrl	Type	Function
P10	P01.7	I	**MP** / **PU1** / **VEXT**	General-purpose input
	TIN115			GTM input
	SCLK3C			QSPI3 input
	DSITR8F			DSADC channel 8 input F
	P01.7	O0		General-purpose output
	TOUT115	O1		GTM output
	–	O2		Reserved
	–	O3		Reserved
	SCLK3	O4		QSPI3 output
	–	O5		Reserved
	–	O6		Reserved
	–	O7		Reserved
L1	P01.8	I	**LP** / **PU1** / **VEXT**	General-purpose input
	TIN162			GTM input
	DSDIN9A			DSADC channel 9 input A
	SENT12B			SENT input
	ARX0C			ASCLIN0 input
	RXDCAN0F			CAN node 0 input
	RXDCANr0E			CAN node 0 input (MultiCANr+)
	RXD1B1			ERAY1 input
	P01.8	O0		General-purpose output
	TOUT162	O1		GTM output
	–	O2		Reserved
	–	O3		Reserved
	–	O4		Reserved
	–	O5		Reserved
	–	O6		Reserved
	–	O7		Reserved

Table 2-2 Port 01 Functions (cont'd)

Pin	Symbol	Ctrl	Type	Function
L2	P01.9	I	**LP** / **PU1** / **VEXT**	General-purpose input
	TIN160			GTM input
	DSCIN9A			DSADC channel 9 input A
	SENT11B			SENT input
	P01.9	O0		General-purpose output
	TOUT160	O1		GTM output
	–	O2		Reserved
	–	O3		Reserved
	–	O4		Reserved
	–	O5		Reserved
	DSCOUT9	O6		DSADC channel 9 output
	–	O7		Reserved
M2	P01.10	I	**LP** / **PU1** / **VEXT**	General-purpose input
	TIN163			GTM input
	DSITR9F			DSADC channel 9 input F
	SENT13B			SENT input
	P01.10	O0		General-purpose output
	TOUT163	O1		GTM output
	–	O2		Reserved
	–	O3		Reserved
	–	O4		Reserved
	–	O5		Reserved
	–	O6		Reserved
	–	O7		Reserved
M1	P01.11	I	**LP** / **PU1** / **VEXT**	General-purpose input
	TIN165			GTM input
	DSITR9E			DSADC channel 9 input E
	SENT14B			SENT input
	P01.11	O0		General-purpose output
	TOUT165	O1		GTM output
	–	O2		Reserved
	–	O3		Reserved
	–	O4		Reserved
	–	O5		Reserved
	–	O6		Reserved
	–	O7		Reserved

Table 2-2 Port 01 Functions (cont'd)

Pin	Symbol	Ctrl	Type	Function
N2	P01.12	I	**MP+** / **PU1** / **VEXT**	General-purpose input
	TIN158			GTM input
	P01.12	O0		General-purpose output
	TOUT158	O1		GTM output
	–	O2		Reserved
	–	O3		Reserved
	–	O4		Reserved
	–	O5		Reserved
	TXD1A	O6		ERAY1 output
	–	O7		Reserved
N1	P01.13	I	**MP+** / **PU1** / **VEXT**	General-purpose input
	TIN161			GTM input
	P01.13	O0		General-purpose output
	TOUT161	O1		GTM output
	ATX0	O2		ASCLIN0 output
	–	O3		Reserved
	TXDCAN0	O4		CAN node 0 output
	TXDCANr0	O5		CAN node 0 output (MultiCANr+)
	TXD1B	O6		ERAY1 output
	–	O7		Reserved
P2	P01.14	I	**MP+** / **PU1** / **VEXT**	General-purpose input
	TIN164			GTM input
	P01.14	O0		General-purpose output
	TOUT164	O1		GTM output
	–	O2		Reserved
	–	O3		Reserved
	–	O4		Reserved
	–	O5		Reserved
	TXEN1A	O6		ERAY1 output
	–	O7		Reserved