Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

MOS DIGITAL INTEGRATED CIRCUIT SILICON GATE CMOS

1 GBIT (128M × 8 BIT) CMOS NAND E^{2}PROM

DESCRIPTION

The TC58BYG0S3HBAI4 is a single 1.8V 1Gbit (1,107,296,256 bits) NAND Electrically Erasable and Programmable Read-Only Memory (NAND E^{2}PROM) organized as (2048 + 64) bytes × 64 pages × 1024 blocks. The device has a 2112-byte static register which allows program and read data to be transferred between the register and the memory cell array in 2112-bytes increments. The Erase operation is implemented in a single block unit (128 Kbytes + 4 Kbytes: 2112 bytes × 64 pages).

The TC58BYG0S3HBAI4 is a serial-type memory device which utilizes the I/O pins for both address and data input/output as well as for command inputs. The Erase and Program operations are automatically executed making the device most suitable for applications such as solid-state file storage, voice recording, image file memory for still cameras and other systems which require high-density non-volatile memory data storage.

The TC58BYG0S3HBAI4 has ECC logic on the chip and 8bit read errors for each 528Bytes can be corrected internally.

FEATURES

- Organization x8
  - Memory cell array 2112 × 64K × 8
  - Register 2112 × 8
  - Page size 2112 bytes
  - Block size (128K + 4K) bytes
- Modes
  - Read, Reset, Auto Page Program, Auto Block Erase, Status Read, Page Copy, ECC Status Read
- Mode control
  - Serial input/output
  - Command control
- Number of valid blocks
  - Min 1004 blocks
  - Max 1024 blocks
- Power supply
  - V_{CC} = 1.7V to 1.95V
- Access time
  - Cell array to register 40 μs typ.
  - Read Cycle Time 25 ns min (C_L=30pF)
- Program/Erase time
  - Auto Page Program 330 μs/page typ.
  - Auto Block Erase 3.5 ms/block typ.
- Operating current
  - Read (25 ns cycle) 30 mA max
  - Program (avg.) 30 mA max
  - Erase (avg.) 30 mA max
  - Standby 50 μA max
- Package
  - P-TFBGA63-0911-0.80CZ (Weight: 0.15 g typ.)
- 8bit ECC for each 528Bytes is implemented on a chip.

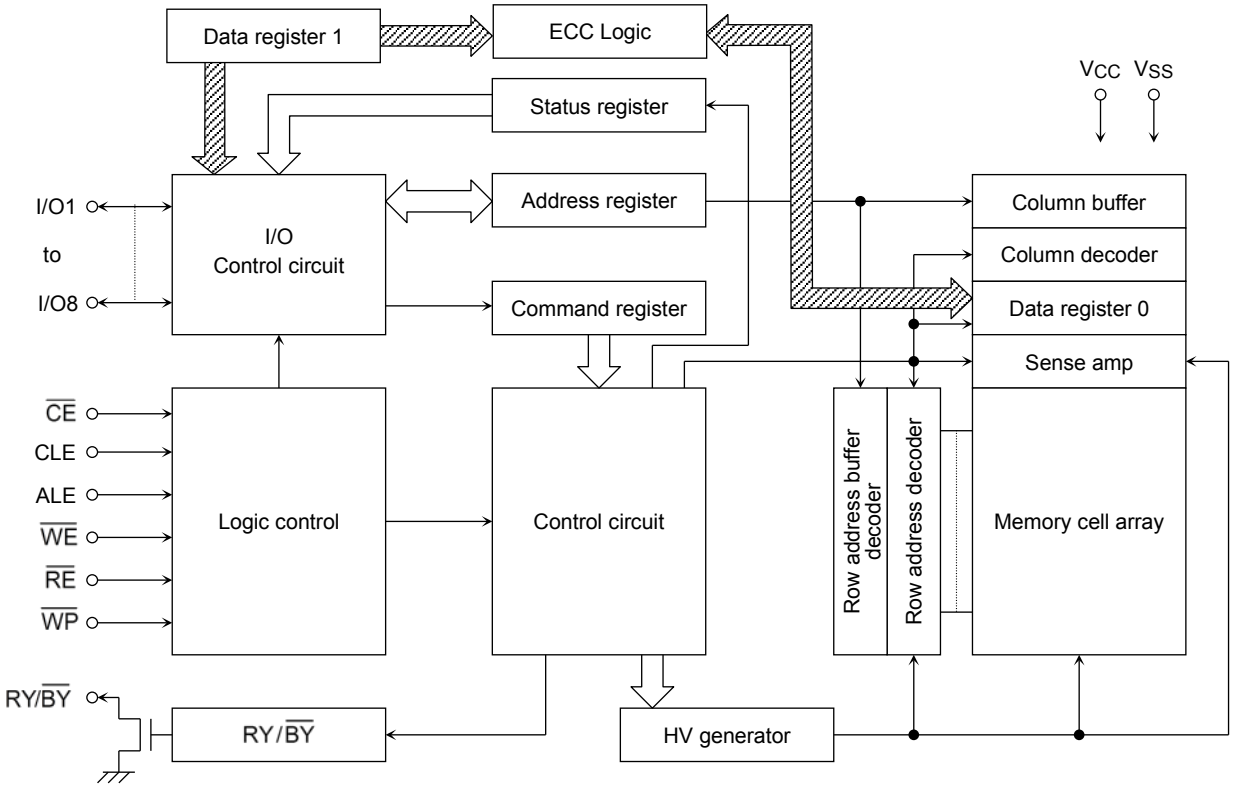
PIN ASSIGNMENT (TOP VIEW)

	1	2	3	4	5	6	7	8	9	10
A	NC	NC							NC	NC
B	NC								NC	NC
C			$\overline{WP}$	ALE	V_{SS}	$\overline{CE}$	$\overline{WE}$	RY/$\overline{BY}$		
D			NC	$\overline{RE}$	CLE	NC	NC	NC		
E			NC	NC	NC	NC	NC	NC		
F			NC	NC	NC	NC	NC	NC		
G			NC	NC	NC	NC	NC	NC		
H			NC	I/O1	NC	NC	NC	V_{CC}		
J			NC	I/O2	NC	V_{CC}	I/O6	I/O8		
K			V_{SS}	I/O3	I/O4	I/O5	I/O7	V_{SS}		
L	NC	NC							NC	NC
M	NC	NC							NC	NC

PIN NAMES

I/O1 to I/O8	I/O port
$\overline{CE}$	Chip enable
$\overline{WE}$	Write enable
$\overline{RE}$	Read enable
CLE	Command latch enable
ALE	Address latch enable
$\overline{WP}$	Write protect
RY/$\overline{BY}$	Ready/Busy
V_{CC}	Power supply
V_{SS}	Ground
NC	No Connection

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

SYMBOL	RATING	VALUE	UNIT
V_{CC}	Power Supply Voltage	−0.6 to 2.5	V
V_{IN}	Input Voltage	−0.6 to 2.5	V
$V_{I/O}$	Input /Output Voltage	−0.6 to V_{CC} + 0.3 (≤ 2.5 V)	V
P_D	Power Dissipation	0.3	W
T_{SOLDER}	Soldering Temperature (10 s)	260	°C
T_{STG}	Storage Temperature	−55 to 125	°C
T_{OPR}	Operating Temperature	-40 to 85	°C

CAPACITANCE *(Ta = 25°C, f = 1 MHz)

SYMBOL	PARAMETER	CONDITION	MIN	MAX	UNIT
C_{IN}	Input	V_{IN} = 0 V	—	10	pF
C_{OUT}	Output	V_{OUT} = 0 V	—	10	pF

* This parameter is periodically sampled and is not tested for every device.

VALID BLOCKS

SYMBOL	PARAMETER	MIN	TYP.	MAX	UNIT
N_{VB}	Number of Valid Blocks	1004	—	1024	Blocks

NOTE: The device occasionally contains unusable blocks. Refer to Application Note (13) toward the end of this document.
The first block (Block 0) is guaranteed to be a valid block at the time of shipment.
The specification for the minimum number of valid blocks is applicable over lifetime.

RECOMMENDED DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN	TYP.	MAX	UNIT
V_{CC}	Power Supply Voltage	1.7	—	1.95	V
V_{IH}	High Level Input Voltage	V_{CC} x 0.8	—	V_{CC} + 0.3	V
V_{IL}	Low Level Input Voltage	–0.3*	—	V_{CC} x 0.2	V

* –2 V (pulse width lower than 20 ns)

DC CHARACTERISTICS (Ta = -40 to 85°C, V_{CC} = 1.7 to 1.95V)

SYMBOL	PARAMETER	CONDITION	MIN	TYP.	MAX	UNIT
I_{IL}	Input Leakage Current	V_{IN} = 0 V to V_{CC}	—	—	±10	μA
I_{LO}	Output Leakage Current	V_{OUT} = 0 V to V_{CC}	—	—	±10	μA
I_{CCO1}	Serial Read Current	$\overline{CE}$ = V_{IL}, I_{OUT} = 0 mA, t_{RC} = 25 ns	—	—	30	mA
I_{CCO2}	Programming Current	—	—	—	30	mA
I_{CCO3}	Erasing Current	—	—	—	30	mA
I_{CCS}	Standby Current	$\overline{CE}$ = V_{CC} – 0.2 V, $\overline{WP}$ = 0 V/V_{CC}	—	—	50	μA
V_{OH}	High Level Output Voltage	I_{OH} = –0.1 mA	V_{CC} – 0.2	—	—	V
V_{OL}	Low Level Output Voltage	I_{OL} = 0.1 mA	—	—	0.2	V
I_{OL} (RY/$\overline{BY}$)	Output Current of RY/$\overline{BY}$ pin	V_{OL} = 0.2 V	—	4	—	mA

AC CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

(Ta = -40 to 85°C, V_{CC} = 1.7 to 1.95V)

SYMBOL	PARAMETER	MIN	MAX	UNIT
t_{CLS}	CLE Setup Time	12	—	ns
t_{CLH}	CLE Hold Time	5	—	ns
t_{CS}	$\overline{CE}$ Setup Time	20	—	ns
t_{CH}	$\overline{CE}$ Hold Time	5	—	ns
t_{WP}	Write Pulse Width	12	—	ns
t_{ALS}	ALE Setup Time	12	—	ns
t_{ALH}	ALE Hold Time	5	—	ns
t_{DS}	Data Setup Time	12	—	ns
t_{DH}	Data Hold Time	5	—	ns
t_{WC}	Write Cycle Time	25	—	ns
t_{WH}	$\overline{WE}$ High Hold Time	10	—	ns
t_{WW}	$\overline{WP}$ High to $\overline{WE}$ Low	100	—	ns
t_{RR}	Ready to $\overline{RE}$ Falling Edge	20	—	ns
t_{RW}	Ready to $\overline{WE}$ Falling Edge	20	—	ns
t_{RP}	Read Pulse Width	12	—	ns
t_{RC}	Read Cycle Time	25	—	ns
t_{REA}	$\overline{RE}$ Access Time	—	20	ns
t_{CEA}	$\overline{CE}$ Access Time	—	25	ns
t_{CLR}	CLE Low to $\overline{RE}$ Low	10	—	ns
t_{AR}	ALE Low to $\overline{RE}$ Low	10	—	ns
t_{RHOH}	$\overline{RE}$ High to Output Hold Time	25	—	ns
t_{RLOH}	$\overline{RE}$ Low to Output Hold Time	5	—	ns
t_{RHZ}	$\overline{RE}$ High to Output High Impedance	—	60	ns
t_{CHZ}	$\overline{CE}$ High to Output High Impedance	—	20	ns
t_{CSD}	$\overline{CE}$ High to ALE or CLE Don't Care	0	—	ns
t_{REH}	$\overline{RE}$ High Hold Time	10	—	ns
t_{IR}	Output-High-Impedance-to-$\overline{RE}$ Falling Edge	0	—	ns
t_{RHW}	$\overline{RE}$ High to $\overline{WE}$ Low	30	—	ns
t_{WHC}	$\overline{WE}$ High to $\overline{CE}$ Low	30	—	ns
t_{WHR}	$\overline{WE}$ High to $\overline{RE}$ Low	60	—	ns
t_{WB}	$\overline{WE}$ High to Busy	—	100	ns
t_{RST}	Device Reset Time (Ready/Read/Program/Erase)	—	5/5/10/500	μs

*1: tCLS and tALS can not be shorter than tWP.

*2: tCS should be longer than tWP + 8ns.

AC TEST CONDITIONS

PARAMETER	CONDITION
	V_{CC}: 1.7 to 1.95
Input level	V_{CC}-0.2V, 0.2V
Input pulse rise and fall time	3 ns
Input comparison level	V_{CC} / 2
Output data comparison level	V_{CC} / 2
Output load	C_L (30 pF) + 1 TTL

Note: Busy to ready time depends on the pull-up resistor tied to the RY/$\overline{BY}$ pin.
(Refer to Application Note (9) toward the end of this document)

PROGRAMMING / ERASING / READING CHARACTERISTICS
(Ta = -40 to 85°C, V_{CC} = 1.7 to 1.95V)

SYMBOL	PARAMETER	MIN	TYP.	MAX	UNIT	NOTES
t_{PROG}	Average Programming Time	—	330	700	μs	
N	Number of Partial Program Cycles in the Same Page	—	—	4		(1)
t_{BERASE}	Block Erasing Time	—	3.5	10	ms	
t_R	Memory Cell Array to Starting Address	—	40	120	μs	

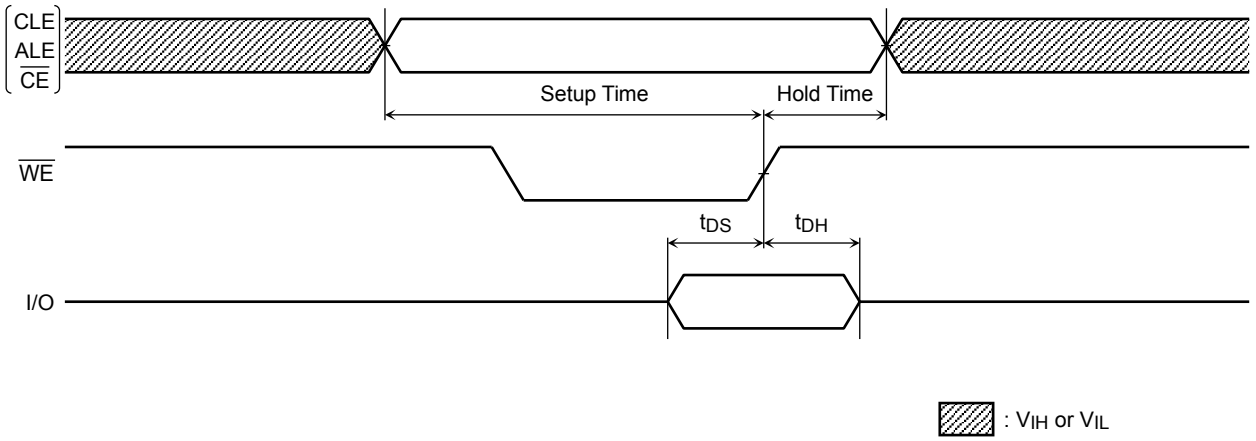
(1) Refer to Application Note (12) toward the end of this document.

Data Output

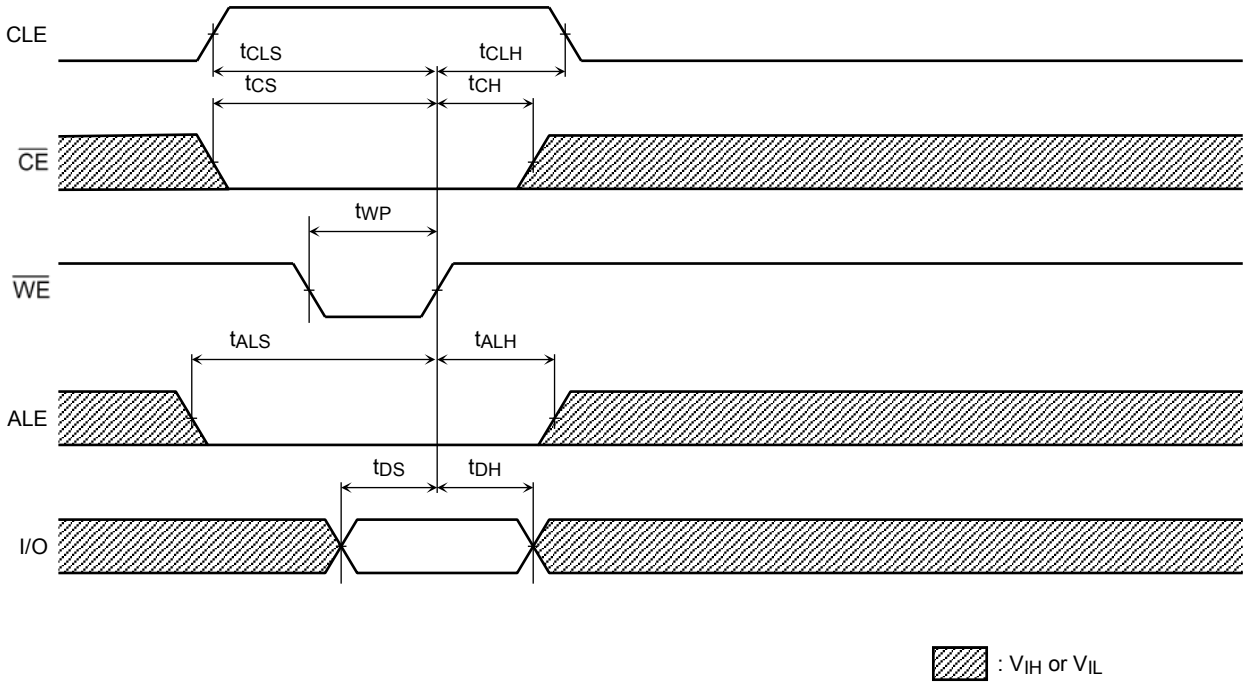
When tREH is long, output buffers are disabled by /RE=High, and the hold time of data output depend on tRHOH (25ns MIN). On this condition, waveforms look like normal serial read mode.
When tREH is short, output buffers are not disabled by /RE=High, and the hold time of data output depend on tRLOH (5ns MIN). On this condition, output buffers are disabled by the rising edge of CLE, ALE, /CE or falling edge of /WE, and waveforms look like Extended Data Output Mode.

TIMING DIAGRAMS

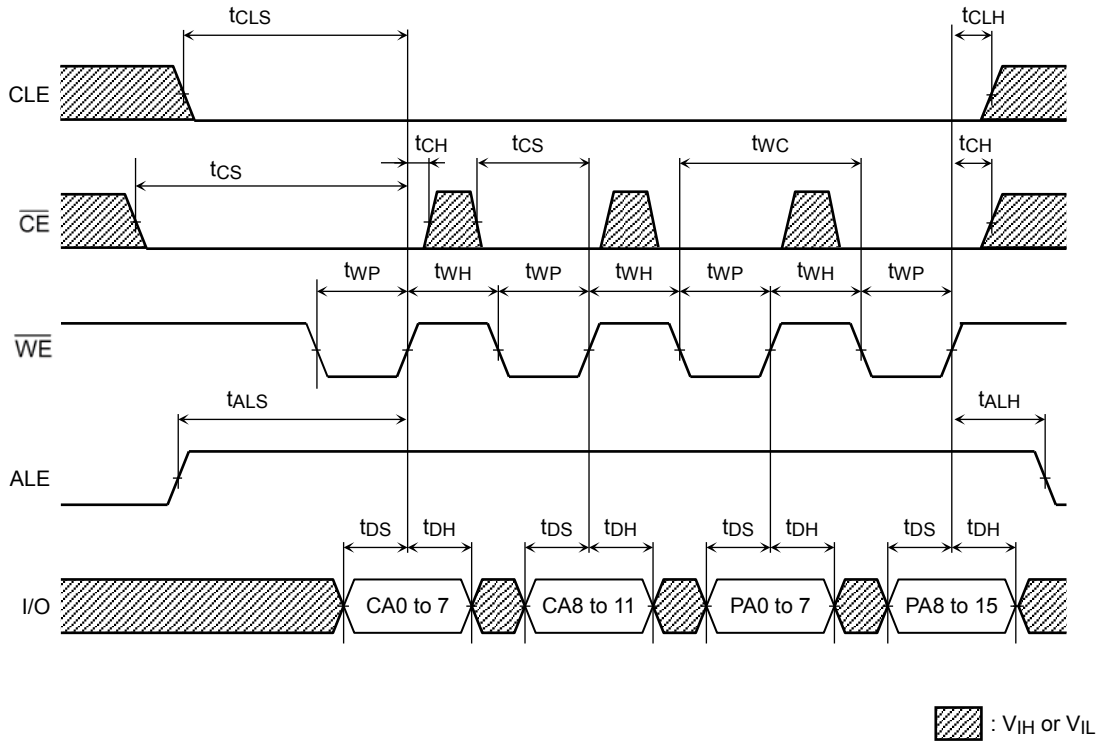
Latch Timing Diagram for Command/Address/Data



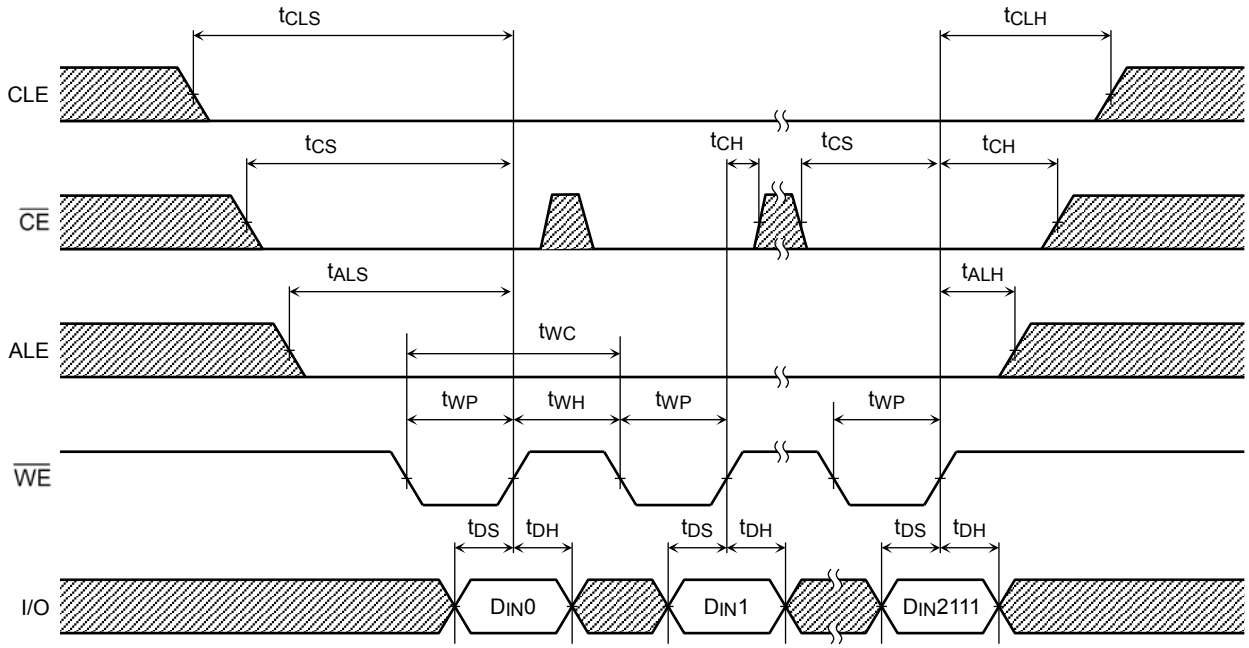
Command Input Cycle Timing Diagram



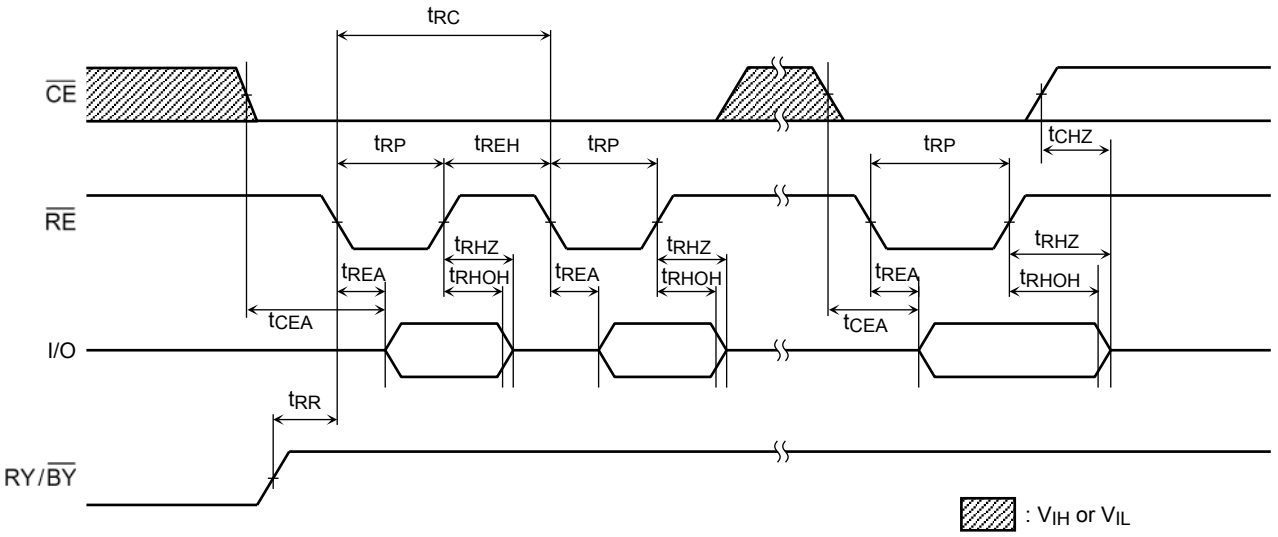
Address Input Cycle Timing Diagram



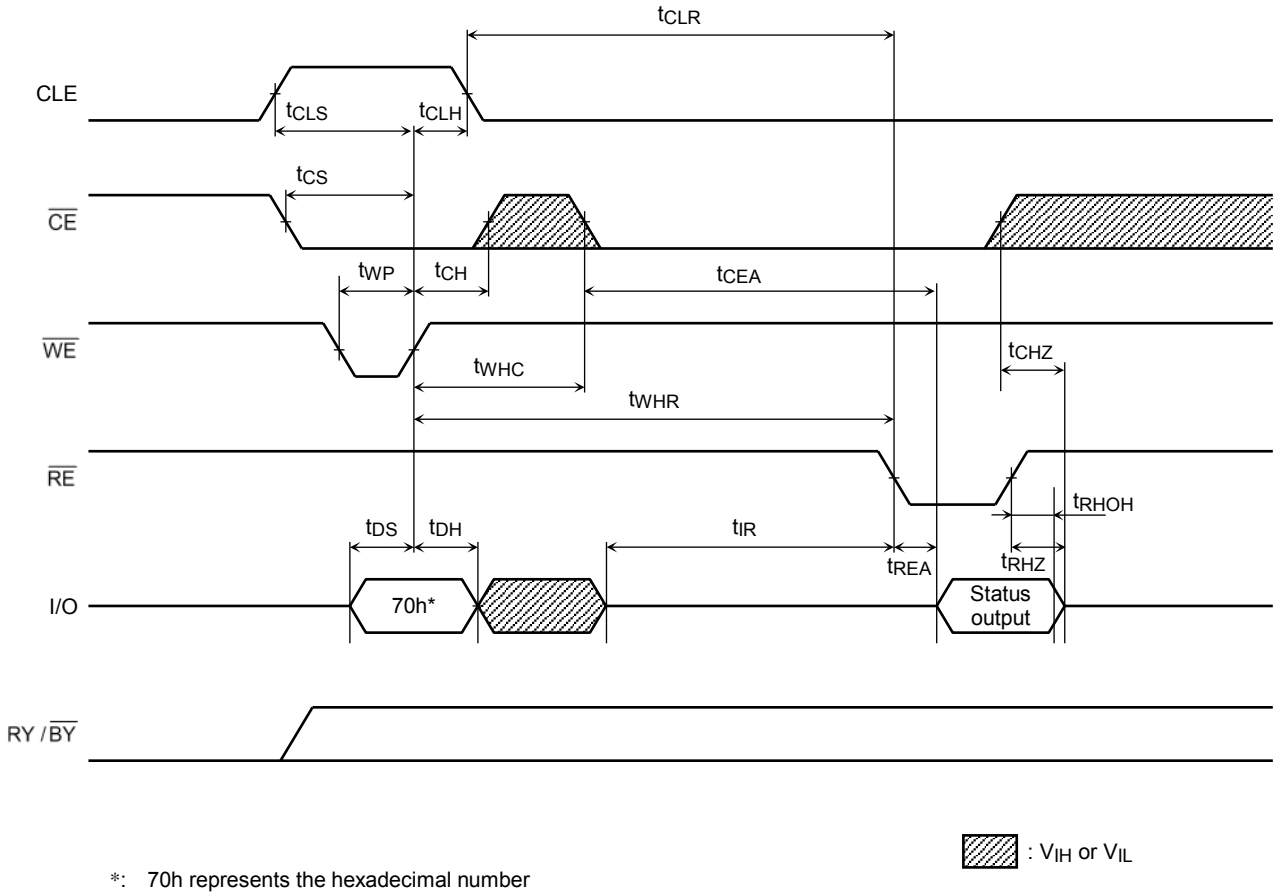
Data Input Cycle Timing Diagram



Serial Read Cycle Timing Diagram

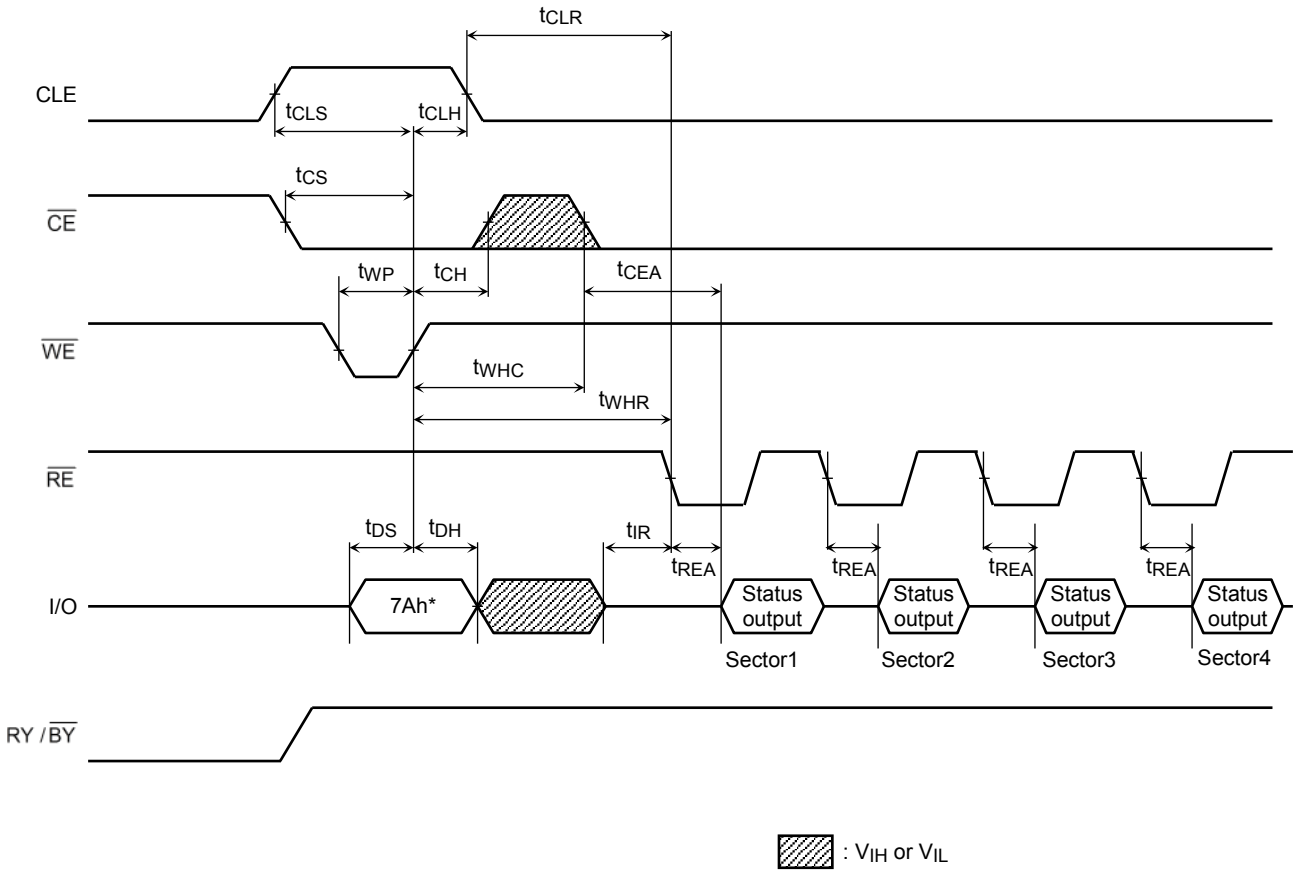


Status Read Cycle Timing Diagram



*: 70h represents the hexadecimal number

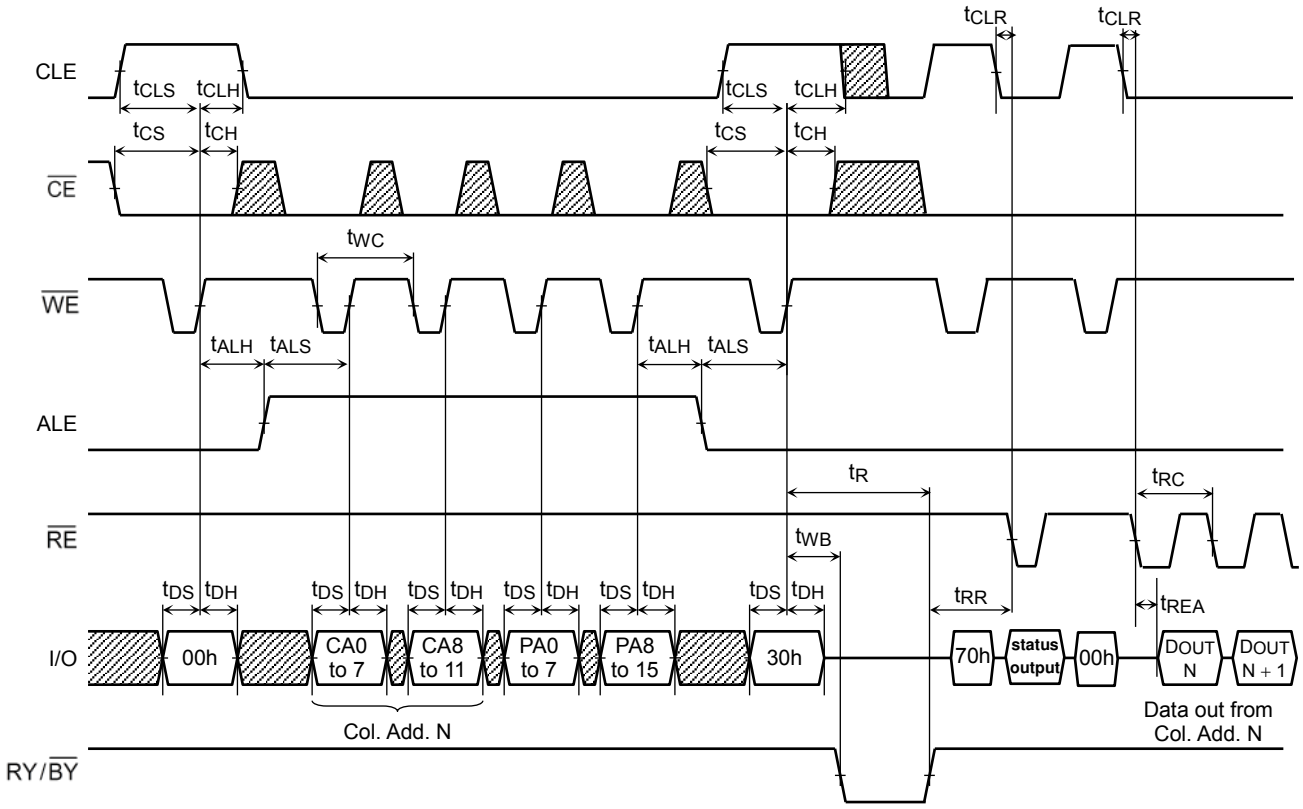
ECC Status Read Cycle Timing Diagram



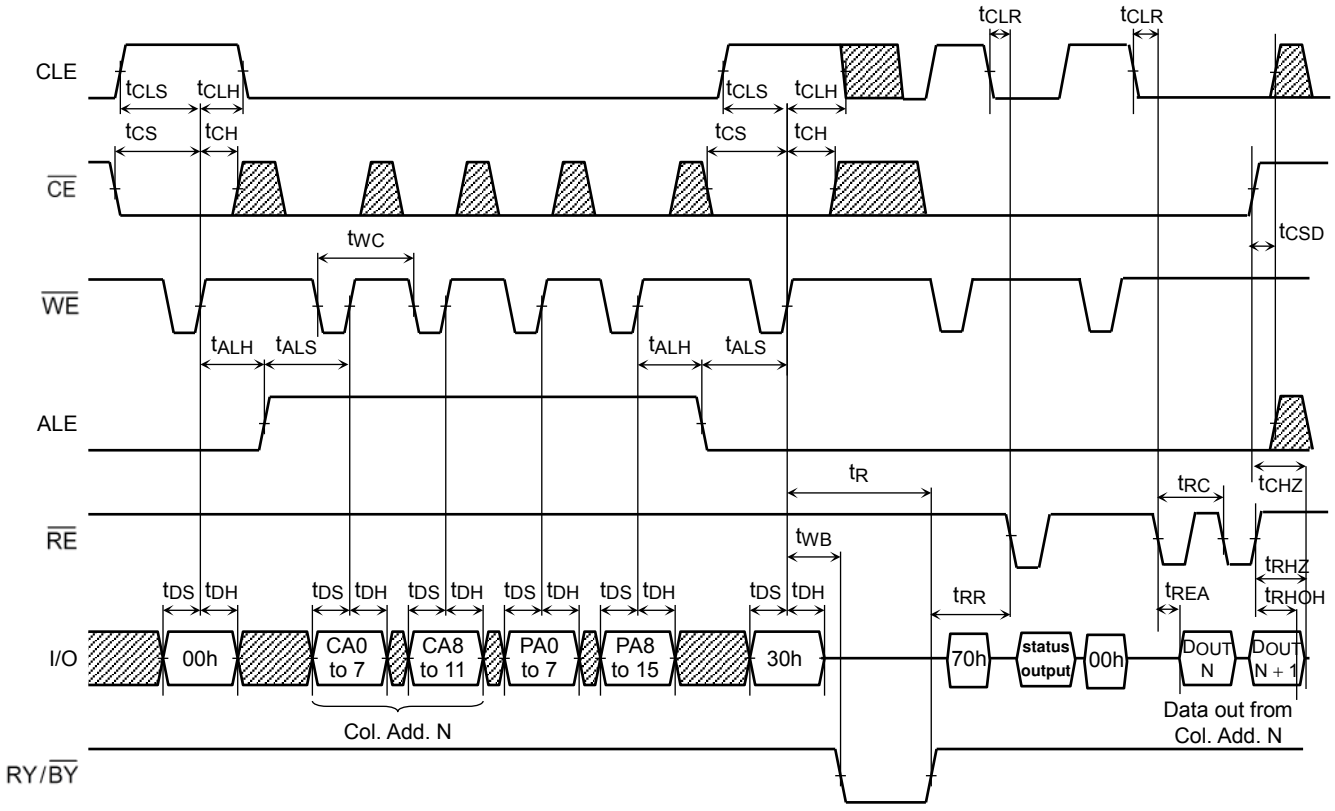
* :ECC Status output should be read for all 4 sector information.

** :7Ah command can be input to the device from [after RY/$\overline{BY}$ returns to High] to [before Dout or Next command input].

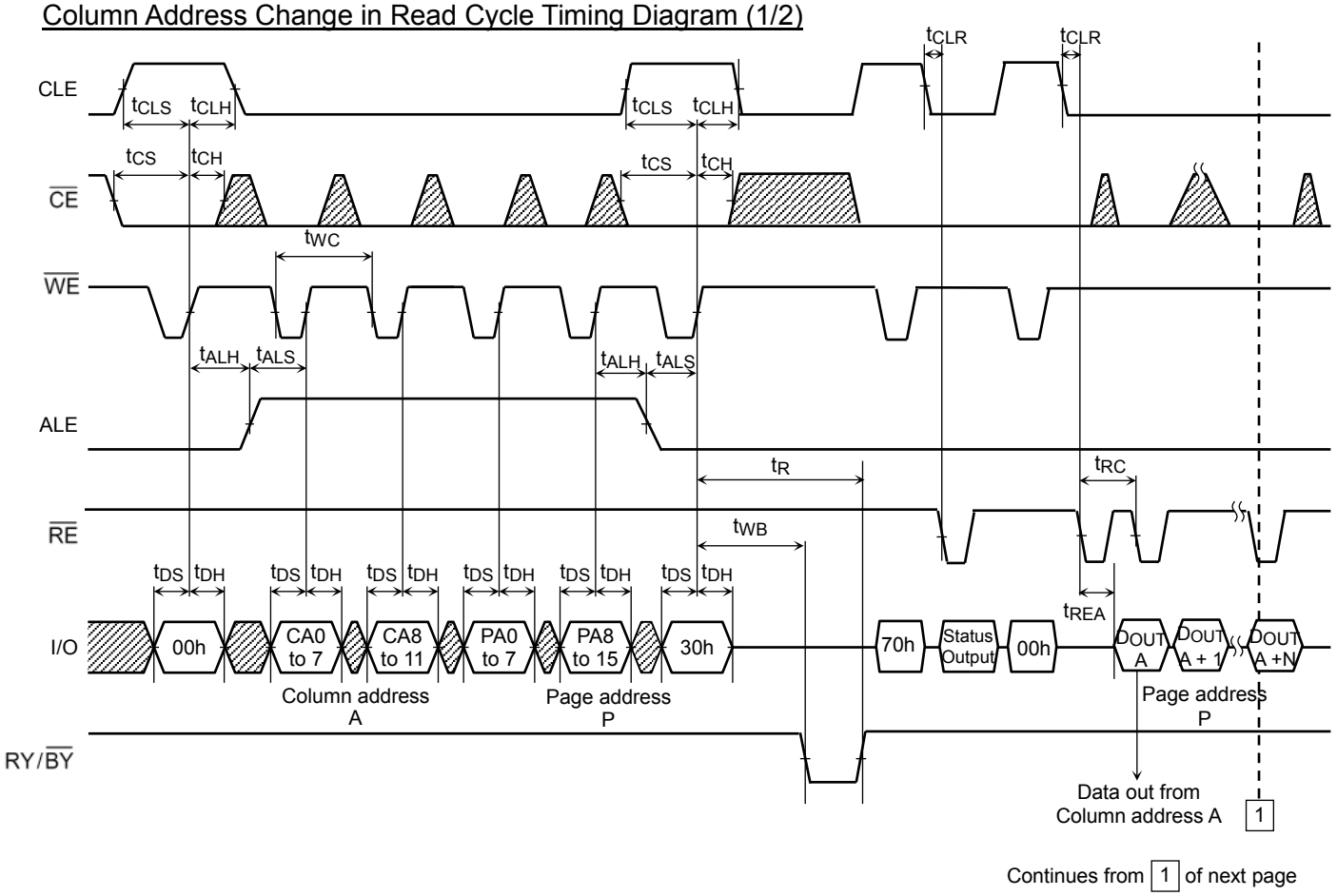
Read Cycle Timing Diagram



Read Cycle Timing Diagram: When Interrupted by $\overline{CE}$

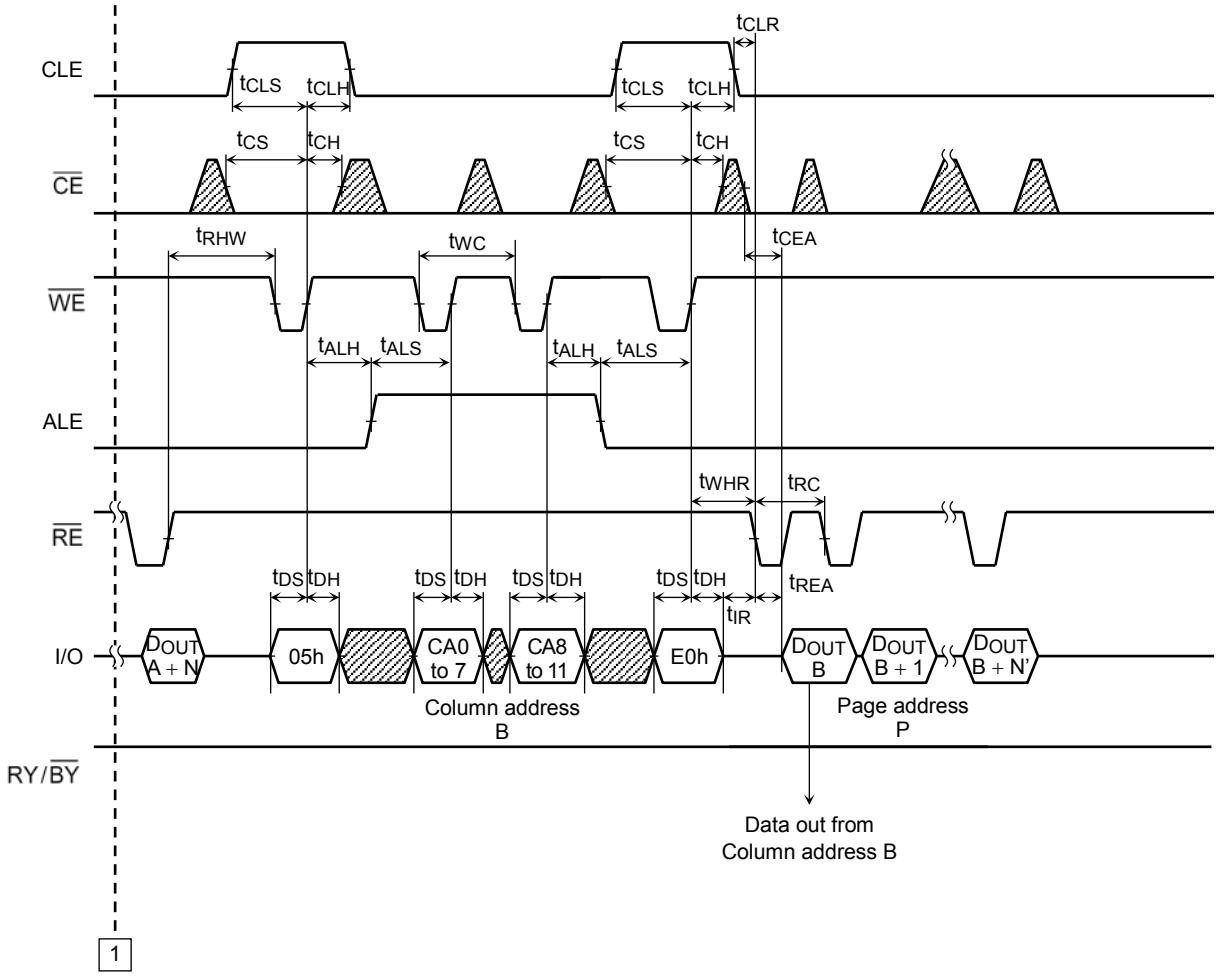


Column Address Change in Read Cycle Timing Diagram (1/2)



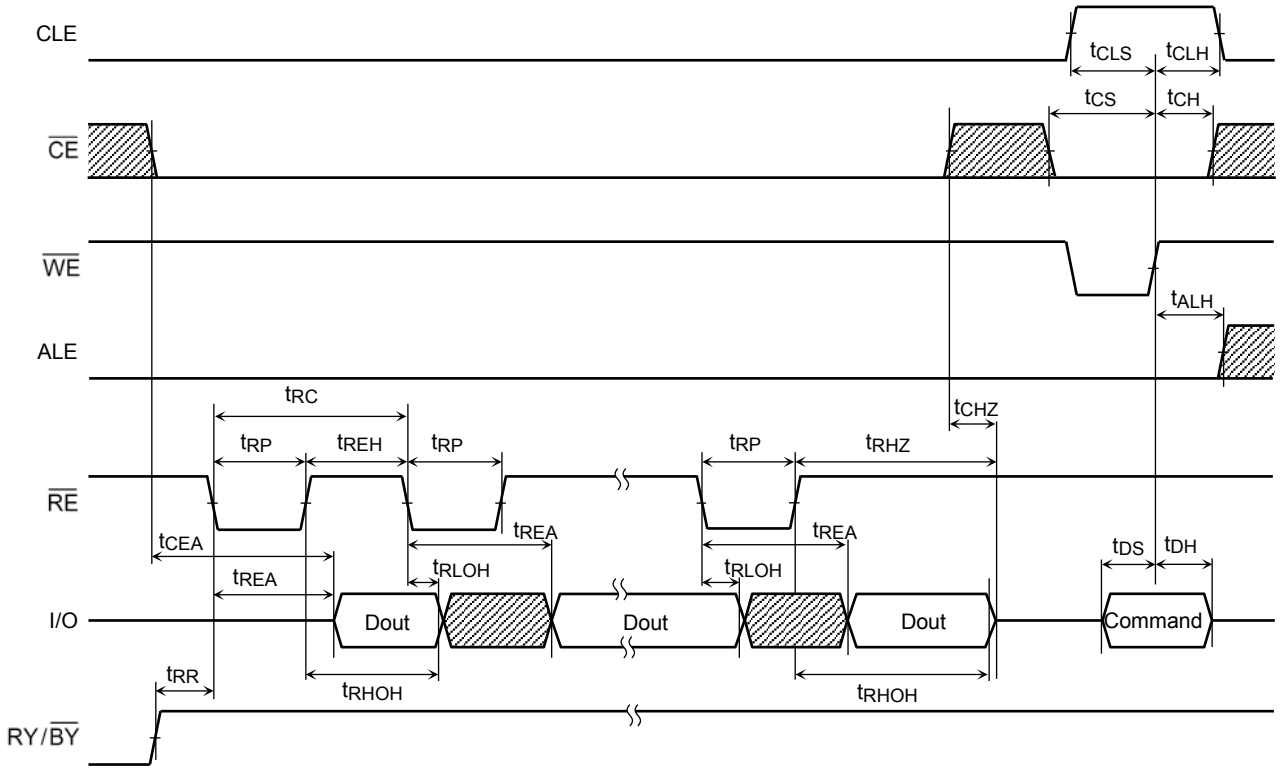
Continues from 1 of next page

Column Address Change in Read Cycle Timing Diagram (2/2)

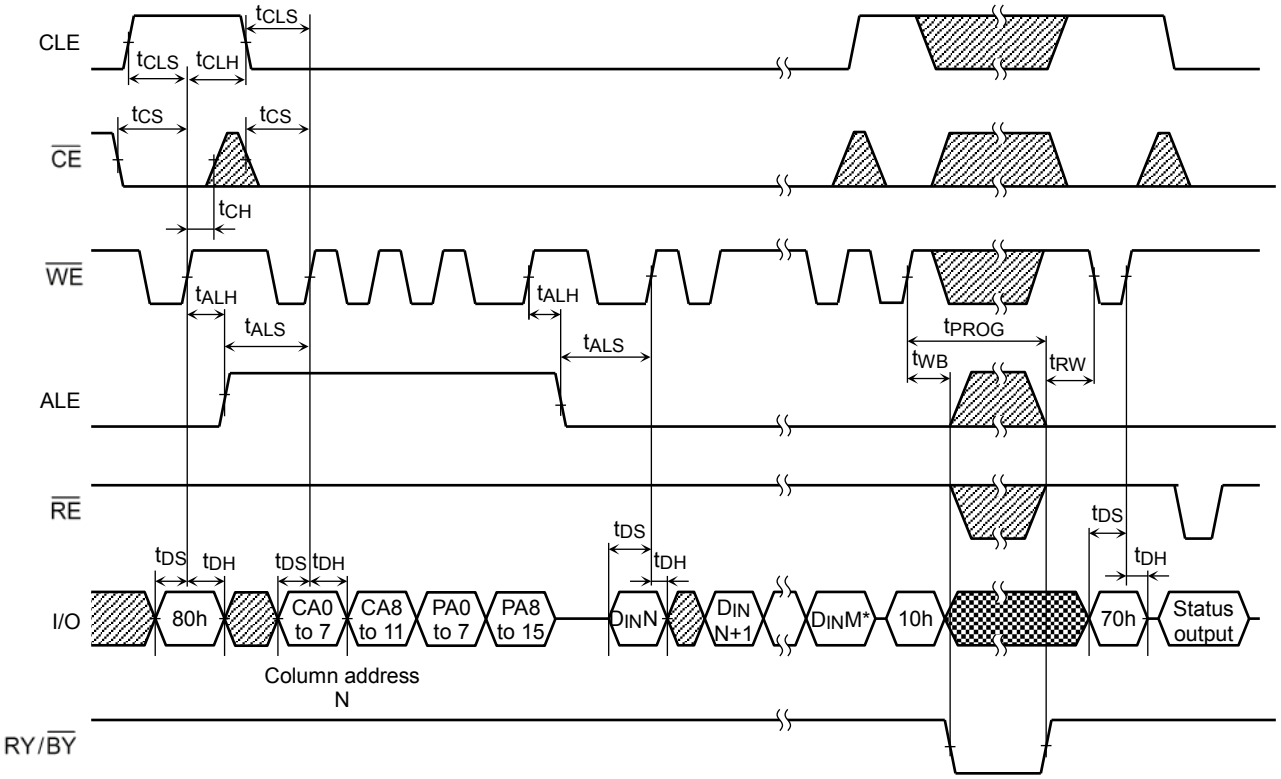


Continues from 1 of previous page

Data Output Timing Diagram



Auto-Program Operation Timing Diagram

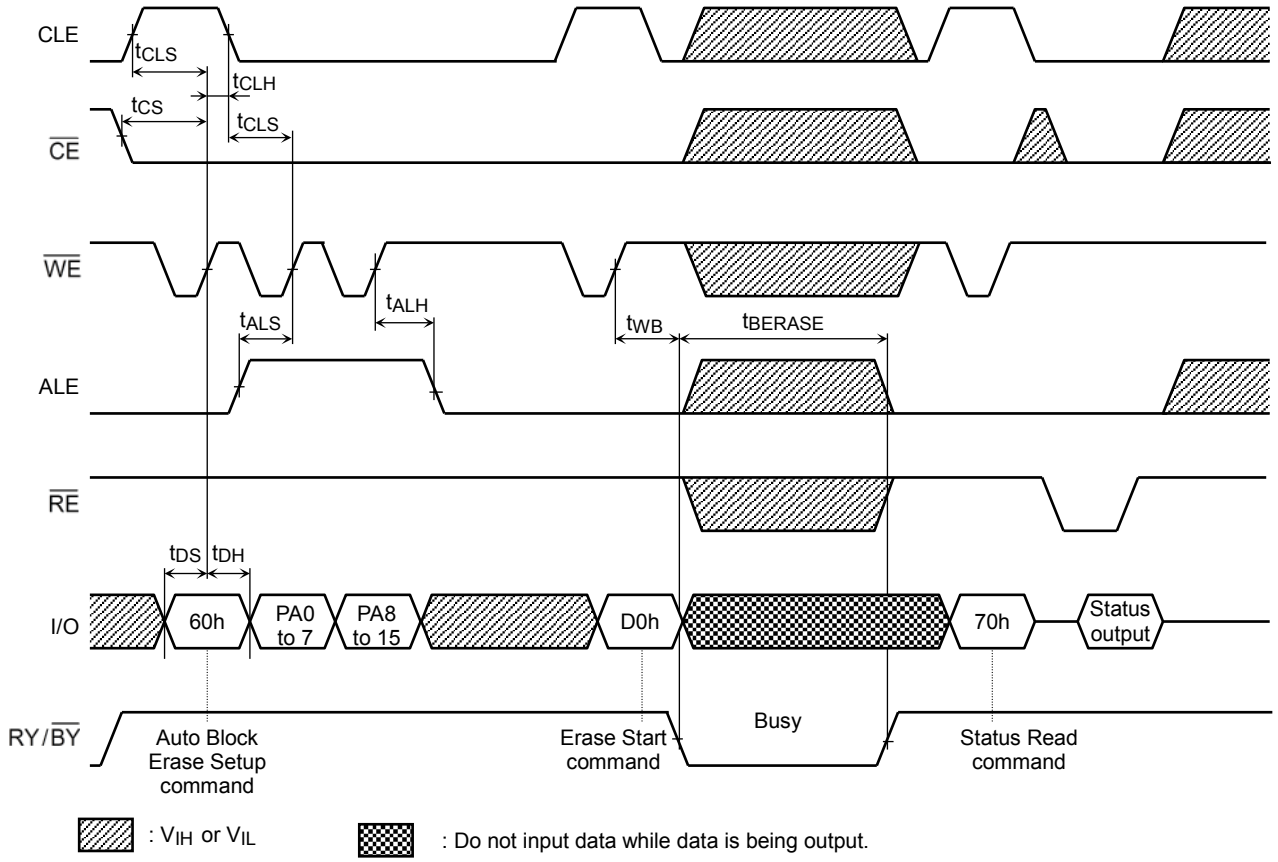


: Do not input data while data is being output.

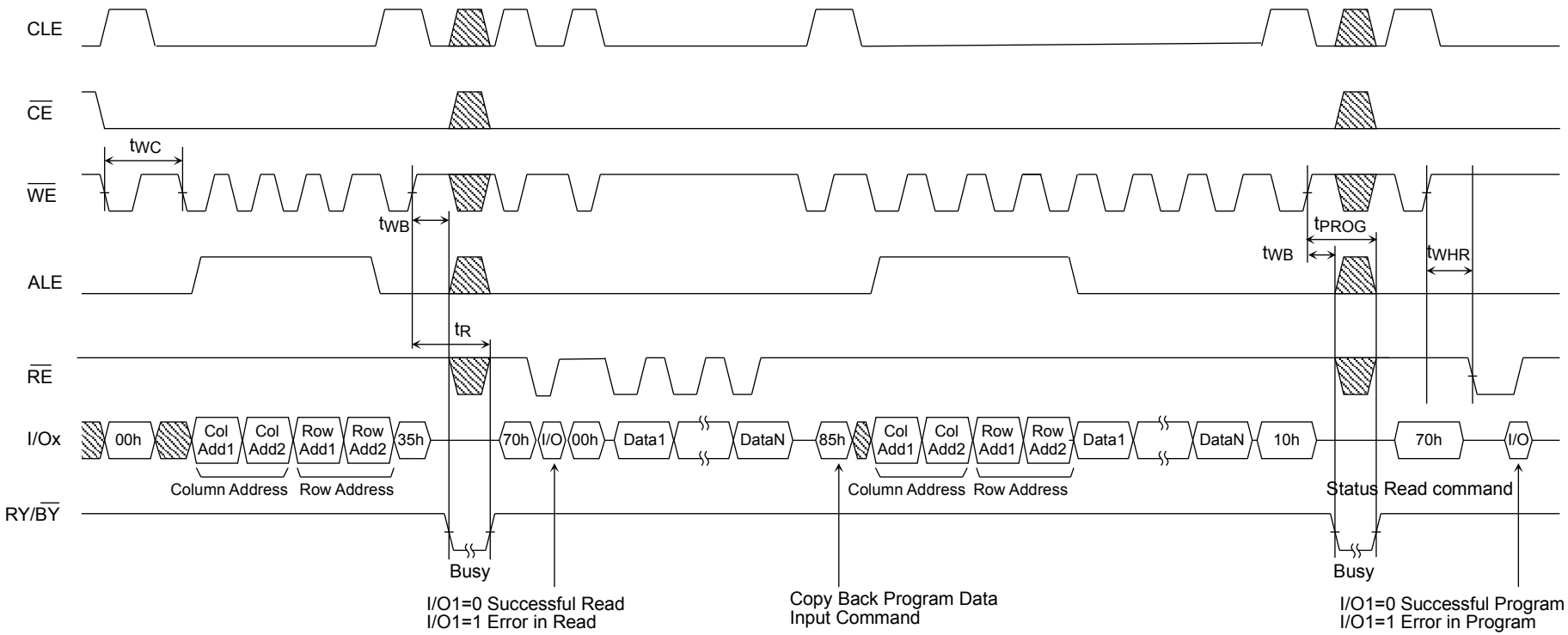
: V_{IH} or V_{IL}

*) M: up to 2111

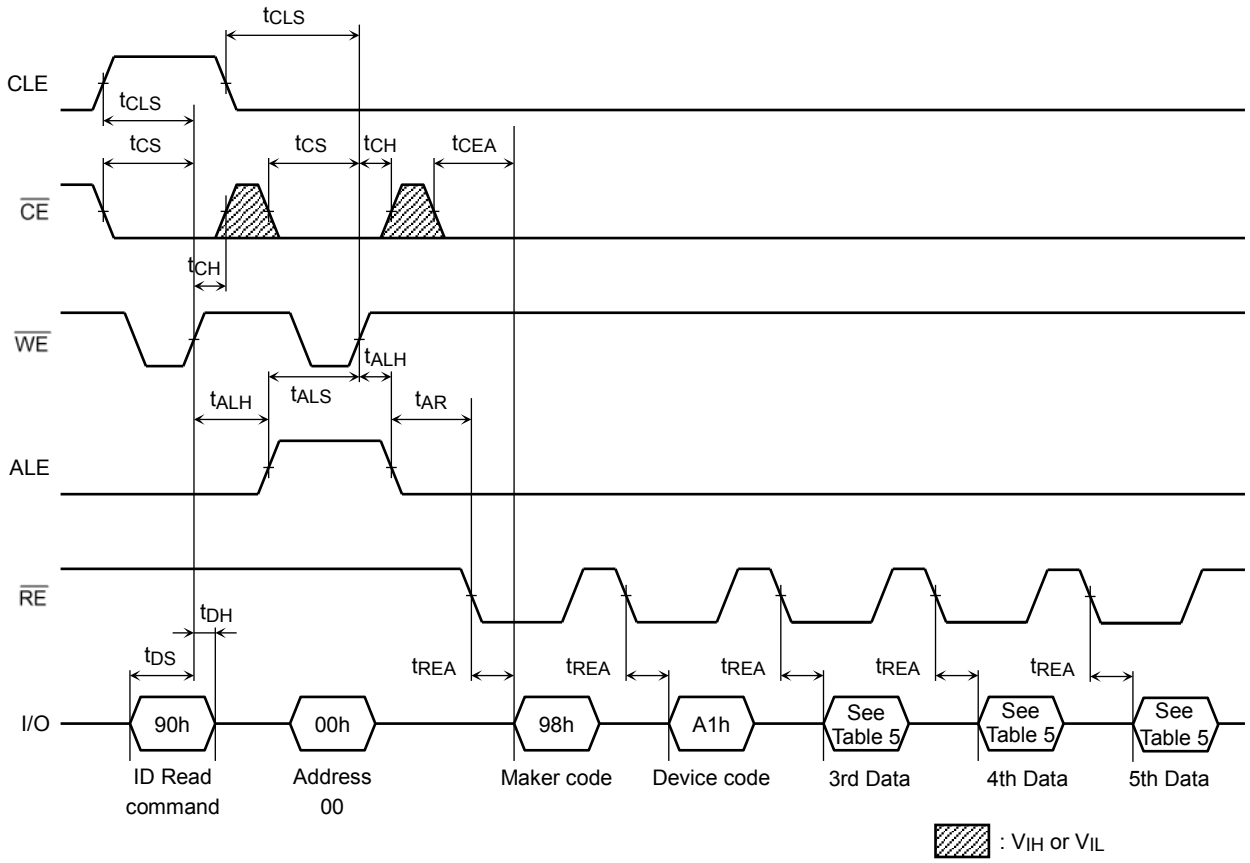
Auto Block Erase Timing Diagram



Copy Back Program with Random Data Input



ID Read Operation Timing Diagram



PIN FUNCTIONS

The device is a serial access memory which utilizes time-sharing input of address information.

Command Latch Enable: CLE

The CLE input signal is used to control loading of the operation mode command into the internal command register. The command is latched into the command register from the I/O port on the rising edge of the $\overline{WE}$ signal while CLE is High.

Address Latch Enable: ALE

The ALE signal is used to control loading address information into the internal address register. Address information is latched into the address register from the I/O port on the rising edge of $\overline{WE}$ while ALE is High.

Chip Enable: $\overline{CE}$

The device goes into a low-power Standby mode when $\overline{CE}$ goes High during the device is in Ready state. The $\overline{CE}$ signal is ignored when device is in Busy state ($RY/\overline{BY}$ = L), such as during a Program, Erase or Read operation, and will not enter Standby mode even if the $\overline{CE}$ input goes High.

Write Enable: $\overline{WE}$

The $\overline{WE}$ signal is used to control the acquisition of data from the I/O port.

Read Enable: $\overline{RE}$

The $\overline{RE}$ signal controls serial data output. Data is available t_{REA} after the falling edge of $\overline{RE}$.
The internal column address counter is also incremented (Address = Address + 1) on this falling edge.

I/O Port: I/O1 to 8

The I/O1 to 8 pins are used as a port for transferring address, command and input/output data to and from the device.

Write Protect: $\overline{WP}$

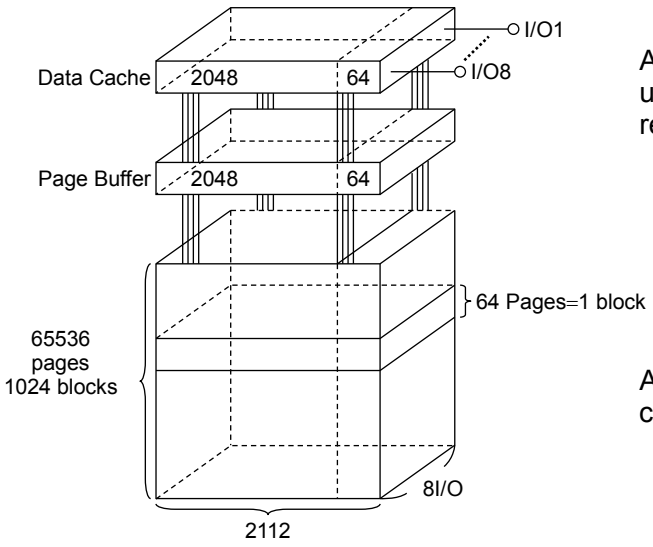
The $\overline{WP}$ signal is used to protect the device from accidental programming or erasing. The internal voltage regulator is reset when $\overline{WP}$ is Low. This signal is usually used for protecting the data during the power-on/off sequence when input signals are invalid.

Ready/Busy: RY / $\overline{BY}$

The $RY/\overline{BY}$ output signal is used to indicate the operating condition of the device. The $RY/\overline{BY}$ signal is in Busy state ($RY/\overline{BY}$ = L) during the Program, Erase and Read operations and will return to Ready state ($RY/\overline{BY}$ = H) after completion of the operation. The output buffer for this signal is an open drain and has to be pulled-up to V_{CC} with an appropriate resistor.

Schematic Cell Layout and Address Assignment

The Program operation works on page units while the Erase operation works on block units.



A page consists of 2112 bytes in which 2048 bytes are used for main memory storage and 64 bytes are for redundancy or for other uses.

1 page = 2112 bytes

1 block = 2112 bytes × 64 pages = (128K + 4K) bytes

Capacity = 2112 bytes × 64 pages × 1024 blocks

An address is read in via the I/O port over four consecutive clock cycles, as shown in Table 1.

Table 1. Addressing

	I/O8	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1
First cycle	CA7	CA6	CA5	CA4	CA3	CA2	CA1	CA0
Second cycle	L	L	L	L	CA11	CA10	CA9	CA8
Third cycle	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0
Fourth cycle	PA15	PA14	PA13	PA12	PA11	PA10	PA9	PA8

CA0 to CA11: Column address
PA0 to PA5: Page address in block
PA6 to PA15: Block address

Operation Mode: Logic and Command Tables

The operation modes such as Program, Erase, Read and Reset are controlled by command operations shown in Table 3. Address input, command input and data input/output are controlled by the CLE, ALE, $\overline{CE}$, $\overline{WE}$, $\overline{RE}$ and $\overline{WP}$ signals, as shown in Table 2.

Table 2. Logic Table

	CLE	ALE	$\overline{CE}$	$\overline{WE}$	$\overline{RE}$	$\overline{WP}$ *1
Command Input	H	L	L	⌐└⌐	H	*
Data Input	L	L	L	⌐└⌐	H	H
Address Input	L	H	L	⌐└⌐	H	*
Serial Data Output	L	L	L	H	¬└¬	*
During Program (Busy)	*	*	*	*	*	H
During Erase (Busy)	*	*	*	*	*	H
During Read (Busy)	*	*	H	*	*	*
	*	*	L	H (*2)	H (*2)	*
Program, Erase Inhibit	*	*	*	*	*	L
Standby	*	*	H	*	*	0 V/V_{CC}

H: V_{IH}, L: V_{IL}, *: V_{IH} or V_{IL}

*1: Refer to Application Note (10) toward the end of this document regarding the $\overline{WP}$ signal when Program or Erase Inhibit.

*2: If $\overline{CE}$ is low during read busy, $\overline{WE}$ and $\overline{RE}$ must be held High to avoid unintended command/address input to the device or read to device. Reset or Status Read command can be input during Read Busy.

Table 3. Command table (HEX)

	First Set	Second Set	Acceptable while Busy
Serial Data Input	80	—	
Read	00	30	
Column Address Change in Serial Data Output	05	E0	
Auto Page Program	80	10	
Column Address Change in Serial Data Input	85	—	
Read for Copy-Back	00	35	
Copy-Back Program	85	10	
Auto Block Erase	60	D0	
ID Read	90	—	
Status Read	70	—	○
ECC Status Read	7A	—	
Reset	FF	—	○

HEX data bit assignment

(Example)

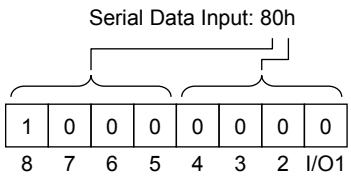


Table 4. Read mode operation states

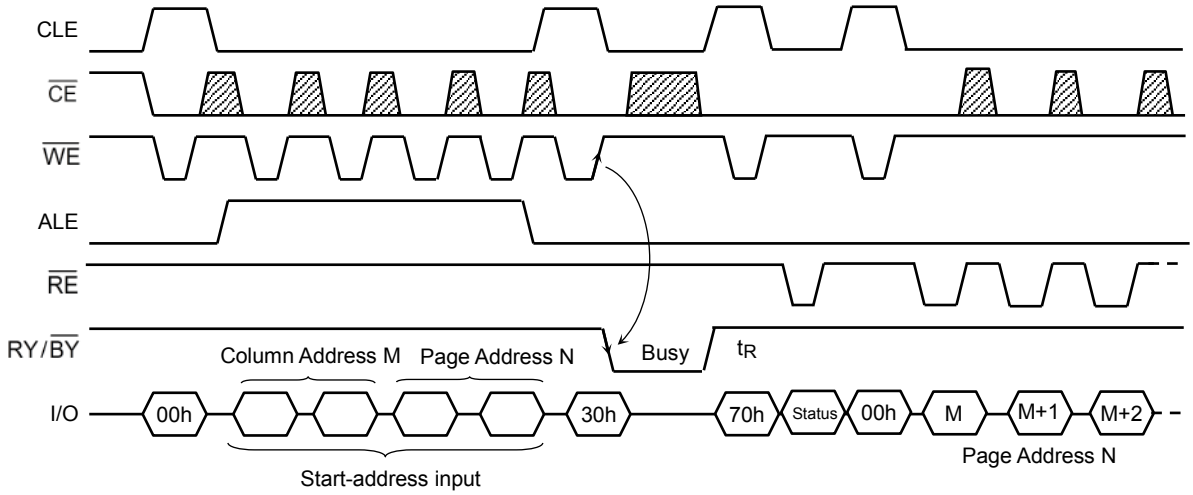
	CLE	ALE	$\overline{CE}$	$\overline{WE}$	$\overline{RE}$	I/O1 to I/O8	Power
Output select	L	L	L	H	L	Data output	Active
Output Deselect	L	L	L	H	H	High impedance	Active

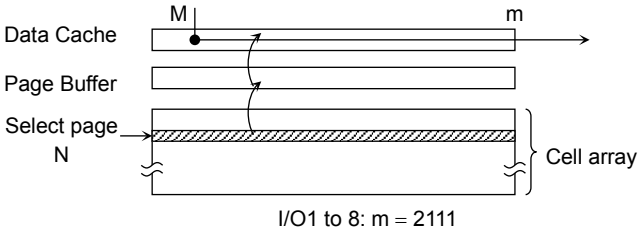
H: V_{IH}, L: V_{IL}

DEVICE OPERATION

Read Mode

Read mode is set when the "00h" and “30h” commands are issued to the Command register. Between the two commands, a start address for the Read mode needs to be issued. After initial power on sequence, “00h” command is latched into the internal command register. Therefore read operation after power on sequence is executed by the setting of only four address cycles and “30h” command. Refer to the figures below for the sequence and the block diagram (Refer to the detailed timing chart).

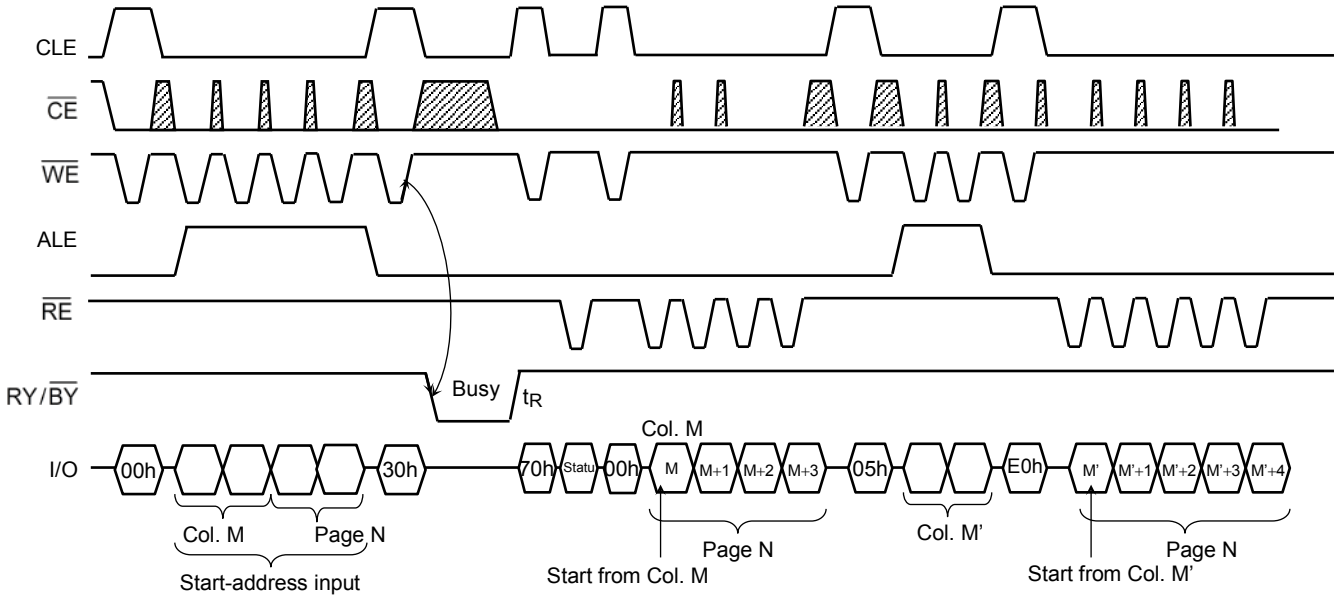


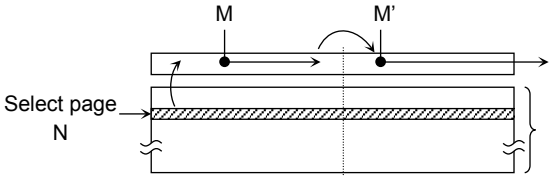


A data transfer operation from the cell array to the Data Cache via Page Buffer starts on the rising edge of $\overline{WE}$ in the 30h command input cycle (after the address information has been latched). The device will be in the Busy state during this transfer period.

After the transfer period, the device returns to Ready state. Serial data can be output synchronously with the $\overline{RE}$ clock from the start address designated in the address input cycle.

Random Column Address Change in Read Cycle





During the serial data output from the register, the column address can be changed by inputting a new column address using the 05h and E0h commands. The data is read out in serial starting at the new column address. Random Column Address Change operation can be done multiple times within the same page.

ECC & Sector definition for ECC

Internal ECC logic generates Error Correction Code during busy time in program operation. The ECC logic manages 9bit error detection and 8bit error correction in each 528Bytes of main data and spare data. A section of main field (512Bytes) and spare field (16Bytes) are paired for ECC. During read, the device executes ECC of itself. Once read operation is executed, Status Read Command (70h) can be issued to check the read status. The read status remains until other valid commands are executed.

To use ECC function, below limitation must be considered.

- A sector is the minimum unit for program operation and the number of program per page must not exceed 4.

2KByte Page Assignment

1st Main	2nd Main	3rd Main	4th Main	1st Spare	2nd Spare	3rd Spare	4th Spare
512B	512B	512B	512B	16B	16B	16B	16B

Note) Internal ECC manages all data of Main area and Spare area.

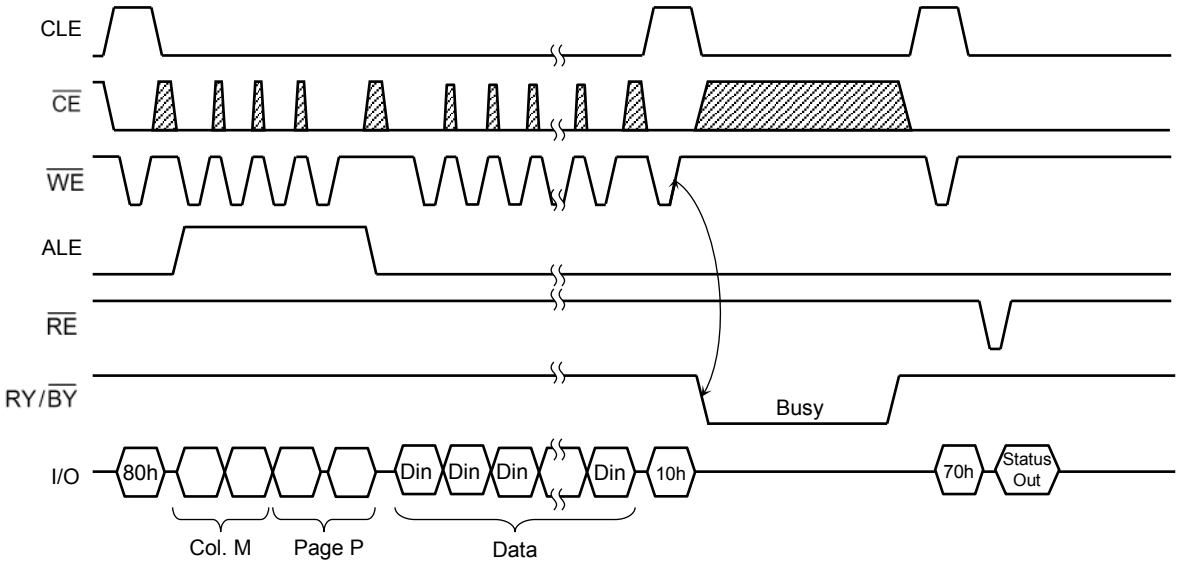
Definition of 528Byte Sector

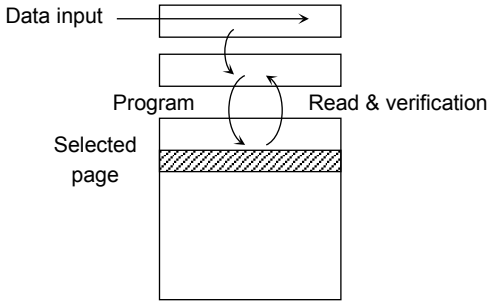
Sector	**Column Address (Byte)**	
	Main Field	**Spare Field**
1st Sector	0 to 511	2,048 to 2,063
2nd Sector	512 to 1,023	2,064 to 2,079
3rd Sector	1,024 to 1,535	2,080 to 2,095
4th Sector	1,536 to 2,047	2,096 to 2,111

Note) The ECC parity code generated by internal ECC is stored in column addresses 2112-2175 and the user cannot access to these specific addresses.
While using the Partial Page Program, the user must program the data to main field and spare field simultaneously by the definition of sector.

Auto Page Program Operation

The device carries out an Automatic Page Program operation when it receives a "10h" Program command after the address and data have been input. The sequence of command, address and data input is shown below (Refer to the detailed timing chart).





The data is transferred (programmed) from the Data Cache via the Page Buffer to the selected page on the rising edge of $\overline{WE}$ following input of the “10h” command. After programming, the programmed data is transferred back to the Page Buffer to be automatically verified by the device. If the programming does not succeed, the Program/Verify operation is repeated by the device until success is achieved or until the maximum loop number set in the device is reached.

Random Column Address Change in Auto Page Program Operation

The column address can be changed by the 85h command during the data input sequence of the Auto Page Program operation.

Two address input cycles after the 85h command are recognized as a new column address for the data input. After the new data is input to the new column address, the 10h command initiates the actual data program into the selected page automatically. The Random Column Address Change operation can be repeated multiple times within the same page.