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TOSHIBA
Serial Interface NAND
Technical Data Sheet

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TOSHIBA

Storage & Electronic Devices Solutions

Memory Division

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1. Introduction

1.1. General Description

The TC58CVG2S0HxAIx is a serial interface NAND Flash for embedded applications which supports the SPI interface.
The TC58CVG2S0HxAIx is organized as (4096 + 128) bytes × 64 pages × 2048 blocks. The device has a 4224 byte data buffer which allows program and read data to be transferred between the buffer and the memory cell array in 4224-byte increments. The Erase Operation is implemented in a single block unit (256 Kbytes + 8 Kbytes: 4224 bytes × 64 pages). The device has the high speed mode for sequential Page Read Operation. When high speed mode is enabled, the average of tR is shortened.
The TC58CVG2S0HxAIx has ECC logic on the chip and 8bit read errors for each (512 bytes + 16 bytes) can be corrected. The internal ECC logic has detailed bit flip count report.

1.2. Definitions and Abbreviations

SPI
Serial Peripheral Interface.

Address
The address is comprised of a column address (CA) with 13bits and a row address (RA) with 17bits. The row address identifies the page and block to be accessed. The column address identifies the byte within a page to access.

Column
The byte location within the page.

Row
Refer to the block and page to be accessed.

Sector
The 512 bytes unit in a page.

Page
The smallest addressable unit for the Read and the Program operations.

Block
Consists of multiple pages and is the smallest addressable unit for the Erase Operation.

Data Buffer
Buffer used to transfer data to and from the cell array.

Cell Array
Memory cell of NAND flash

Device
The packaged NAND unit.

1.3. Features

- **Organization**

  Organization (Internal ECC is enabled, default)

Memory Cell Array	4224 × 64 × 2048 × 8 bits
Data Buffer	4224 × 8 bits
Page Size	4224 bytes
Block Size	(256K + 8K) bytes

  Organization (Internal ECC is disabled)

Memory Cell Array	4352 × 64 × 2048 × 8 bits
Data Buffer	4352 × 8 bits
Page Size	4352 bytes
Block Size	(256K + 16K) bytes

- **ECC**

  8 bit ECC for each 512bytes is required. The device has ECC logic internally.

- **Mode**

  Page Read, Page Program, Block Erase, Internal Data Move, Reset, Write Enable, Write Disable, Block Lock, Get Feature, Set Feature, Block Protection, Parameter Page Read, Read ID, Unique ID Read

- **Power Supply**

  V_{CC} = 2.7 V to 3.6 V

- **Access Time**

Cell Array to Data Buffer	280 μs max
	115 μs typ
Data Transfer rate	104 MHz max

- **Program/Erase Time**

Programming Time	450 μs/page typ
Block Erasing Time	2.0 ms/block typ

- **Operating Current**

Read Operation Current with HSE on (Average)	21 mA max
Read Operation Current with HSE off (Average)	15 mA max
Program Operation Current (Average)	18 mA max
Erase Operation Current (Average)	22 mA max
Standby Current	180 μA max
	35 uA typ

- **Reliability**

  Refer to reliability note.

- **Package**

- SOP16 (P-SOP16-1111-1.27-001)
- WSON8 (P-WSON8-0608-1.27-003)

2. Memory Organization

2.1. Pin Descriptions

Table 1 Pin Descriptions

Pin Name	Pin Function
$\overline{CS}$	Chip Select
SO/SO1	Serial Data Output / Serial Data Output 1
$\overline{WP}$/SO2	Write Protect / Serial Data Output 2
SI/SO0	Serial Data Input / Serial Data Output 0
$\overline{HOLD}$/SO3	Hold Input / Serial Data Output 3
SCK	Serial Clock Input
VCC	Power Supply
VSS	Ground

Note:

If the WP pin is low and BRWD bit is set to 1, the overwrite for the BRWD(bit [7]) and the BL bits (bits [5:3]) in address A0h of the feature table shown in Table 12 is prohibited.

The users cannot drive the WP pin while CS pin is low.

The HOLD pin and the WP pin are pull up to VCC internally.

2.2. Pin Assignment (Top View)

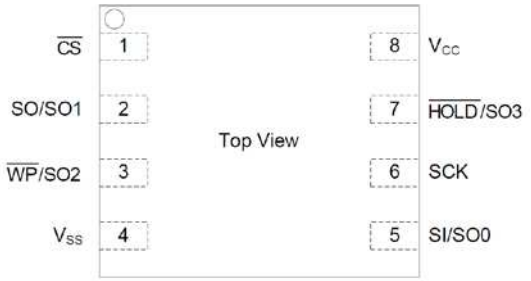


Figure 1. WSON8 Pin Assignment (Top View)

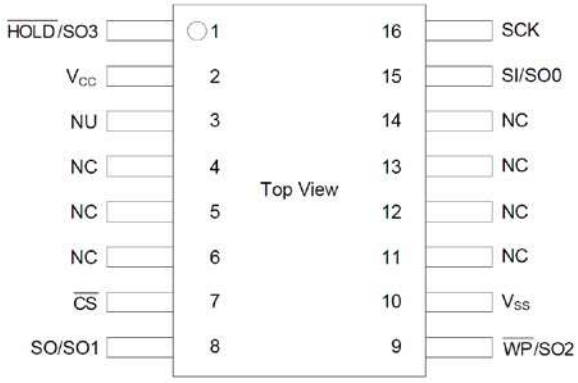


Figure 2. SOP16 Pin Assignment (Top View)

2.3. Block Diagram

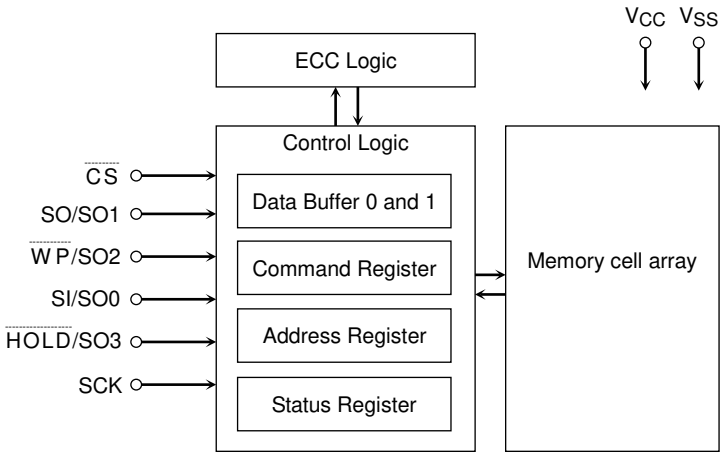


Figure 3. Block Diagram

2.4. Cell Layout

The Program Operation works on page units while the Erase Operation works on block units.
When internal ECC is turned ON the default setting, a page consists of 4224 bytes in which 4096 bytes are used for main memory storage and 128 bytes are used for redundancy or for other uses. In the case that internal ECC is turned OFF, the redundancy area will be expanded to 256 bytes automatically.

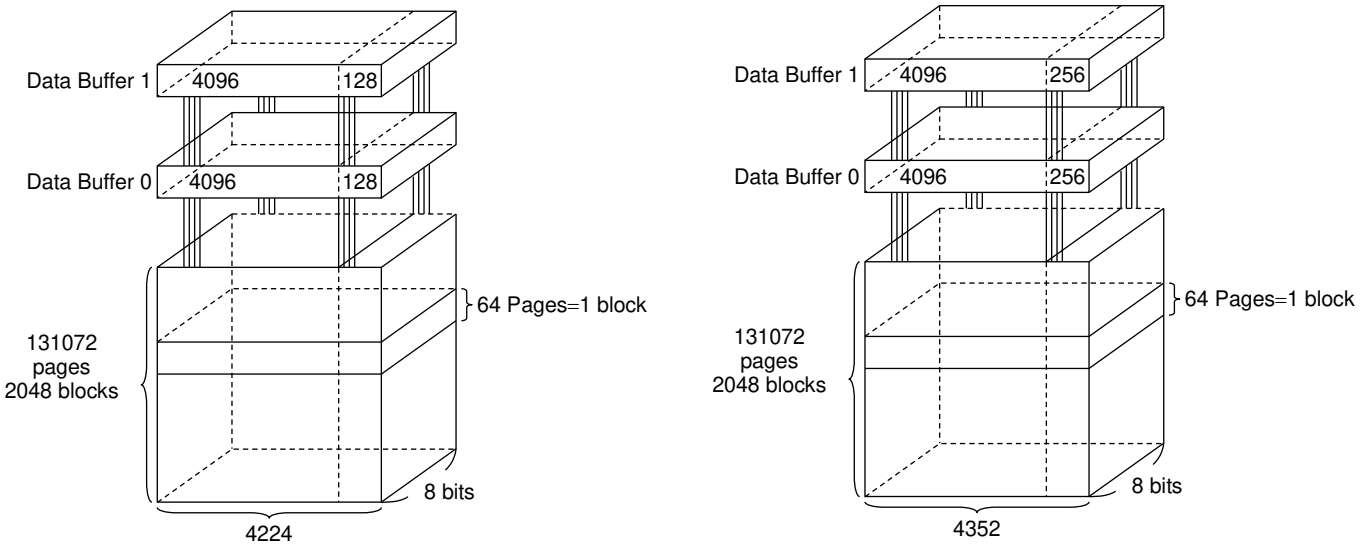
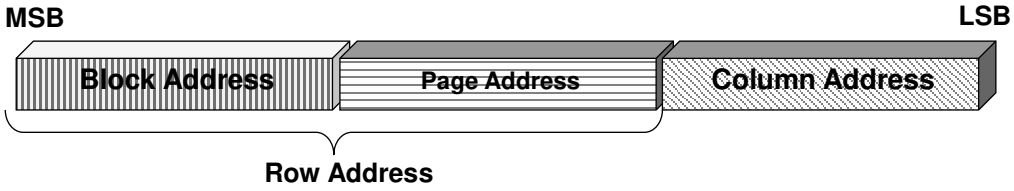


Figure 4. Cell Layout

2.5. Addressing

There are two address types used: the column address and the row address. The column address is used to access bytes within a page. The row address is used to address pages and blocks. There are some functions that may require only row addresses, such as Block Erase.



Row Address: 17 bits
Block Address (2048 blocks/device): 11 bits
Page Address (64 pages/block): 6 bits
Column Address: 13 bits
Column Address (4224 or 4352 bytes/page): 13 bits

Figure 5. Addressing

2.6. Valid Blocks

Table 2 Valid Blocks

Symbol	Parameter	Min.	Typ.	Max.	Unit
N_{VB}	Number of Valid Blocks	2008	-	2048	Block

Note:
The device occasionally contains unusable blocks.
The first block (Block 0) is guaranteed to be a valid block at the time of shipment.
The specification for the minimum number of valid blocks is applicable over the lifetime

3. Physical Interface

3.1. Absolute Maximum Rating

Stresses greater than those listed in Table 3 may cause permanent damage to the device. This is a stress rating only.

Table 3 Absolute Maximum Rating

Symbol	Parameter	Value	Unit
V_{CC}	Power Supply Voltage	–0.3 to 3.9	V
V_{IN}	Input Voltage	–0.3 to V_{CC} + 0.3 (≤ 3.9 V)	V
$V_{I/O}$	Input /Output Voltage	–0.3 to V_{CC} + 0.3 (≤ 3.9 V)	V
P_{D1}	Power Dissipation 1	0.42	W
P_{D2}	Power Dissipation 2 (WSON8 ePAD without solder)	0.27	W
T_{SOLDER}	Soldering Temperature (10 s)	260	°C
T_{STG}	Storage Temperature	–55 to 150	°C
T_{OPR}	Operating Temperature	-40 to 85	°C

3.2. Capacitance

Table 4 Capacitance (T_{OPR} = 25℃, f = 1MHz)

Symbol	Parameter	Condition	Min.	Max.	Unit
C_{IN}	Input	V_{IN} = 0 V	-	2.5	pF
C_{OUT}	Output	V_{OUT} = 0 V	-	4	pF

Note: This parameter is periodically sampled and is not tested for every device.

3.3. Recommended DC Operating Conditions

Table 5 Recommended DC Operating Condition

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Power Supply Voltage	2.7	-	3.6	V
V_{IH}	High Level input Voltage	V_{CC} × 0.8	-	V_{CC} + 0.3	V
V_{IL}	Low Level Input Voltage	-0.3	-	V_{CC} × 0.2	V

3.4. Signal Timing

The device supports SPI mode 0 and mode 3. Input data is latched at the rising edge of SCK and data is output at the falling edge of SCK for mode 0 and 3. When HOLD goes Low, the communication is held. The hold state begins the falling edge of SCK.

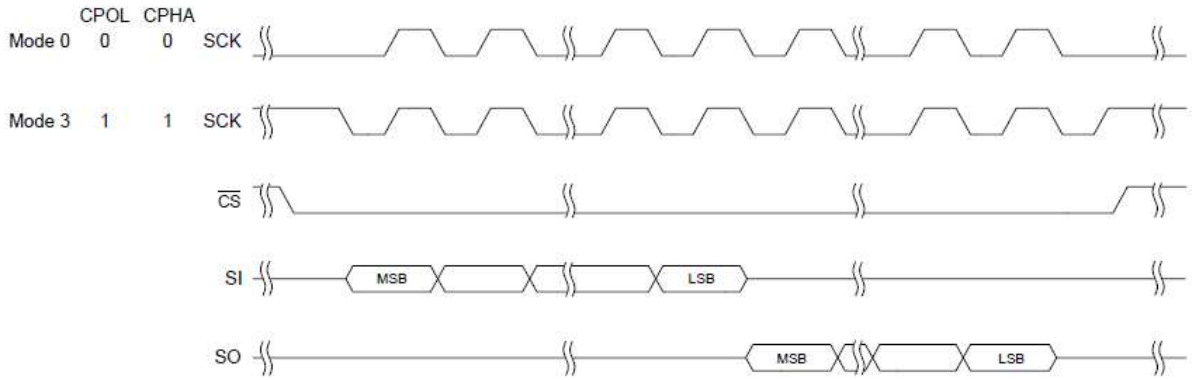


Figure 6. SPI Timing

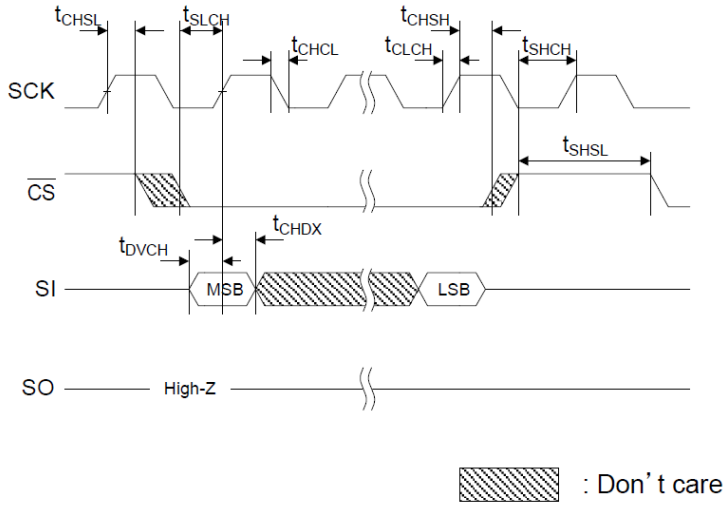


Figure 7. Serial Input Timing

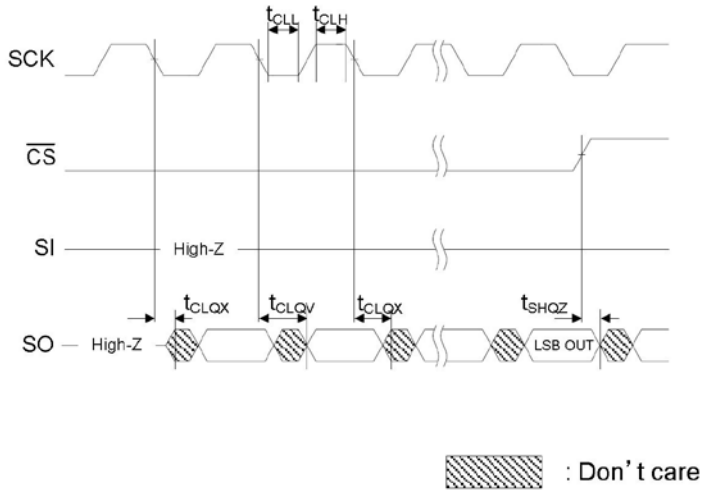


Figure 8. Serial Output Timing

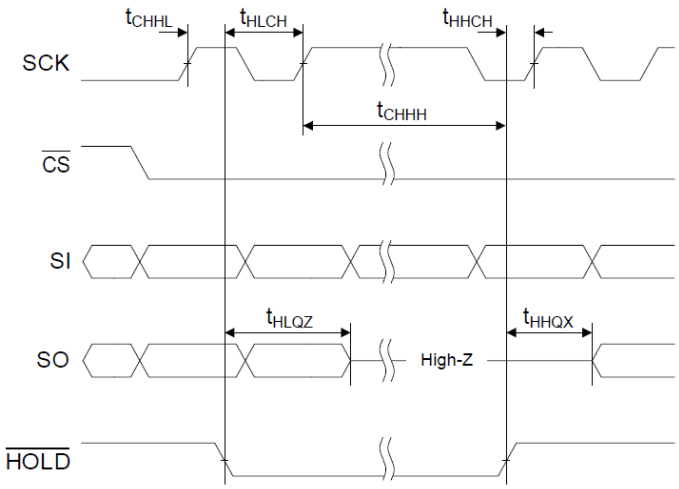


Figure 9. Hold Timing

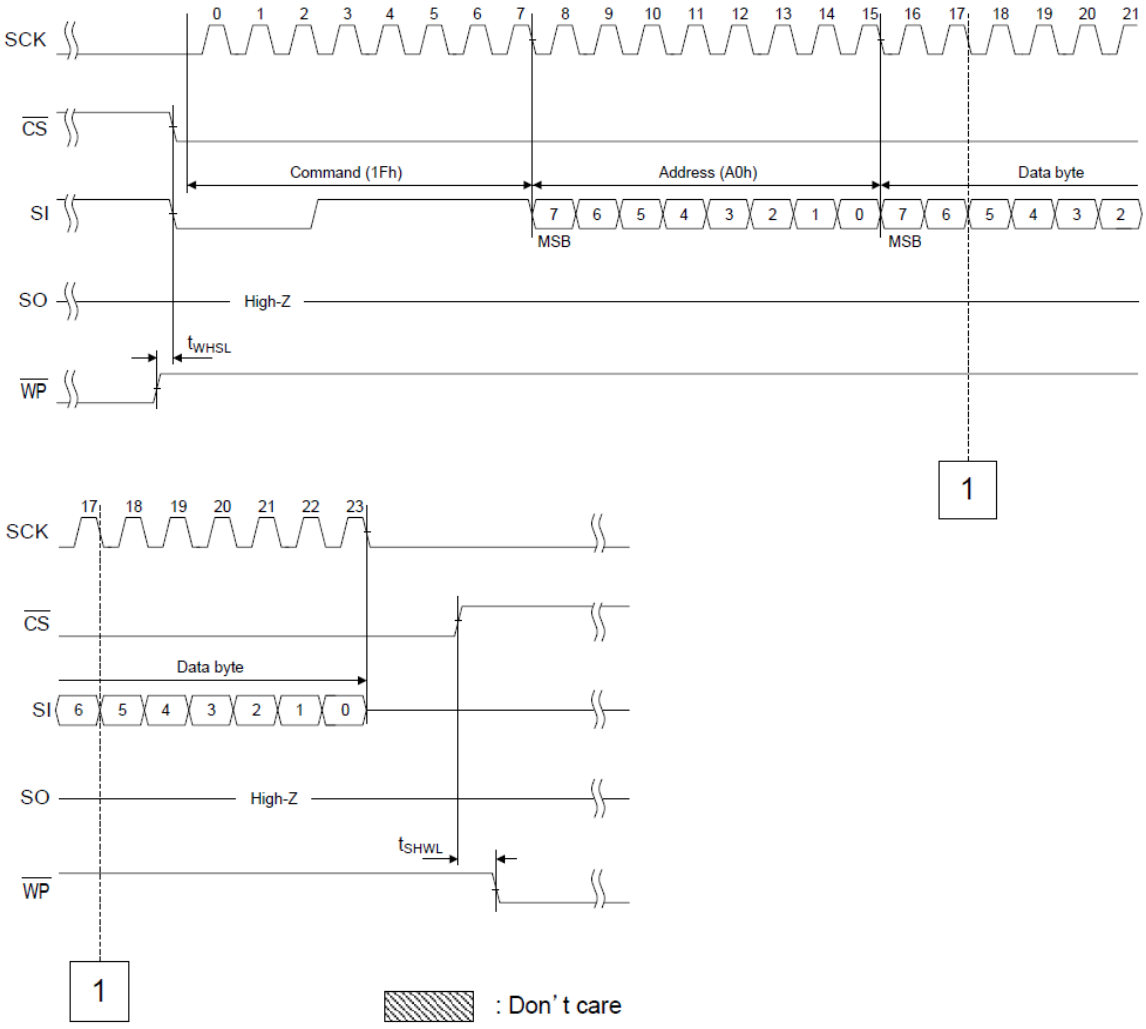


Figure 10. WP Timing (Example)

3.5. AC Characteristics

Table 6 AC Characteristics (T_{OPR} = -40 to 85℃, VCC = 2.7 to 3.6V)

Symbol	Parameter	Min.	Typ.	Max.	Unit
F_C	Serial Clock Frequency For: all command	-	-	104	MHz
t_{CLH}	Serial Clock High Time	4.5	-	-	ns
t_{CLL}	Serial Clock Low Time	4.5	-	-	ns
t_{CLCH}	Serial Clock Rise Time (Slew Rate)	0.1	-	-	V/ns
t_{CHCL}	Serial Clock Fall Time (Slew Rate)	0.1	-	-	V/ns
t_{SLCH}	$\overline{CS}$ Active Setup Time	4.6	-	-	ns
t_{CHSH}	$\overline{CS}$ Active Hold Time	5	-	-	ns
t_{SHCH}	$\overline{CS}$ Not Active Setup Time	5	-	-	ns
t_{CHSL}	$\overline{CS}$ Not Active Hold Time	5	-	-	ns
t_{SHSL} / t_{CS}	$\overline{CS}$ High Time	100	-	-	ns
t_{SHQZ}	Output Disable Time	-	-	20	ns
t_{CLQX}	Output Hold Time	1	-	-	ns
t_{DVCH}	Data In Setup Time	2	-	-	ns
t_{CHDX}	Data In Hold Time	5	-	-	ns
t_{HLCH}	$\overline{HOLD}$ Low Setup Time (relative to Clock)	5	-	-	ns
t_{HHCH}	$\overline{HOLD}$ High Setup Time (relative to Clock)	5	-	-	ns
t_{CHHL}	$\overline{HOLD}$ High Hold Time (relative to Clock)	5	-	-	ns
t_{CHHH}	$\overline{HOLD}$ Low Hold Time (relative to Clock)	5	-	-	ns
t_{HLQZ}	$\overline{HOLD}$ Low To High-Z Output	-	-	7	ns
t_{HHQX}	$\overline{HOLD}$ High To Output	-	-	7	ns
t_{CLQV}	Clock Low To Output Valid	-	-	7.0(CL=10pF) 7.5(CL=20pF) 8.0(CL=30pF)	ns
t_{WHSL}	$\overline{WP}$ Setup Time Before $\overline{CS}$ Low	20	-	-	ns
t_{SHWL}	$\overline{WP}$ Hold Time After $\overline{CS}$ High	100	-	-	ns

3.6. DC Operating Characteristics

Table 7 DC & Operating Characteristics (T_{OPR} = -40 to 85℃, VCC = 2.7 to 3.6V)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
I_{IL}	Input Leakage Current	V_{IN} = 0 V to V_{CC}	-	-	±10	μA
I_{LO}	Output Leakage Current	V_{OUT} = 0 V to V_{CC}	-	-	±10	μA
I_{CCOA1}	Read Operation Current (Average)	Fc = 104MHz High Speed Mode = Enable Read Buffer Command : 03h or 0Bh (x1)	-	-	21	mA
I_{CCOA2}	Read Operation Current (Average)	Fc = 104MHz High Speed Mode = Disable Read Buffer Command : 03h or 0Bh (x1)	-	-	15	mA
I_{CCOA3}	Program Operation Current (Average)	Fc = 104MHz	-	-	18	mA
I_{CCOA4}	Erase Operation Current (Average)	Fc = 104MHz	-	-	22	mA
I_{CCS}	Standby Current	$\overline{CS}$= V_{CC} – 0.2 V, $\overline{WP}$ = V_{CC}, $\overline{HOLD}$ = V_{CC}	-	35	180	μA
V_{OH}	High Level Output Voltage	I_{OH} = –0.1 mA	Vcc-0.2	-	-	V
V_{OL}	Low Level Output Voltage	I_{OL} = 0.1 mA	-	-	0.2	V

Note:

Refer to the High Speed Mode in 4.3.

ICCOA1~ICCOA4 are the average current during the full operation sequence.

3.7. Programming, Reading and Erasing Characteristics

Table 8 Programming, Reading and Erasing Characteristics (T_{OPR} = -40 to 85℃, VCC = 2.7 to 3.6V)

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_{PROG}	Average Programming Time	-	450	600	μs
N	Number of Partial Program Cycles in the Same Page	-	-	4	time
t_{BERASE}	Block Erasing Time	-	2	7	ms
t_R	Cell Array to the Buffer (with ECC)	-	115	280	μs
t_{RHSA4}	Average Read Time for Sequential Read (High Speed Mode, x4)	-	35	-	μs
t_{RST}	Device Reset Time (Read)	-	-	280	μs
	Device Reset Time (Program)	-	-	600	μs
	Device Reset Time (Erase)	-	-	7	ms

Note:

Refer to the data pair of ECC calculation in 4.16 Internal ECC.

Refer to the High Speed Mode in 4.3.

t_R is the average busy time for page read operation of 64pages continuously in a block.

t_{RHSA4} is the average busy time for sequential page read operation with all data output in each page of 64pages continuously in a block.

The busy time after Protect Execute command is shorter than t_{PROG} (Max.).

3.8. Power ON/OFF Sequence

The timing sequence shown in the figure below is necessary for the power ON/OFF sequence.

The device internal initialization starts after the power supply reaches an appropriate level in the power on sequence. The users cannot issue any commands while t_{VSL}. From the end of t_{VSL} to the end of t_{VOP}, Get Feature Operation and Reset Operation can be issued. OIP bit in the feature table indicates the busy state in this time period. All operations are available after t_{VOP}.

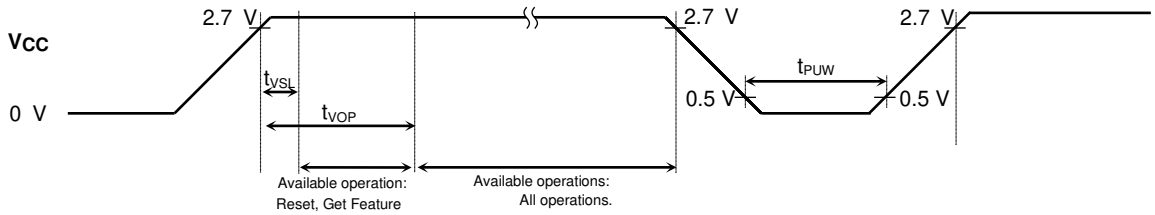


Figure 11. Power ON/OFF Sequence

Table 9 Power on Timing

Symbol	Parameter	Min.	Max.	Unit
t_{VSL}	VCC(min) to $\overline{CS}$ Low	-	100	μs
t_{VOP}	VCC(min) to all operation	-	1.1	ms
t_{PUW}	Waiting time for power on	1	-	ms
VCCSR	VCC Slew Rate	-	216	mV/μs

3.9. AC Test Condition

Table 10 AC Test Condition

PARAMETER	CONDITION
	V_{CC}: 2.7 to 3.6V
Input level	V_{CC} × 0.2 to V_{CC} × 0.8
Input pulse rise and fall time	2 ns
Input comparison level	Vcc / 2
Output data comparison level	Vcc / 2
Output load	C_L (30pF) + 1 TTL

4. Command Description and Device Operation

4.1. Command Set

Table 11 Command Set

Operation	Byte 1 (CMD)	Byte 2	Byte 3	Byte 4	Byte 5	Byte N
Read Cell Array	13h	Dummy + A16 (Input)	A15-A8 (Input)	A7-A0 (Input)	-	-
Read Buffer	03h/0Bh	Dummy + A12-A8 (Input)	A7-A0 (Input)	Dummy	D*-D* (Output)	D*-D* (Output)
Read Buffer x2	3Bh	Dummy + A12-A8 (Input)	A7-A0 (Input)	Dummy	D*-D* (Output)	D*-D* (Output)
Read Buffer x4	6Bh	Dummy + A12-A8 (Input)	A7-A0 (Input)	Dummy	D*-D* (Output)	D*-D* (Output)
Program Load	02h	Dummy + A12-A8 (Input)	A7-A0 (Input)	D*-D* (Input)	D*-D* (Input)	D*-D* (Input)
Program Execute	10h	Dummy + A16 (Input)	A15-A8 (Input)	A7-A0 (Input)	-	-
Protect Execute	2Ah	Dummy + A16 (Input)	A15-A8 (Input)	A7-A0 (Input)	-	-
Program Load Random Data	84h	Dummy + A12-A8 (Input)	A7-A0 (Input)	D*-D* (Input)	D*-D* (Input)	D*-D* (Input)
Block Erase	D8h	Dummy + A16 (Input)	A15-A8 (Input)	A7-A0 (Input)	-	-
Reset	FFh/FEh	-	-	-	-	-
Write Enable	06h	-	-	-	-	-
Write Disable	04h	-	-	-	-	-
Get Feature	0Fh	A7-A0 (Input)	D7-D0 (Output)	D7-D0 (Output)	D7-D0 (Output)	D7-D0 (Output)
Set Feature	1Fh	A7-A0 (Input)	D7-D0 (Input)	-	-	-
Read ID	9Fh	Dummy	ID (Output)	ID (Output)	-	-

Note:

1) Input of a command other than those specified in Table 11 is prohibited. Stored data may be corrupted if an unknown command is entered during the command cycle.

2) During the operation in progress, do not input any command except 0Fh, FFh and FEh.

3) The user can issue the Protect Execute (2Ah) only one time for each block.

4) Once the Get Feature command is issued, the status and setting information are outputted continuously.

4.2. Page Read Operation

The Read Cell Array and Read Buffer commands are required to read the data in a page. The Read Cell Array command reads the page data from the NAND cell array to the data buffer. The Read Buffer command reads the data from the data buffer. The operation sequence is as follows.

1. Read Cell Array (13h) : To read the data from the cell array to the internal data buffer.
2. Get Feature (0Fh) : To read the status (OIP, ECCS0 and ECCS1 bits) of the device.
3. Read Buffer (03h or 0Bh) : To output the data from the internal data buffer.
   or Read Buffer x2 (3Bh)
   or Read Buffer x4 (6Bh)

Read Buffer, Read Buffer x2, Read Buffer x4 and Get Feature commands are repeatable commands.
For the Read Buffer x2 and Read Buffer x4 read modes are available as shown in Figure 14 and Figure 15.
The users are able to check the detailed bit flip count using ECC Bit Flip Count Detection and other functions using Get Feature command.

4.2.1. Read Cell Array (13h)

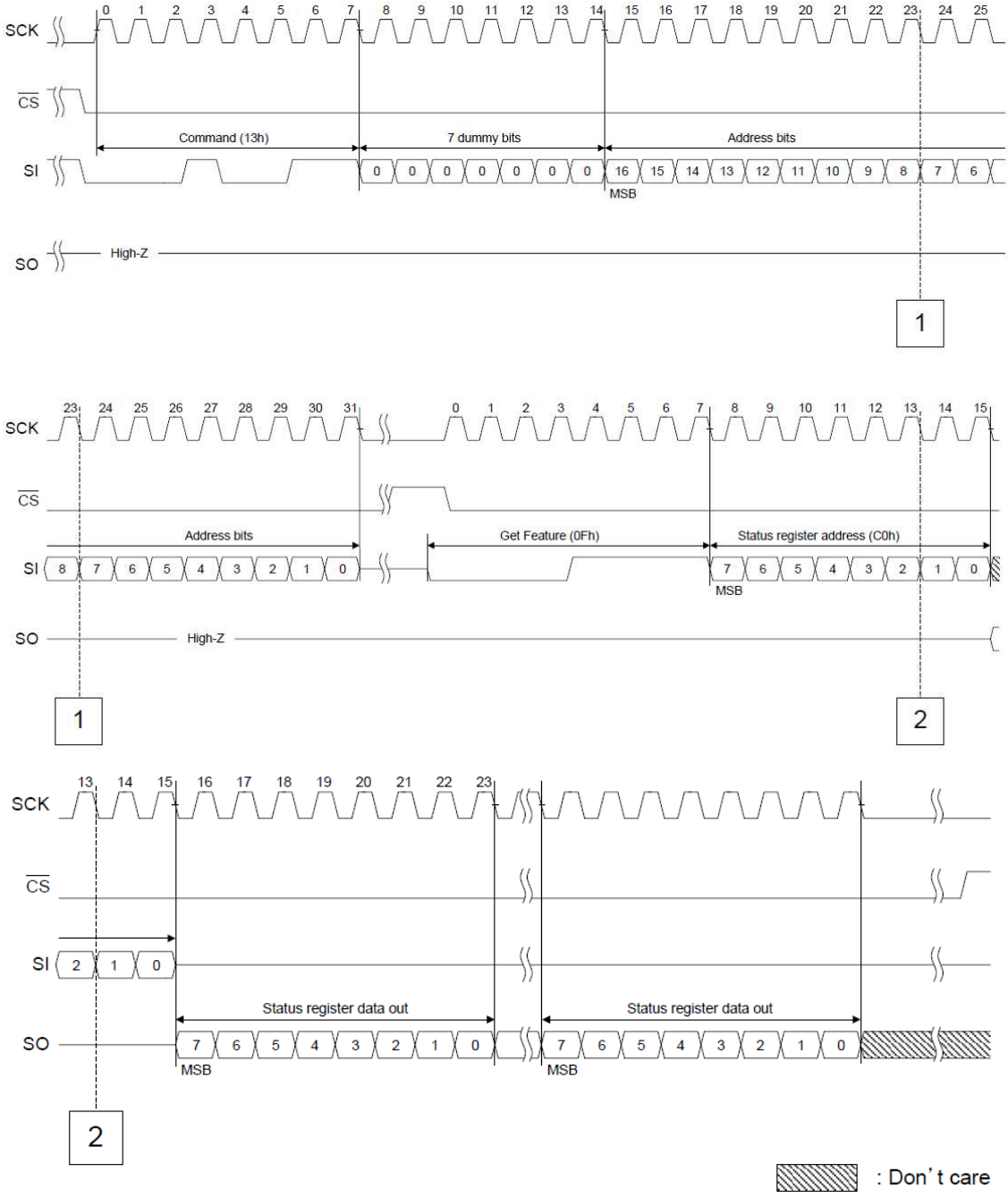
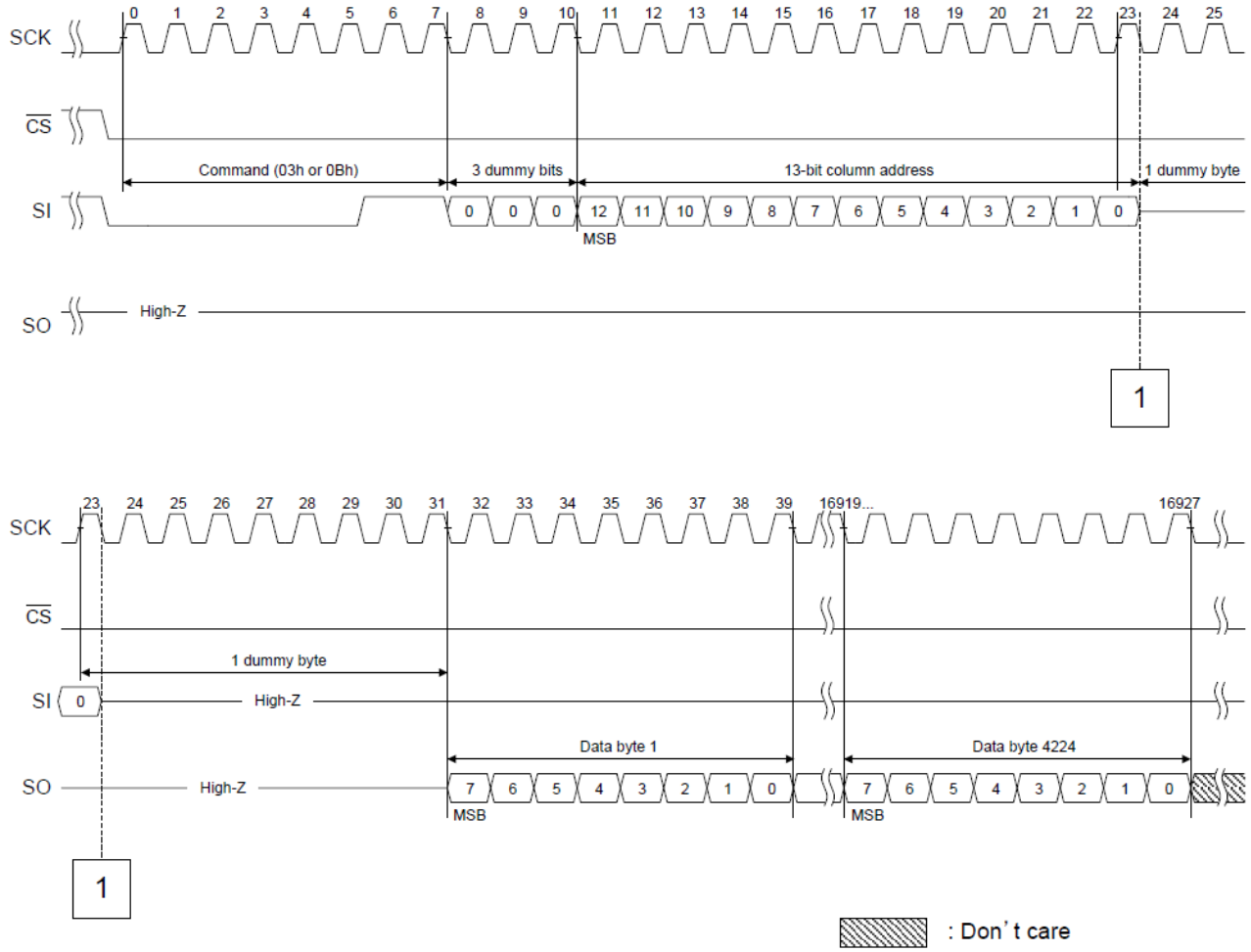


Figure 12. Page Read from Cell Array to Buffer

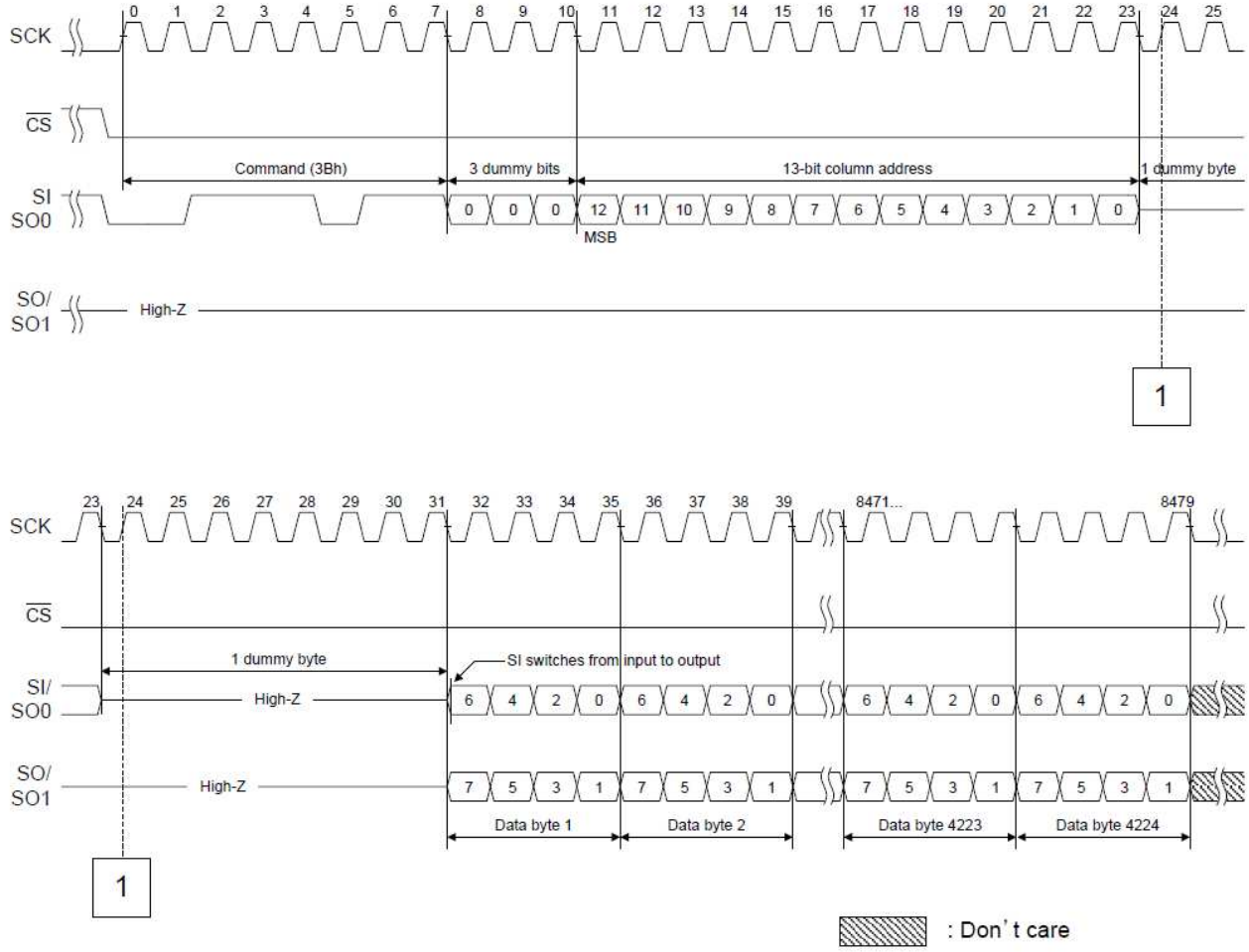
4.2.2. Read Buffer (03h or 0Bh)



Note:
When internal ECC is turned OFF, the maximum output data size is 4352 Bytes.

Figure 13. Page Read from Buffer Timing

4.2.3. Read Buffer x2 (3Bh)



Note:
When internal ECC is turned OFF, the maximum output data size is 4352 Bytes.

Figure 14. Page Read from Buffer x2 Timing

4.2.4. Read Buffer x4 (6Bh)

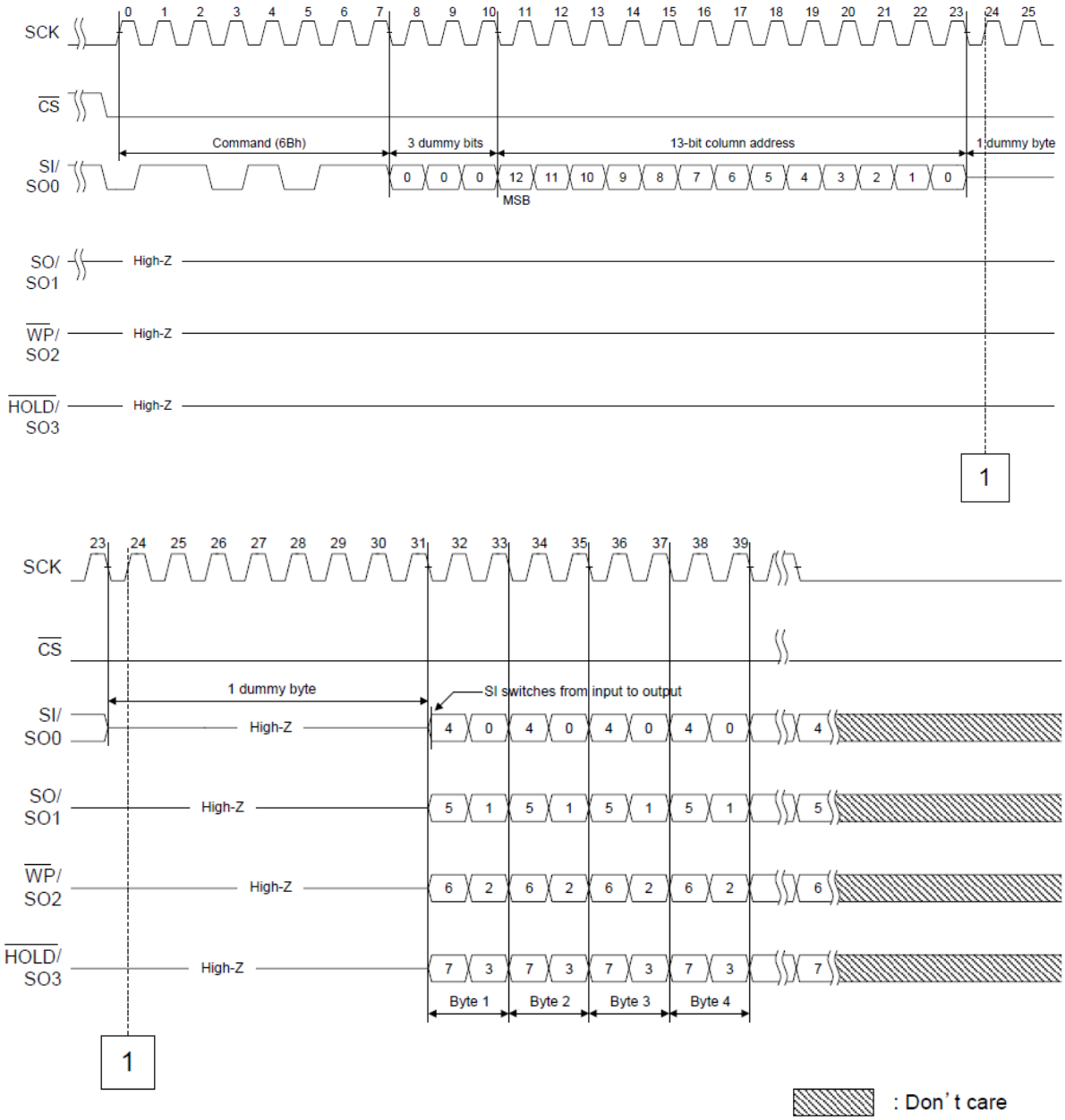


Figure 15. Page Read from Buffer x4 Timing

4.3. Page Read Operation - High Speed Mode

The device has a high speed mode for sequential read operation. When high speed mode is enabled, the average tR is shortened. The command sequence is the same as the Page Read Operation. The users set or clear the HSE bit which enables or disables the high speed mode in the feature table as shown in Table 12. High speed mode is enabled (HSE bit is set to 1) in the default condition. When the users switching the HSE bit, the users have to issue the Set Feature command just before the Read Cell Array (13h) command.

When the users use the random page read, the recommended setting of the HSE bit is 0 (disable) since t_R becomes longer.

4.4. Page Program Operation

The Program Load and Program Execute commands are required to program data to a page. The Program Load command transfers data to the buffer. The unit of data transfer is a byte. The Program Execute command programs data from the buffer to the cell array. The operation sequence is as follows.

1. Write Enable (06h) : To enable the Program Operation.
2. Program Load (02h) : To transfer data to the internal data buffer.
3. Program Execute (10h) : To program data from the buffer to the cell array.
4. Get Feature (0Fh) : To read the status (OIP and PRG_F bits) of the device.

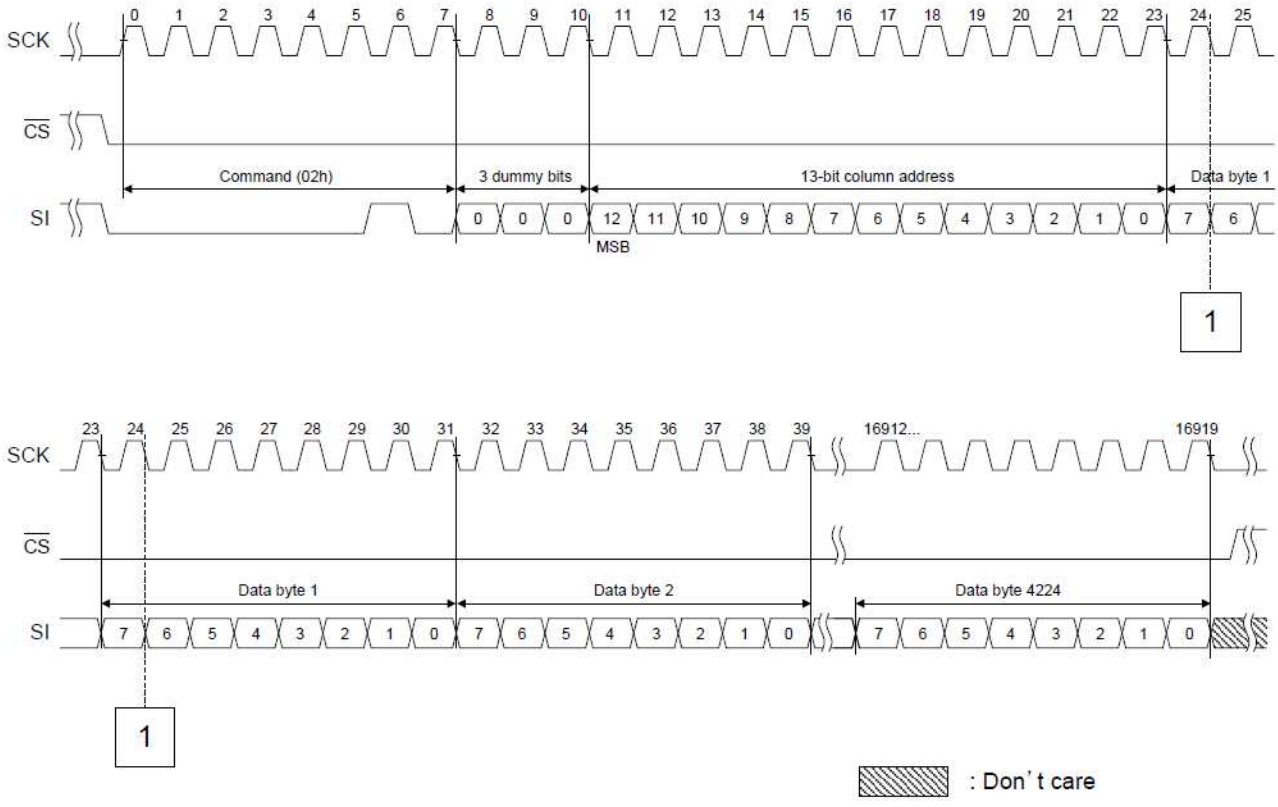
The internal data buffer is cleared by the Program Load command.

The Program Load Random Data (84h) command is also available to transfer data to the internal buffer. The users issue Program Load Random Data and the column address before the program execute (10h). The operation sequence is as follows.

1. Write Enable (06h) : To enable the Program Operation.
2. Program Load (02h) : To transfer data to the internal data buffer.
3. Program Load Random Data (84h) : To transfer data to the internal data buffer.
4. Program Execute (10h) : To program data from the buffer to the cell array.
5. Get Feature (0Fh) : To read the status (OIP and PRG_F bits) of the device.

Program Load Random Data and Get Feature commands are repeatable command.
The internal data buffer is not cleared by the Program Load Random Data command.

4.4.1. Program Load (02h)



Note:
When internal ECC is turned OFF, the maximum input data size is 4352 Bytes.

Figure 16. Program Load

4.4.2. Program Execute (10h)

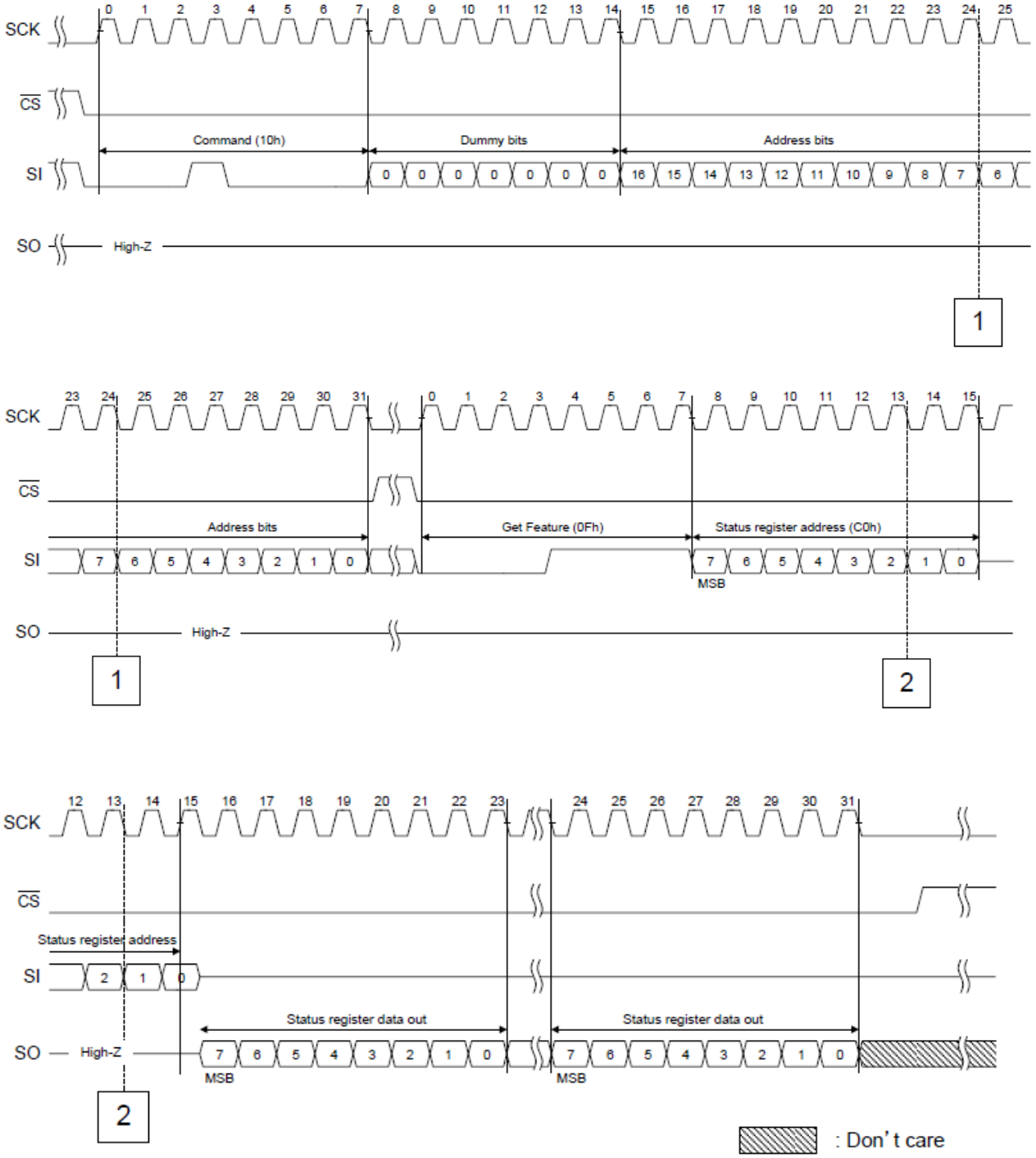
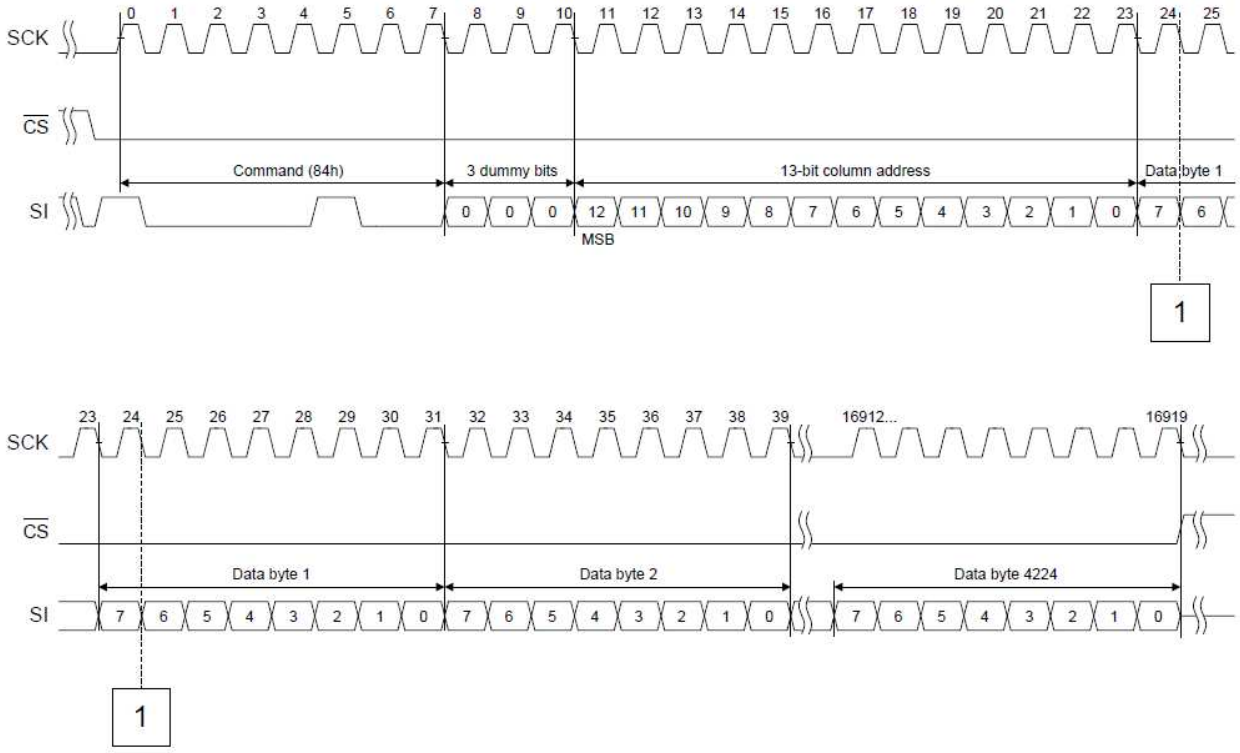


Figure 17. Program Execute Timing

4.4.3. Program Load Random Data (84h)



Note:
When internal ECC is turned OFF, the maximum input data size is 4352 Bytes.

Figure 18. Program Load Random Data Timing

4.5. Internal Data Move Operation

The Internal Data Move Operation is used to change the data in a page without data output. Before using this operation, the users must disable the Page Read High Speed Mode. The operation sequence is as follows.

1. Set Feature (1Fh) : To disable Page Read High Speed Mode.
2. Read Cell Array (13h) : To read data from the cell array to internal buffer.
3. Get Feature (0Fh) : To read the status (OIP, ECCS0 and ECCS1 bits) of the device.
4. Write Enable (06h) : To enable the write.
5. Program Load Random Data (84h) : To change the data in the internal buffer.
6. Program Execute (10h) : To program data from the buffer to the cell array.
7. Get Feature (0Fh) : To read the status (OIP, PRG_F bits) of the device.

Program Load Random Data and Get Feature commands are repeatable command.
The status of the internal ECC depends on ECC_E bit in the feature table. When internal ECC is disabled, bit flips are not managed by the device.

4.6. Block Erase (D8h)

The Block Erase Operation erases the selected block. The page address is ignored automatically.
The operation sequence is as follows.
1. Write Enable (06h) : To enable the Erase Operation.
2. Block Erase (D8h) : To erase data in the block.
3. Get Feature (0Fh) : To read the status (OIP and ERS_F bits) of the device.

Get Feature command is repeatable command.

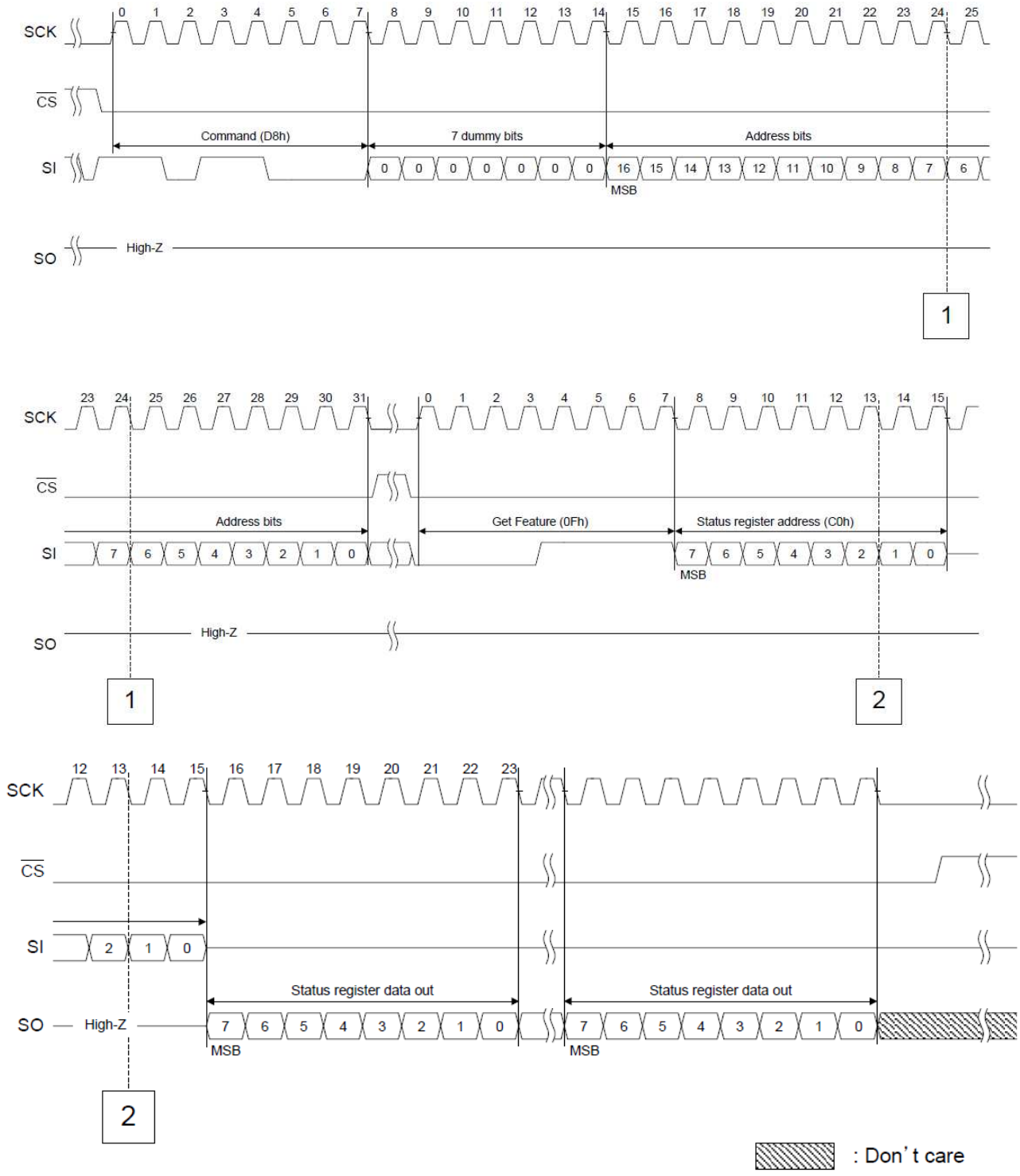


Figure 19. Block Erase Timing

4.7. Reset (FFh or FEh)

The Reset Operation is to reset the operations. For example, in case of a Program or Erase operation, the internally generated voltage is discharged and the device enters the busy state. The operation sequence is as follows.

1. Reset (FFh or FEh) :To reset the device
2. Get Feature (0Fh) :To read the status of the device

Get Feature command is repeatable command.

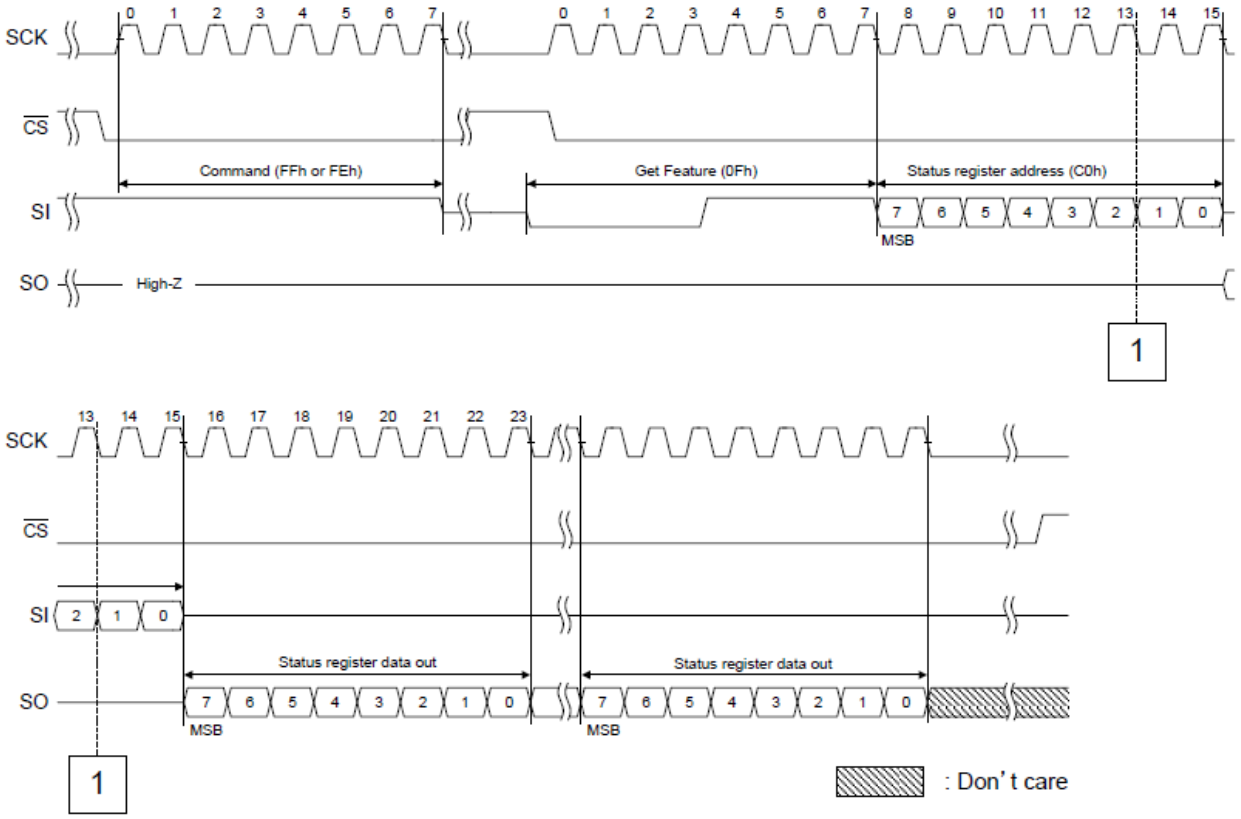


Figure 20. Reset Timing

4.8. Write Enable (06h) / Write Disable (04h)

The Write Enable / Disable commands set or reset the WEL (-Write Enable Latch) bit in the feature table shown in Table 12.

The Write Enable command sets the WEL bit to 1. The Write Enable command must be issued before the Page Program, Block Protection and Block Erase operations. The Write Disable command clears the WEL bit to 0. If the WEL bit is cleared, Page Program, Block Protection and Block Erase commands are ignored by the device.

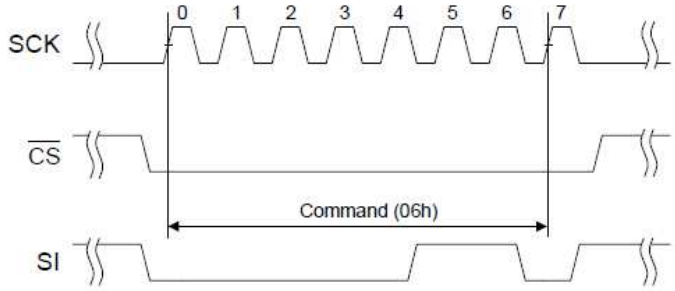


Figure 21. Write Enable

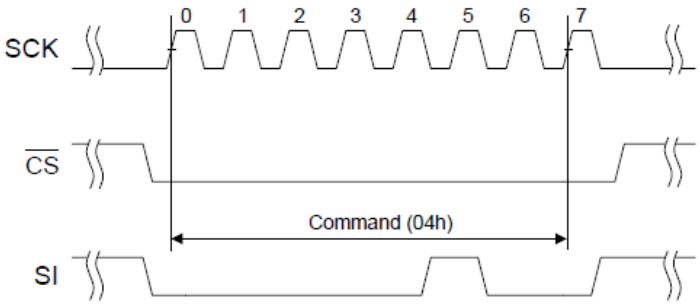


Figure 22. Write Disable Timing