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## Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832

Email & Skype: info@chipsmall.com Web: www.chipsmall.com

Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China



# TOSHIBA

## Serial Interface NAND

### Technical Data Sheet

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TOSHIBA

Storage & Electronic Devices Solutions  
Memory Division

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## 1. Introduction

### 1.1. General Description

The TC58CYG0S3HxAIx is a serial interface NAND Flash for embedded applications which supports the SPI interface.

The TC58CYG0S3HxAIx is organized as (2048 + 64) bytes × 64 pages × 1024 blocks. The device has a 2112 byte data buffer which allows program and read data to be transferred between the buffer and the memory cell array in 2112-byte increments. The Erase Operation is implemented in a single block unit (128 Kbytes + 4 Kbytes: 2112 bytes × 64 pages). The device has the high speed mode for sequential Page Read Operation. When high speed mode is enabled, the average of tR is shortened.

The TC58CYG0S3HxAIx has ECC logic on the chip and 8bit read errors for each (512 bytes + 16 bytes) can be corrected. The internal ECC logic has detailed bit flip count report.

### 1.2. Definitions and Abbreviations

#### **SPI**

Serial Peripheral Interface.

#### **Address**

The address is comprised of a column address (CA) with 12bits and a row address (RA) with 16bits. The row address identifies the page and block to be accessed. The column address identifies the byte within a page to access.

#### **Column**

The byte location within the page.

#### **Row**

Refer to the block and page to be accessed.

#### **Sector**

The 512 bytes unit in a page.

#### **Page**

The smallest addressable unit for the Read and the Program operations.

#### **Block**

Consists of multiple pages and is the smallest addressable unit for the Erase Operation.

#### **Data Buffer**

Buffer used to transfer data to and from the cell array.

#### **Cell Array**

Memory cell of NAND flash

#### **Device**

The packaged NAND unit.

### 1.3. Features

- **Organization**

- Organization (Internal ECC is enabled, default)

Memory Cell Array	2112 × 64 × 1024 × 8 bits
Data Buffer	2112 × 8 bits
Page Size	2112 bytes
Block Size	(128K + 4K) bytes

- Organization (Internal ECC is disabled)

Memory Cell Array	2176 × 64 × 1024 × 8 bits
Data Buffer	2176 × 8 bits
Page Size	2176 bytes
Block Size	(128K + 8K) bytes

- **ECC**

8 bit ECC for each 512bytes is required. The device has ECC logic internally.

- **Mode**

Page Read, Page Program, Block Erase, Internal Data Move, Reset, Write Enable, Write Disable, Block Lock, Get Feature, Set Feature, Block Protection, Parameter Page Read, Read ID, Unique ID Read.

- **Power Supply**

$V_{CC} = 1.7\text{ V to }1.95\text{ V}$

- **Access Time**

Cell Array to Data Buffer	155 $\mu\text{s}$ max
	70 $\mu\text{s}$ typ
Data Transfer rate	104 MHz max

- **Program/Erase Time**

Programming Time	360 $\mu\text{s}$ /page typ
Block Erasing Time	2.7 ms/block typ

- **Operating Current**

Read Operation Current with HSE on (Average)	21 mA max
Read Operation Current with HSE off (Average)	15 mA max
Program Operation Current (Average)	18 mA max
Erase Operation Current (Average)	22 mA max
Standby Current	180 $\mu\text{A}$ max
	35 $\mu\text{A}$ typ

- **Reliability**

Refer to reliability note.

- **Package**

- SOP16 (P-SOP16-1111-1.27-001)
- WSON8 (P-WSON8-0608-1.27-003)

## 2. Memory Organization

### 2.1. Pin Descriptions

Table 1 Pin Descriptions

Pin Name	Pin Function
$\overline{\text{CS}}$	Chip Select
SO/SO1	Serial Data Output / Serial Data Output 1
$\overline{\text{WP}}/\text{SO2}$	Write Protect / Serial Data Output 2
SI/SO0	Serial Data Input / Serial Data Output 0
HOLD/SO3	Hold Input / Serial Data Output 3
SCK	Serial Clock Input
VCC	Power Supply
VSS	Ground

**Note:**

If the WP pin is low and BRWD bit is set to 1, the overwrite for the BRWD(bit [7]) and the BL bits (bits [5:3]) in address A0h of the feature table shown in Table 12 is prohibited.

The users cannot drive the WP pin while CS pin is low.

The HOLD pin and the WP pin are pull up to VCC internally.

### 2.2. Pin Assignment (Top View)

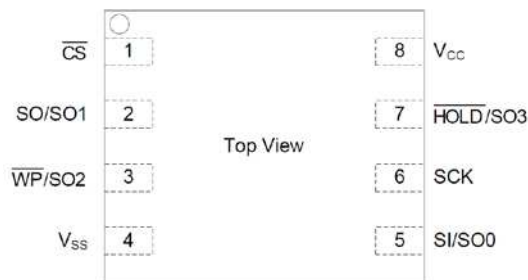


Figure 1. WSON8 Pin Assignment (Top View)

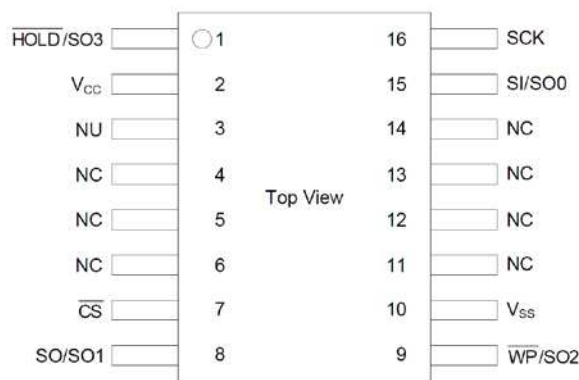


Figure 2. SOP16 Pin Assignment (Top View)



**2.3. Block Diagram**

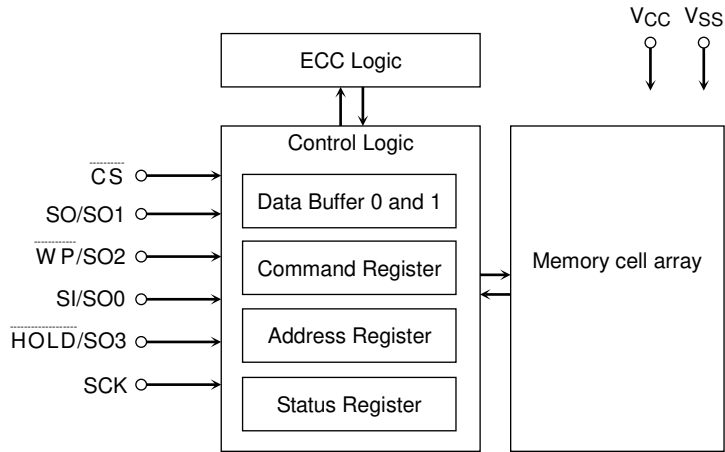


Figure 3. Block Diagram

**2.4. Cell Layout**

The Program Operation works on page units while the Erase Operation works on block units. In the case that internal ECC is turned ON the default setting, a page consists of 2112 bytes in which 2048 bytes are used for main memory storage and 64 bytes are used for redundancy or for other uses. In the case that internal ECC is turned OFF, the redundancy area will be expanded to 128 bytes automatically.

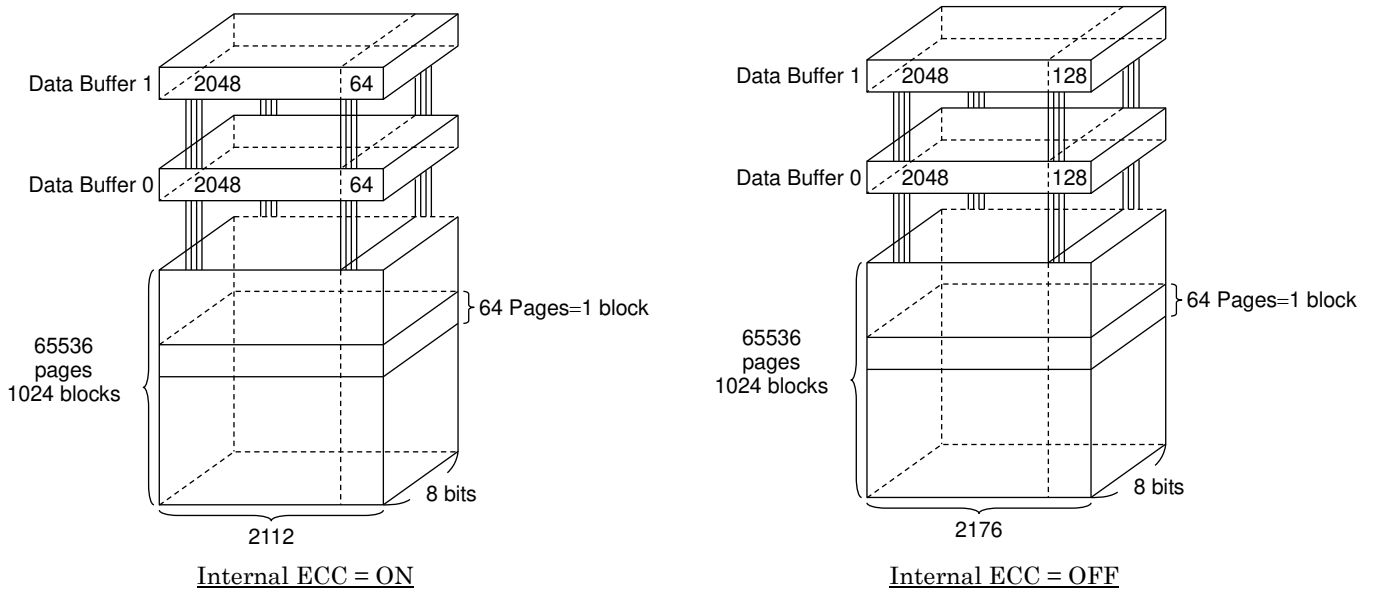
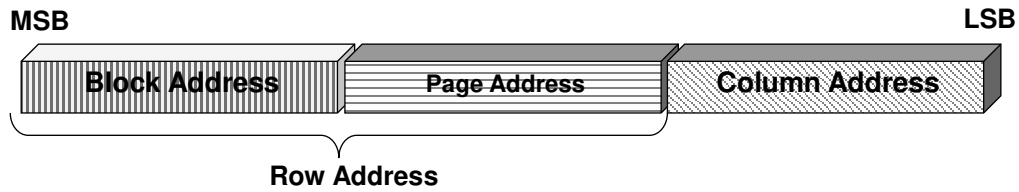


Figure 4. Cell Layout

## 2.5. Addressing

There are two address types used: the column address and the row address. The column address is used to access bytes within a page. The row address is used to address pages and blocks. There are some functions that may require only row addresses, such as Block Erase.



Row Address: 16 bits

Block Address (1024 blocks/device): 10 bits

Page Address (64 pages/block): 6 bits

Column Address: 12 bits

Column Address (2112 or 2176 bytes/page): 12 bits

Figure 5. Addressing

## 2.6. Valid Blocks

Table 2 Valid Blocks

Symbol	Parameter	Min.	Typ.	Max.	Unit
N <sub>VB</sub>	Number of Valid Blocks	1004	-	1024	Block

**Note:**

The device occasionally contains unusable blocks.

The first block (Block 0) is guaranteed to be a valid block at the time of shipment.

The specification for the minimum number of valid blocks is applicable over the lifetime

### 3. Physical Interface

#### 3.1. Absolute Maximum Rating

Stresses greater than those listed in Table 3 may cause permanent damage to the device. This is a stress rating only.

Table 3 Absolute Maximum Rating

Symbol	Parameter	Value	Unit
V <sub>CC</sub>	Power Supply Voltage	-0.3 to 3.9	V
V <sub>IN</sub>	Input Voltage	-0.3 to V <sub>CC</sub> + 0.3 (≤ 3.9 V)	V
V <sub>I/O</sub>	Input /Output Voltage	-0.3 to V <sub>CC</sub> + 0.3 (≤ 3.9 V)	V
PD1	Power Dissipation 1	0.42	W
PD2	Power Dissipation 2 (WSON8 ePAD without solder)	0.27	W
T <sub>SOLDER</sub>	Soldering Temperature (10 s)	260	°C
T <sub>STG</sub>	Storage Temperature	-55 to 150	°C
T <sub>OPR</sub>	Operating Temperature	-40 to 85	°C

#### 3.2. Capacitance

Table 4 Capacitance (T<sub>OPR</sub> = 25°C, f = 1MHz)

Symbol	Parameter	Condition	Min.	Max.	Unit
C <sub>IN</sub>	Input	V <sub>IN</sub> = 0 V	-	2.5	pF
C <sub>OUT</sub>	Output	V <sub>OUT</sub> = 0 V	-	4	pF

**Note:** This parameter is periodically sampled and is not tested for every device.

#### 3.3. Recommended DC Operating Conditions

Table 5 Recommended DC Operating Condition

Symbol	Parameter	Min.	Typ.	Max.	Unit
V <sub>CC</sub>	Power Supply Voltage	1.7	-	1.95	V
V <sub>IH</sub>	High Level input Voltage	V <sub>CC</sub> × 0.8	-	V <sub>CC</sub> + 0.3	V
V <sub>IL</sub>	Low Level Input Voltage	-0.3	-	V <sub>CC</sub> × 0.2	V

**3.4. Signal Timing**

The device supports SPI mode 0 and mode 3. Input data is latched at the rising edge of SCK and data is output at the falling edge of SCK for mode 0 and 3. When HOLD goes Low, the communication is held. The hold state begins the falling edge of SCK.

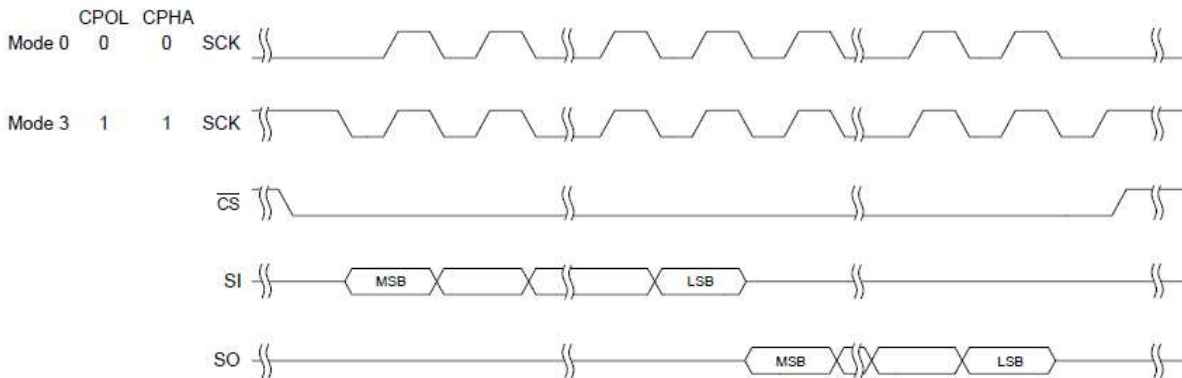


Figure 6. SPI Timing

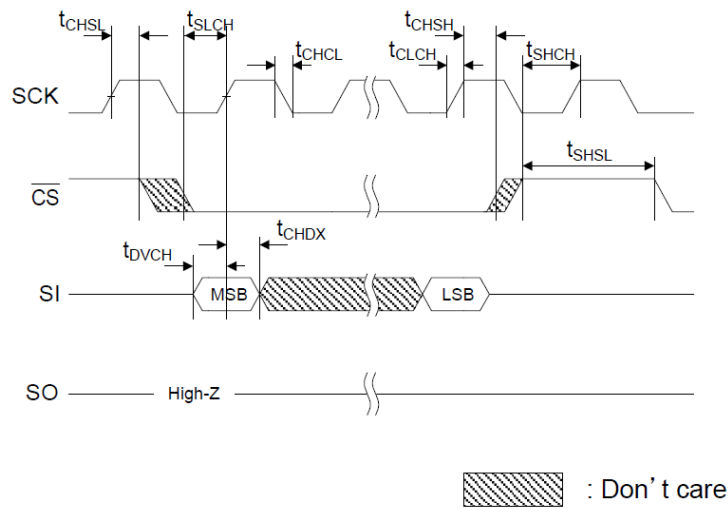


Figure 7. Serial Input Timing

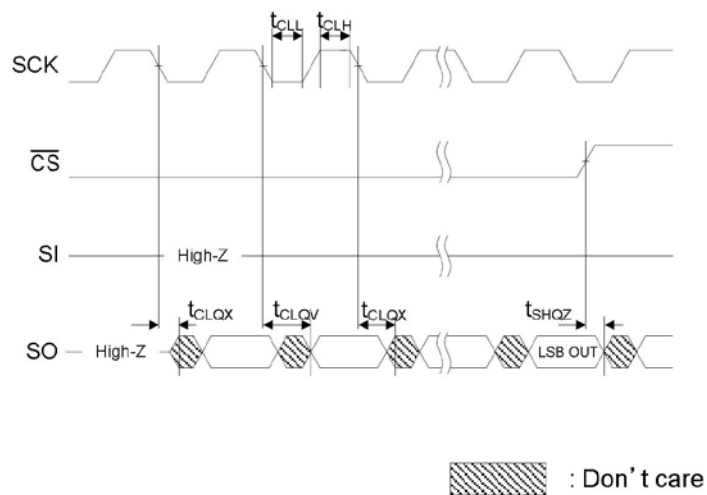


Figure 8. Serial Output Timing

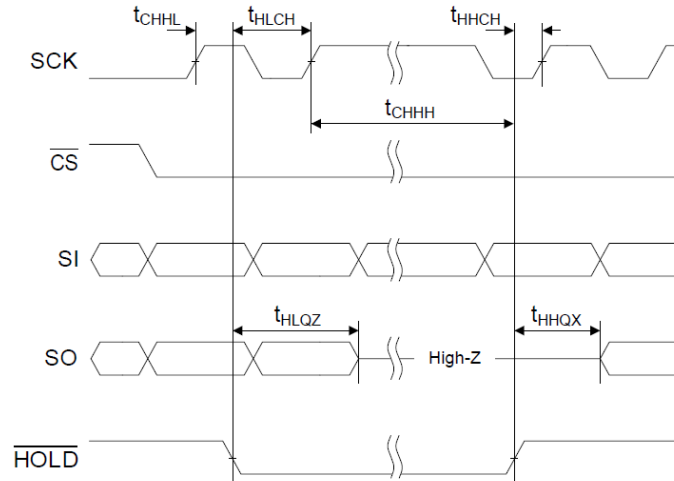


Figure 9. Hold Timing

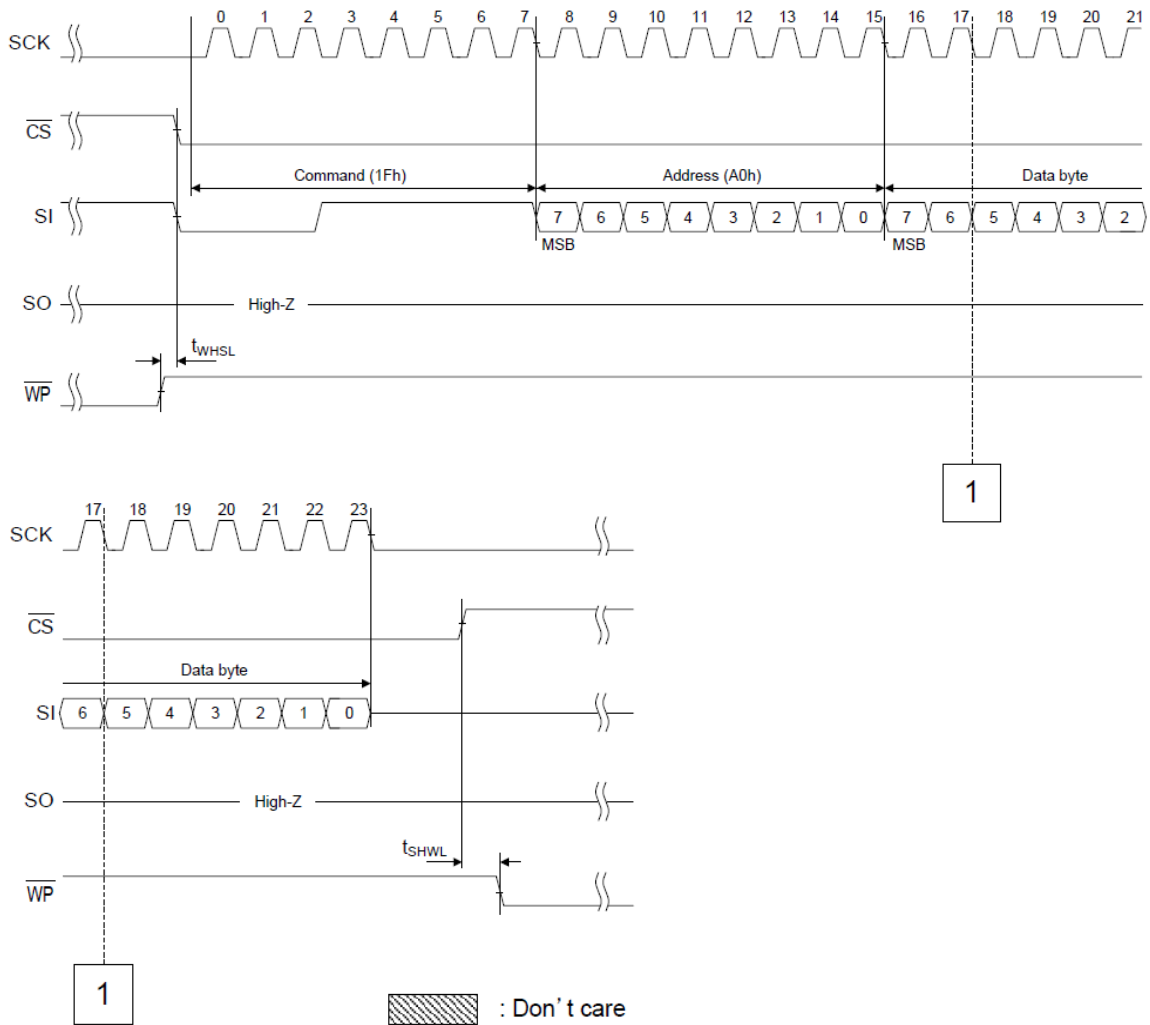


Figure 10. WP Timing (Example)

### 3.5. AC Characteristics

Table 6 AC Characteristics ( $T_{OPR} = -40$  to  $85^{\circ}\text{C}$ ,  $V_{CC} = 1.7$  to  $1.95\text{V}$ )

Symbol	Parameter	Min.	Typ.	Max.	Unit
$F_C$	Serial Clock Frequency For: all command	-	-	104	MHz
$t_{CLH}$	Serial Clock High Time	4.5	-	-	ns
$t_{CLL}$	Serial Clock Low Time	4.5	-	-	ns
$t_{CLCH}$	Serial Clock Rise Time (Slew Rate)	0.1	-	-	V/ns
$t_{CHCL}$	Serial Clock Fall Time (Slew Rate)	0.1	-	-	V/ns
$t_{SLCH}$	CS# Active Setup Time	4.6	-	-	ns
$t_{CHSH}$	CS# Active Hold Time	5	-	-	ns
$t_{SHCH}$	CS# Not Active Setup Time	5	-	-	ns
$t_{CHSL}$	CS# Not Active Hold Time	5	-	-	ns
$t_{SHSL} / t_{CS}$	CS# High Time	100	-	-	ns
$t_{SHOZ}$	Output Disable Time	-	-	20	ns
$t_{CLOX}$	Output Hold Time	1	-	-	ns
$t_{DVCH}$	Data In Setup Time	2	-	-	ns
$t_{CHDX}$	Data In Hold Time	5	-	-	ns
$t_{HLCH}$	Hold# Low Setup Time (relative to Clock)	5	-	-	ns
$t_{HHCH}$	Hold# High Setup Time (relative to Clock)	5	-	-	ns
$t_{CHHL}$	Hold# High Hold Time (relative to Clock)	5	-	-	ns
$t_{CHHH}$	Hold# Low Hold Time (relative to Clock)	5	-	-	ns
$t_{HLQZ}$	Hold# Low To High-Z Output	-	-	7	ns
$t_{HHQX}$	Hold# High To Output	-	-	7	ns
$t_{CLOV}$	Clock Low To Output Valid	-	-	7.0(CL=10pF) 7.5(CL=20pF) 8.0(CL=30pF)	ns
$t_{WHSL}$	WP# Setup Time Before CS# Low	20	-	-	ns
$t_{SHWL}$	WP# Hold Time After CS# High	100	-	-	ns

### 3.6. DC Operating Characteristics

Table 7 DC & Operating Characteristics ( $T_{OPR} = -40$  to  $85^{\circ}\text{C}$ ,  $V_{CC} = 1.7$  to  $1.95\text{V}$ )

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
$I_{IL}$	Input Leakage Current	$V_{IN} = 0\text{V to }V_{CC}$	-	-	$\pm 10$	$\mu\text{A}$
$I_{LO}$	Output Leakage Current	$V_{OUT} = 0\text{V to }V_{CC}$	-	-	$\pm 10$	$\mu\text{A}$
$I_{CCOA1}$	Read Operation Current (Average)	$F_C = 104\text{MHz}$ High Speed Mode = Enable Read Buffer Command : 03h or 0Bh (x1)	-	-	21	mA
$I_{CCOA2}$	Read Operation Current (Average)	$F_C = 104\text{MHz}$ High Speed Mode = Disable Read Buffer Command : 03h or 0Bh (x1)	-	-	15	mA
$I_{CCOA3}$	Program Operation Current (Average)	$F_C = 104\text{MHz}$	-	-	18	mA
$I_{CCOA4}$	Erase Operation Current (Average)	$F_C = 104\text{MHz}$	-	-	22	mA
$I_{CCS}$	Standby Current	$\overline{CS} = V_{CC} - 0.2\text{V}$ , $\overline{WP} = V_{CC}$ , $\overline{HOLD} = V_{CC}$	-	35	180	$\mu\text{A}$
$V_{OH}$	High Level Output Voltage	$I_{OH} = -0.1\text{mA}$	$V_{CC}-0.2$	-	-	V
$V_{OL}$	Low Level Output Voltage	$I_{OL} = 0.1\text{mA}$	-	-	0.2	V

**Note:**

Refer to the High Speed Mode in 4.3.

ICCOA1~ICCOA4 are the average current during the full operation sequence.

### 3.7. Programming, Reading and Erasing Characteristics

Table 8 Programming, Reading and Erasing Characteristics (T<sub>OPR</sub> = -40 to 85°C, V<sub>CC</sub> = 1.7 to 1.95V)

Symbol	Parameter	Min.	Typ.	Max.	Unit
t <sub>PROG</sub>	Programming Time	-	360	500	μs
N	Number of Partial Program Cycles in the Same Page	-	-	4	time
t <sub>BERASE</sub>	Block Erasing Time	-	2.7	10	ms
t <sub>R</sub>	Cell Array to the Buffer (with ECC) (High Speed Mode = Disable)	-	70	155	μs
t <sub>RHSA4</sub>	Average Read Time for Sequential Read (High Speed Mode = Enable, Read Buffer x4)	-	30	-	μs
t <sub>RST</sub>	Device Reset Time (Read)	-	-	155	μs
	Device Reset Time (Program)	-	-	500	μs
	Device Reset Time (Erase)	-	-	10	ms

**Note:**

Refer to the data pair of ECC calculation in 4.16 Internal ECC.

Refer to the High Speed Mode in 4.3.

t<sub>R</sub> is the average busy time for page read operation of 64pages continuously in a block.

t<sub>RHSA4</sub> is the average busy time for sequential page read operation with all data output in each page of 64pages continuously in a block.

The busy time after Protect Execute command is shorter than t<sub>PROG</sub> (Max.).

### 3.8. Power ON/OFF Sequence

The timing sequence shown in the figure below is necessary for the power ON/OFF sequence.

The device internal initialization starts after the power supply reaches an appropriate level in the power on sequence. The users cannot issue any commands while t<sub>vSL</sub>. From the end of t<sub>vSL</sub> to the end of t<sub>vOP</sub>, Get Feature Operation and Reset Operation can be issued. OIP bit in the feature table indicates the busy state in this time period. All operations are available after t<sub>vOP</sub>.

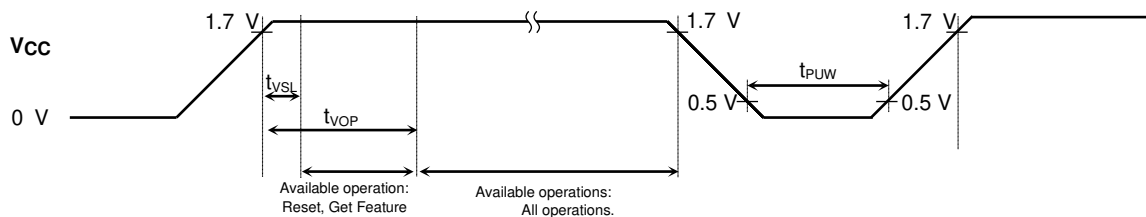


Figure 11. Power ON/OFF Sequence

Table 9 Power on Timing

Symbol	Parameter	Min.	Max.	Unit
t <sub>vSL</sub>	V <sub>CC</sub> (min) to CS Low	-	100	μs
t <sub>vOP</sub>	V <sub>CC</sub> (min) to all operation	-	1.1	ms
t <sub>PUW</sub>	Waiting time for power on	1	-	ms
V <sub>CCSR</sub>	V <sub>CC</sub> Slew Rate	-	136	mV/μs

### 3.9. AC Test Condition

Table 10 AC Test Condition

PARAMETER	CONDITION
	V <sub>CC</sub> : 1.7 to 1.95V
Input level	V <sub>CC</sub> × 0.2 to V <sub>CC</sub> × 0.8
Input pulse rise and fall time	2 ns
Input comparison level	V <sub>CC</sub> / 2
Output data comparison level	V <sub>CC</sub> / 2
Output load	C <sub>L</sub> (30pF) + 1 TTL

## 4. Command Description and Device Operation

### 4.1. Command Set

Table 11 Command Set

Operation	Byte 1 (CMD)	Byte 2	Byte 3	Byte 4	Byte 5	Byte N
Read Cell Array	13h	Dummy	A15-A8 (Input)	A7-A0 (Input)	-	-
Read Buffer	03h/0Bh	Dummy + A11-A8 (Input)	A7-A0 (Input)	Dummy	D*-D* (Output)	D*-D* (Output)
Read Buffer x2	3Bh	Dummy + A11-A8 (Input)	A7-A0 (Input)	Dummy	D*-D* (Output)	D*-D* (Output)
Read Buffer x4	6Bh	Dummy + A11-A8 (Input)	A7-A0 (Input)	Dummy	D*-D* (Output)	D*-D* (Output)
Program Load	02h	Dummy + A11-A8 (Input)	A7-A0 (Input)	D*-D* (Input)	D*-D* (Input)	D*-D* (Input)
Program Execute	10h	Dummy	A15-A8 (Input)	A7-A0 (Input)	-	-
Protect Execute	2Ah	Dummy	A15-A8 (Input)	A7-A0 (Input)	-	-
Program Load Random Data	84h	Dummy + A11-A8 (Input)	A7-A0 (Input)	D*-D* (Input)	D*-D* (Input)	D*-D* (Input)
Block Erase	D8h	Dummy	A15-A8 (Input)	A7-A0 (Input)	-	-
Reset	FFh/FEh	-	-	-	-	-
Write Enable	06h	-	-	-	-	-
Write Disable	04h	-	-	-	-	-
Get Feature	0Fh	A7-A0 (Input)	D7-D0 (Output)	D7-D0 (Output)	D7-D0 (Output)	D7-D0 (Output)
Set Feature	1Fh	A7-A0 (Input)	D7-D0 (Input)	-	-	-
Read ID	9Fh	Dummy	ID (Output)	ID (Output)	-	-

**Note:**

- 1) Input of a command other than those specified in Table 11 is prohibited. Stored data may be corrupted if an unknown command is entered during the command cycle.
- 2) During the operation in progress, do not input any command except 0Fh, FFh and FEh.
- 3) The user can issue the Protect Execute (2Ah) only one time for each block.
- 4) Once the Get Feature command is issued, the status and setting information are outputted continuously.



### 4.2. Page Read Operation

The Read Cell Array and Read Buffer commands are required to read the data in a page. The Read Cell Array command reads the page data from the NAND cell array to the data buffer. The Read Buffer command reads the data from the data buffer. The operation sequence is as follows.

1. Read Cell Array (13h) : To read the data from the cell array to the internal data buffer.
2. Get Feature (0Fh) : To read the status (OIP, ECCS0 and ECCS1 bits) of the device.
3. Read Buffer (03h or 0Bh) : To output the data from the internal data buffer.  
 or Read Buffer x2 (3Bh)  
 or Read Buffer x4 (6Bh)

Read Buffer, Read Buffer x2, Read Buffer x4 and Get Feature commands are repeatable commands.

For the Read Buffer x2 and Read Buffer x4 read modes are available as shown in Figure 14 and Figure 15.

The users are able to check the detailed bit flip count using ECC Bit Flip Count Detection and other functions using Get Feature command.

#### 4.2.1. Read Cell Array (13h)

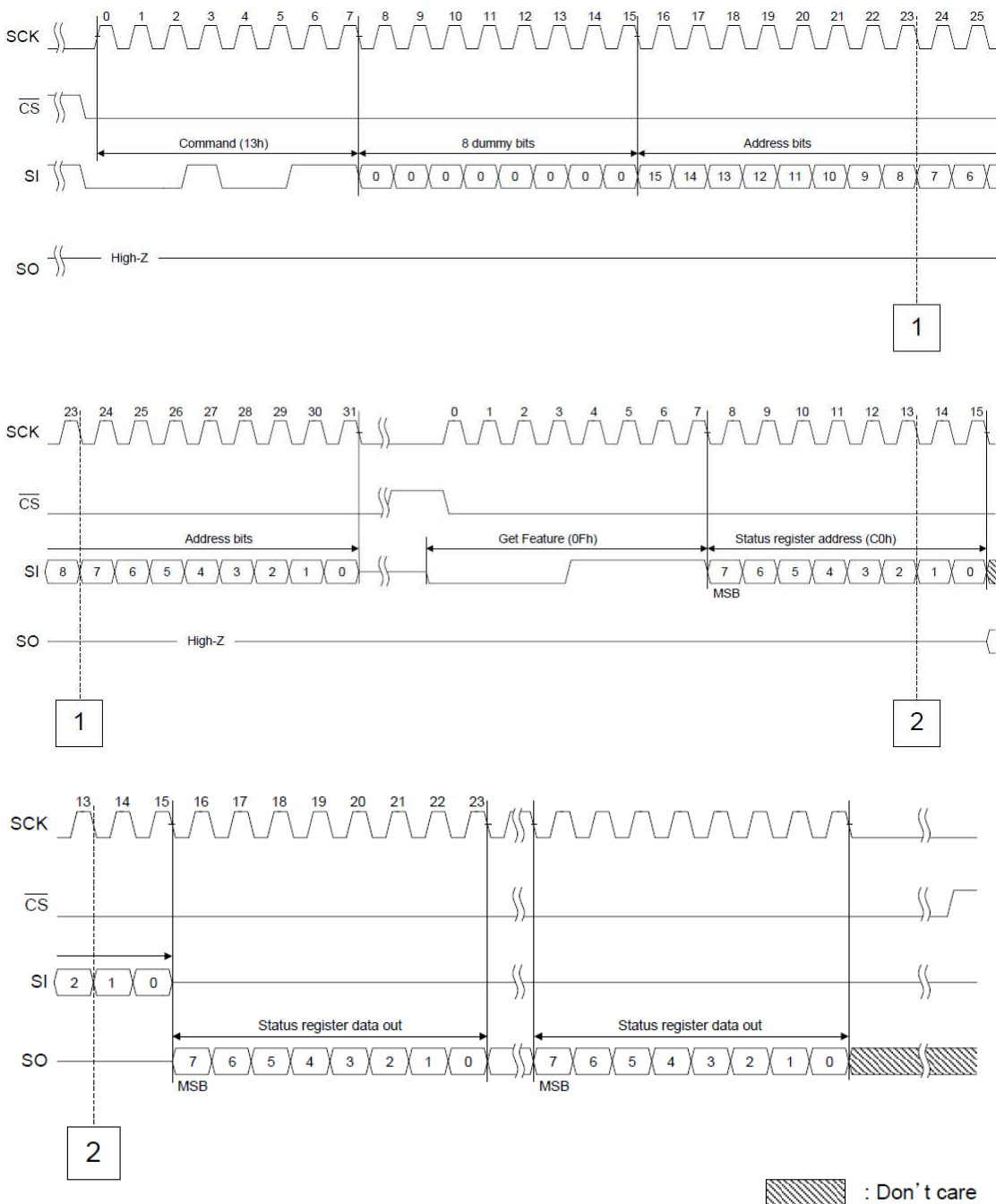
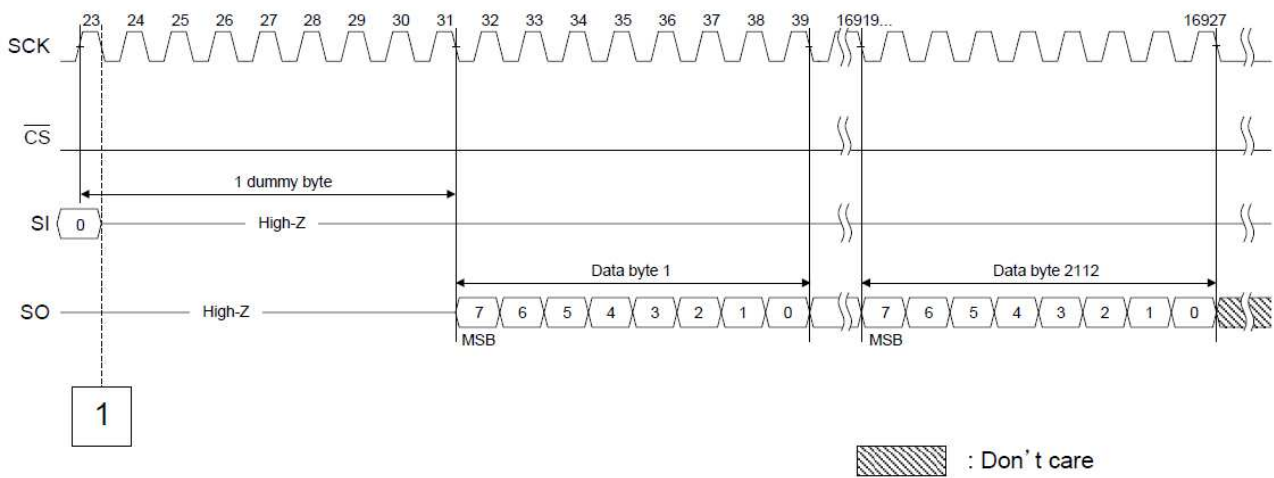
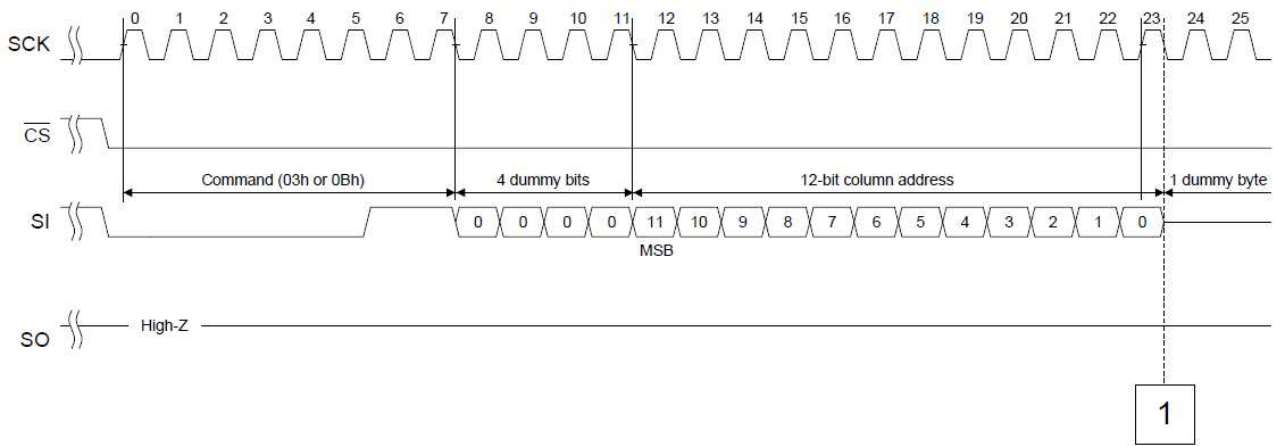


Figure 12. Page Read from Cell Array to Buffer

**4.2.2. Read Buffer (03h or 0Bh)**

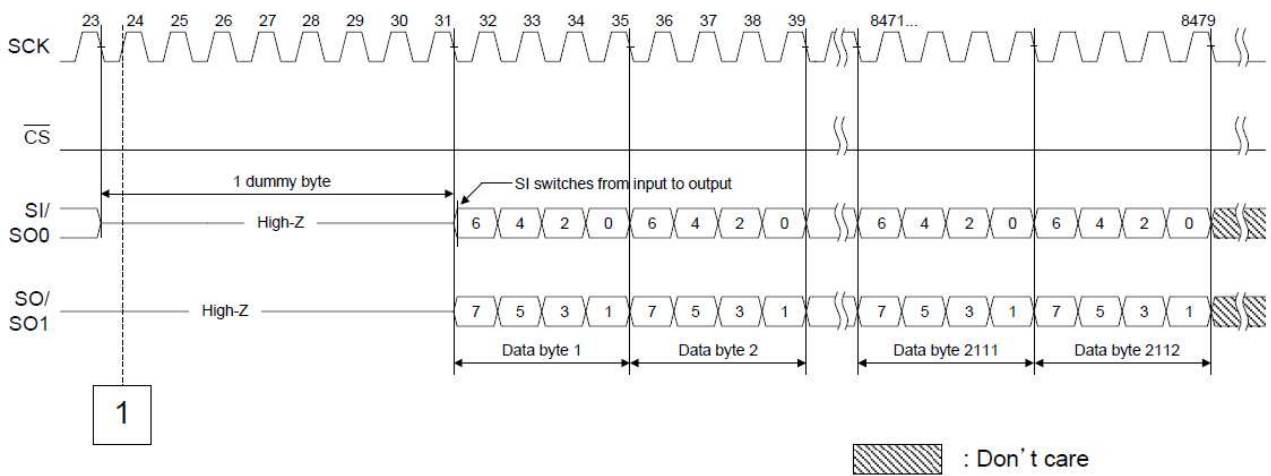
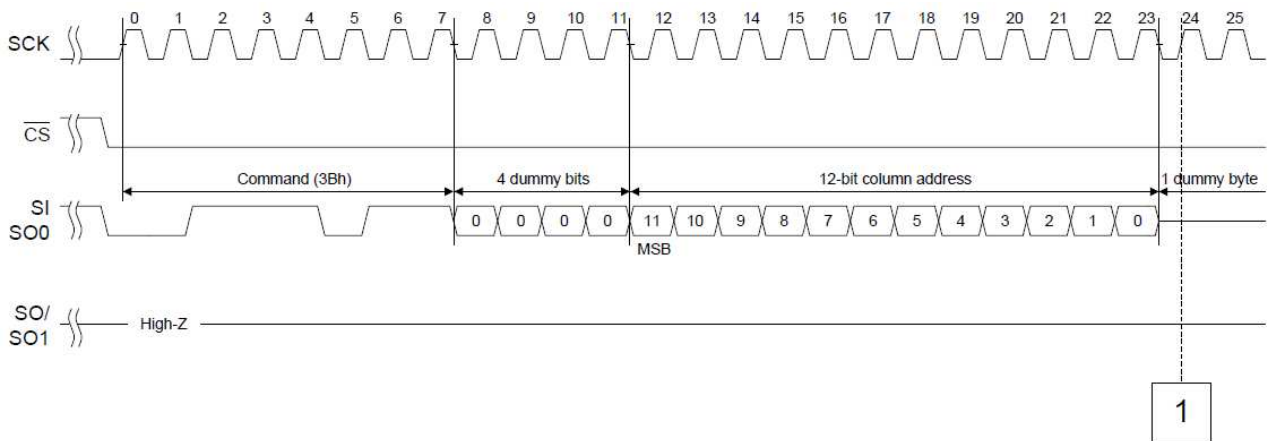


**Note:**

When internal ECC is turned OFF, the maximum output data size is 2176 Bytes.

Figure 13. Page Read from Buffer Timing

**4.2.3. Read Buffer x2 (3Bh)**



**Note:**

When internal ECC is turned OFF, the maximum output data size is 2176 Bytes.

Figure 14. Page Read from Buffer x2 Timing

4.2.4. Read Buffer x4 (6Bh)

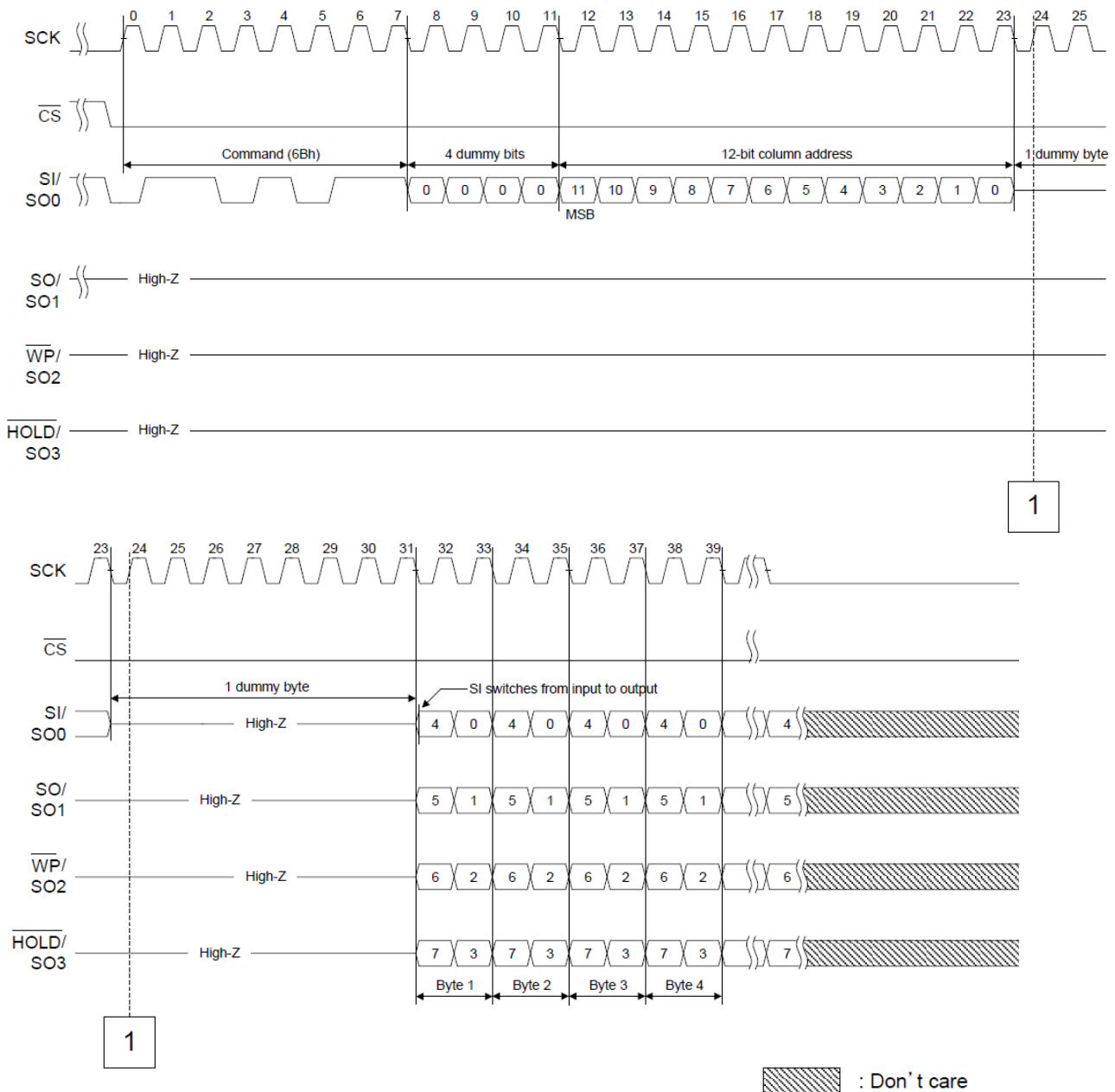


Figure 15. Page Read from Buffer x4 Timing

4.3. Page Read Operation - High Speed Mode

The device has a high speed mode for sequential read operation. When high speed mode is enabled, the average  $t_R$  is shortened. The command sequence is the same as the Page Read Operation. The users set or clear the HSE bit which enables or disables the high speed mode in the feature table as shown in Table 12. High speed mode is enabled (HSE bit is set to 1) in the default condition. When the users switching the HSE bit, the users have to issue the Set Feature command just before the Read Cell Array (13h) command. When the users use the random page read, the recommended setting of the HSE bit is 0 (disable) since  $t_R$  becomes longer.

**4.4. Page Program Operation**

The Program Load and Program Execute commands are required to program data to a page. The Program Load command transfers data to the buffer. The unit of data transfer is a byte. The Program Execute command programs data from the buffer to the cell array. The operation sequence is as follows.

1. Write Enable (06h) : To enable the Program Operation.
2. Program Load (02h) : To transfer data to the internal data buffer.
3. Program Execute (10h) : To program data from the buffer to the cell array.
4. Get Feature (0Fh) : To read the status (OIP and PRG\_F bits) of the device.

The internal data buffer is cleared by the Program Load command.

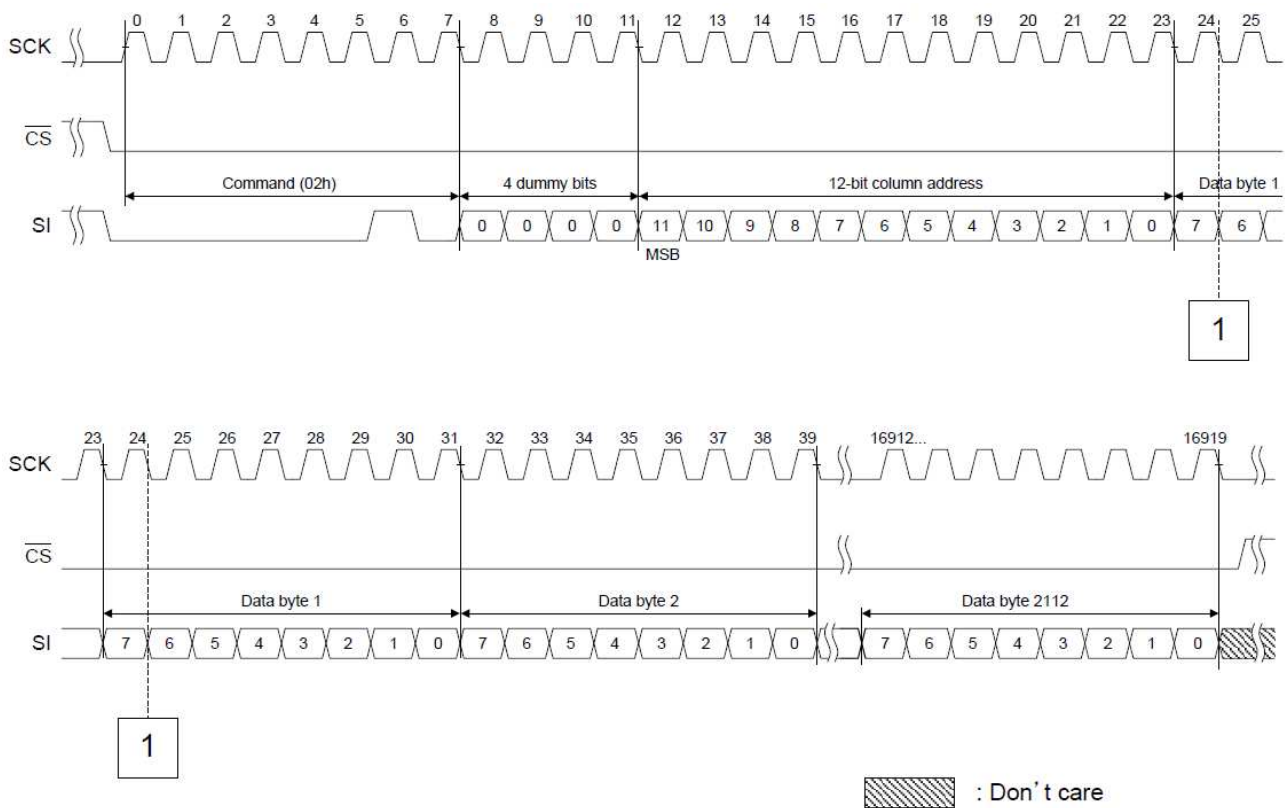
The Program Load Random Data (84h) command is also available to transfer data to the internal buffer. The users issue Program Load Random Data and the column address before the program execute (10h). The operation sequence is as follows.

1. Write Enable (06h) : To enable the Program Operation.
2. Program Load (02h) : To transfer data to the internal data buffer.
3. Program Load Random Data (84h) : To transfer data to the internal data buffer.
4. Program Execute (10h) : To program data from the buffer to the cell array.
5. Get Feature (0Fh) : To read the status (OIP and PRG\_F bits) of the device.

Program Load Random Data and Get Feature commands are repeatable command.

The internal data buffer is not cleared by the Program Load Random Data command.

**4.4.1. Program Load (02h)**



**Note:**

When internal ECC is turned OFF, the maximum input data size is 2176 Bytes.

Figure 16. Program Load

**4.4.2. Program Execute (10h)**

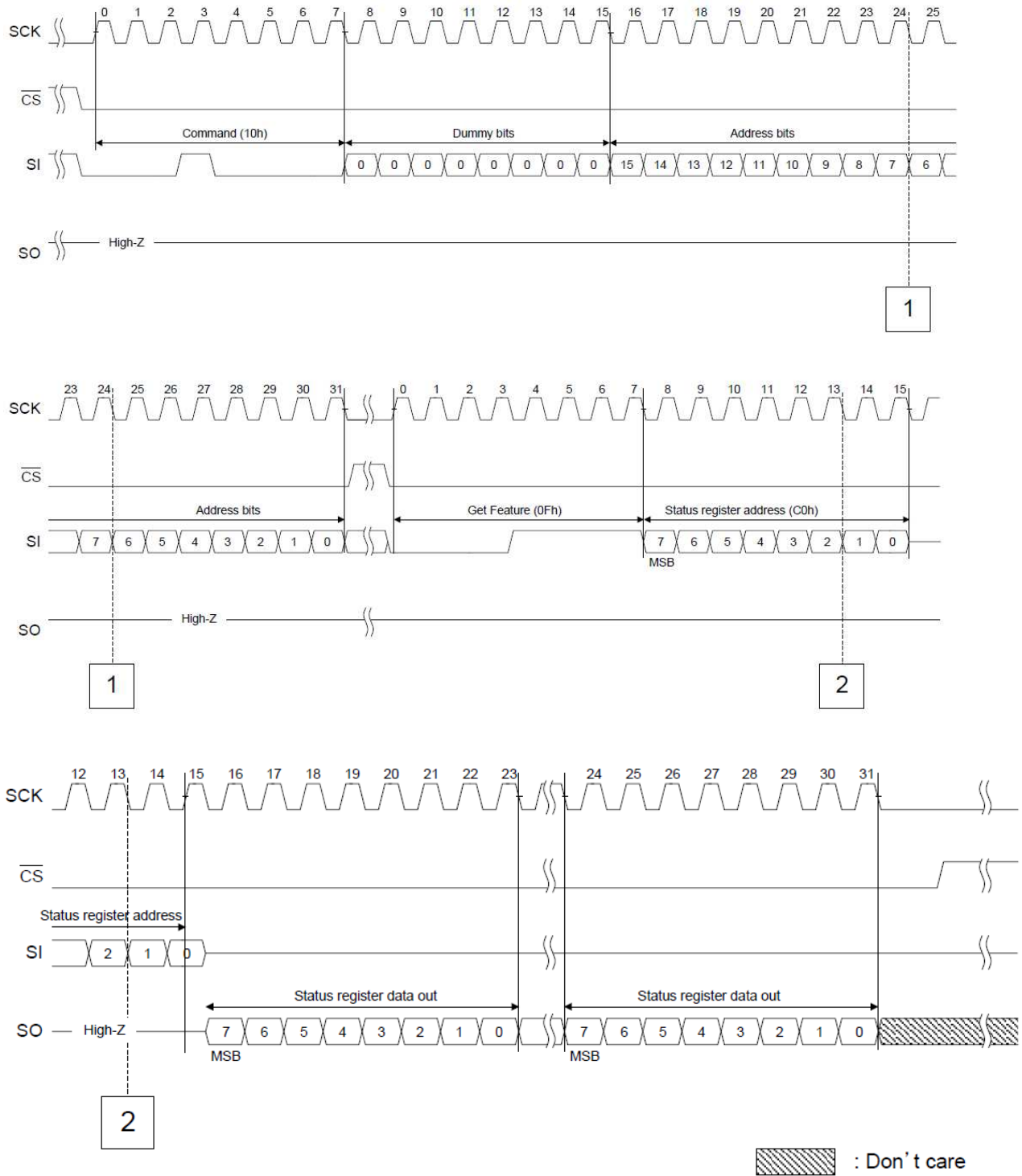
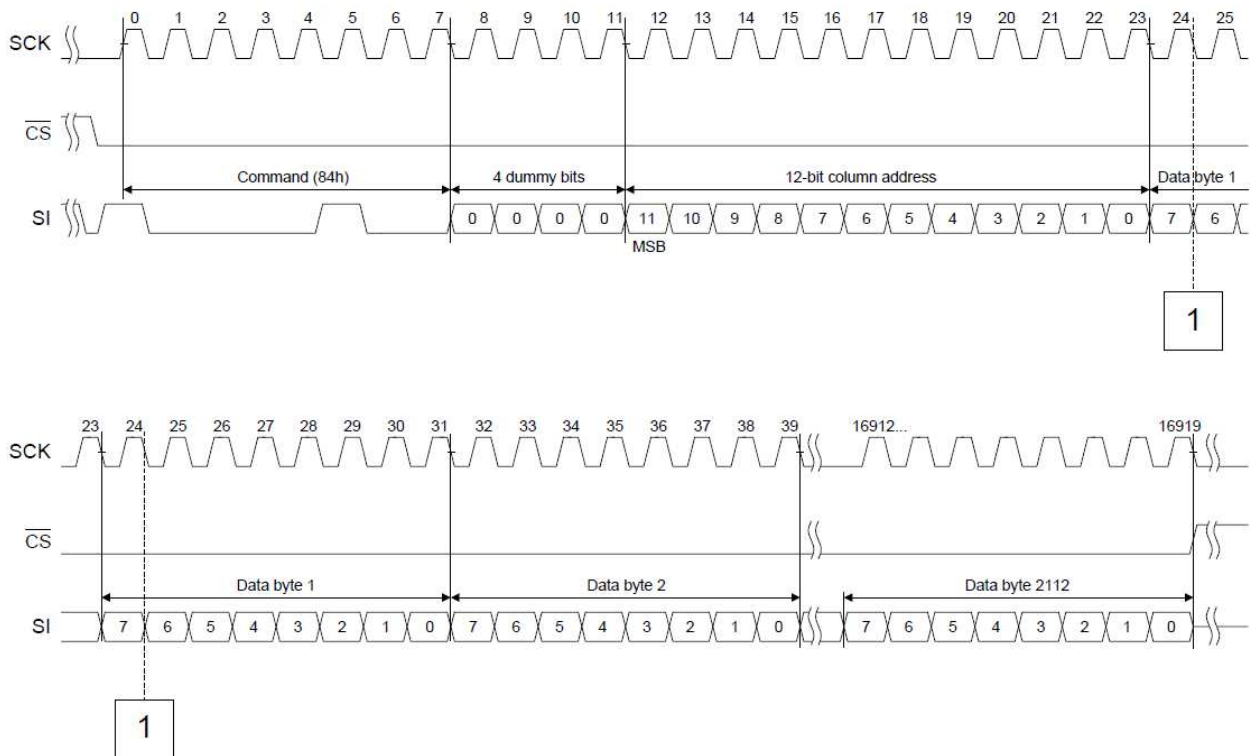


Figure 17. Program Execute Timing

**4.4.3. Program Load Random Data (84h)**



**Note:**

When internal ECC is turned OFF, the maximum input data size is 2176 Bytes.

Figure 18. Program Load Random Data Timing

**4.5. Internal Data Move Operation**

The Internal Data Move Operation is used to change the data in a page without data output. Before using this operation, the users must disable the Page Read High Speed Mode. The operation sequence is as follows.

1. Set Feature (1Fh) : To disable Page Read High Speed Mode.
2. Read Cell Array (13h) : To read data from the cell array to internal buffer.
3. Get Feature (0Fh) : To read the status (OIP, ECCS0 and ECCS1 bits) of the device.
4. Write Enable (06h) : To enable the write.
5. Program Load Random Data (84h) : To change the data in the internal buffer.
6. Program Execute (10h) : To program data from the buffer to the cell array.
7. Get Feature (0Fh) : To read the status (OIP, PRG\_F bits) of the device.

Program Load Random Data and Get Feature commands are repeatable command.

The status of the internal ECC depends on ECC\_E bit in the feature table. When internal ECC is disabled, bit flips are not managed by the device.

**4.6. Block Erase (D8h)**

The Block Erase Operation erases the selected block. The page address is ignored automatically.

The operation sequence is as follows.

1. Write Enable (06h) : To enable the Erase Operation.
2. Block Erase (D8h) : To erase data in the block.
3. Get Feature (0Fh) : To read the status (OIP and ERS\_F bits) of the device.

Get Feature command is repeatable command.

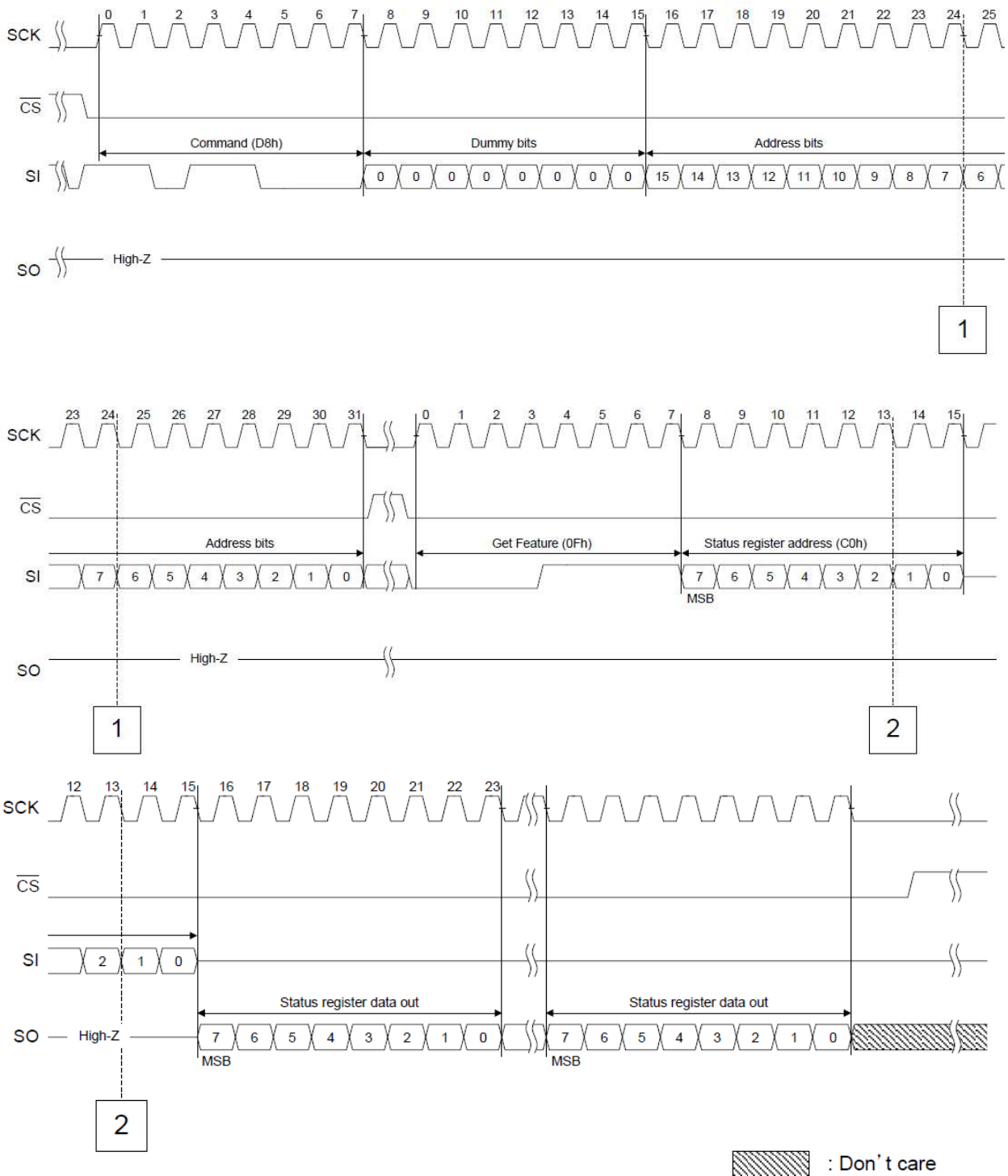


Figure 19. Block Erase Timing



**4.7. Reset (FFh or FEh)**

The Reset Operation is to reset the operations. For example, in case of a Program or Erase operation, the internally generated voltage is discharged and the device enters the busy state. The operation sequence is as follows.

1. Reset (FFh or FEh) :To reset the device
2. Get Feature (0Fh) :To read the status of the device

Get Feature command is repeatable command.

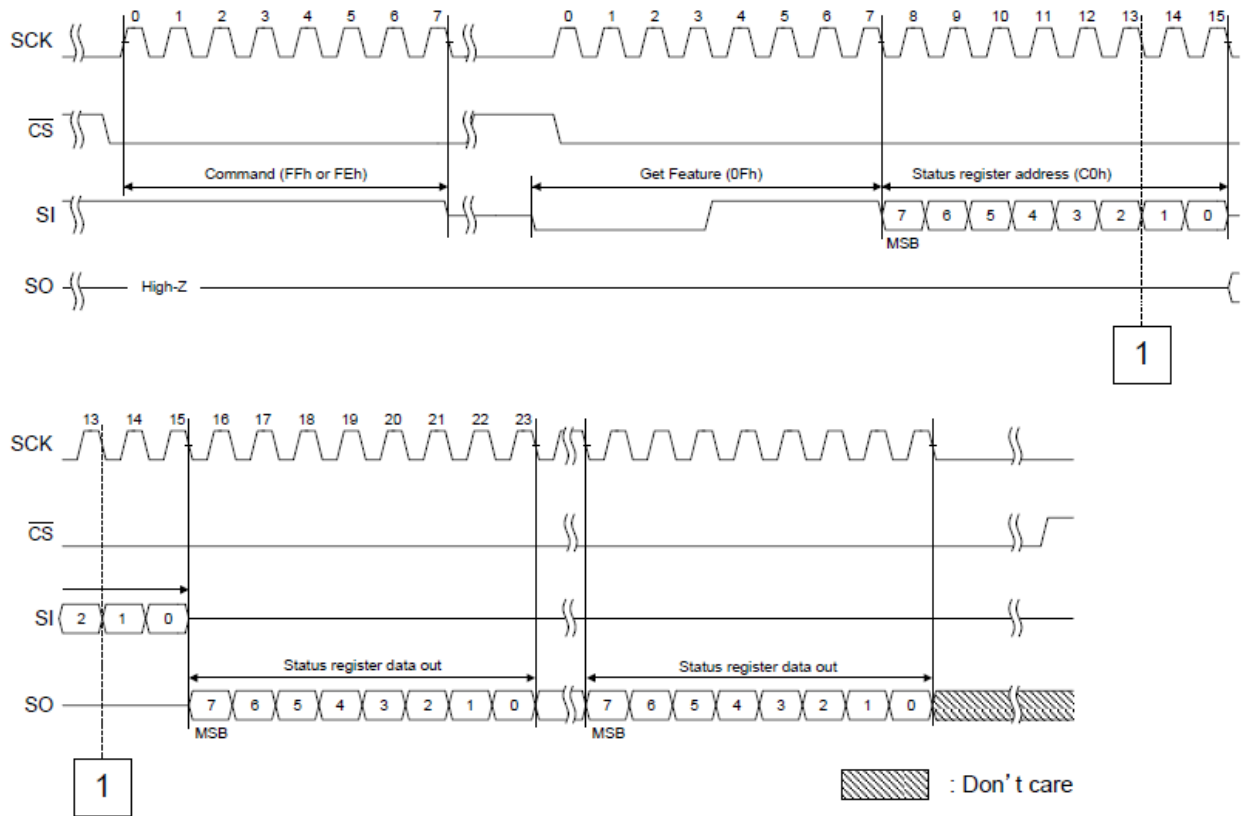


Figure 20. Reset Timing

**4.8. Write Enable (06h) / Write Disable (04h)**

The Write Enable / Disable commands set or reset the WEL (-Write Enable Latch) bit in the feature table shown in Table 12.

The Write Enable command sets the WEL bit to 1. The Write Enable command must be issued before the Page Program, Block Protection and Block Erase operations. The Write Disable command clears the WEL bit to 0. If the WEL bit is cleared, Page Program, Block Protection and Block Erase commands are ignored by the device.

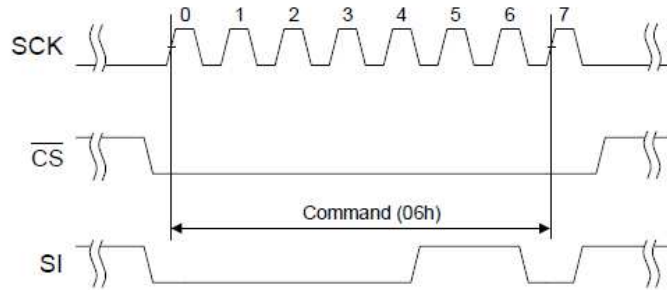


Figure 21. Write Enable

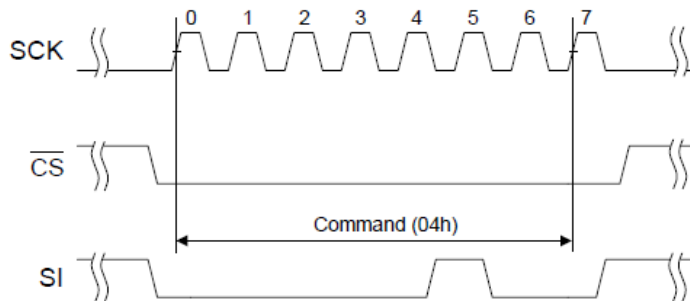


Figure 22. Write Disable Timing