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TOSHIBA MOS DIGITAL INTEGRATED CIRCUIT SILICON GATE CMOS

**2 GBIT (256M × 8 BIT) CMOS NAND E<sup>2</sup>PROM****DESCRIPTION**

The TC58NVG1S3HBAI6 is a single 3.3V 2 Gbit (2,281,701,376 bits) NAND Electrically Erasable and Programmable Read-Only Memory (NAND E<sup>2</sup>PROM) organized as (2048 + 128) bytes × 64 pages × 2048 blocks. The device has two 2176-byte static registers which allow program and read data to be transferred between the register and the memory cell array in 2176-byte increments. The Erase operation is implemented in a single block unit (128 Kbytes + 8 Kbytes: 2176 bytes × 64 pages).

The TC58NVG1S3HBAI6 is a serial-type memory device which utilizes the I/O pins for both address and data input/output as well as for command inputs. The Erase and Program operations are automatically executed making the device most suitable for applications such as solid-state file storage, voice recording, image file memory for still cameras and other systems which require high-density non-volatile memory data storage.

**FEATURES**

- Organization
  - Memory cell array           x8  
                                  2176 × 128K × 8
  - Register                    2176 × 8
  - Page size                   2176 bytes
  - Block size                  (128K + 8K) bytes
- Modes
  - Read, Reset, Auto Page Program, Auto Block Erase, Status Read, Page Copy, Multi Page Program, Multi Block Erase, Multi Page Copy, Multi Page Read
- Mode control
  - Serial input/output
  - Command control
- Number of valid blocks
  - Min 2008 blocks
  - Max 2048 blocks
- Power supply
  - V<sub>CC</sub> = 2.7V to 3.6V
- Access time
  - Cell array to register    25 μs max
  - Serial Read Cycle        25 ns min (CL=50pF)
- Program/Erase time
  - Auto Page Program        300 μs/page typ.
  - Auto Block Erase         2.5 ms/block typ.
- Operating current
  - Read (25 ns cycle)       30 mA max.
  - Program (avg.)            30 mA max
  - Erase (avg.)              30 mA max
  - Standby                   50 μA max
- Package
  - P-VFBGA67-0608-0.80-001 (Weight: 0.095 g typ.)
- 8 bit ECC for each 512Byte is required.

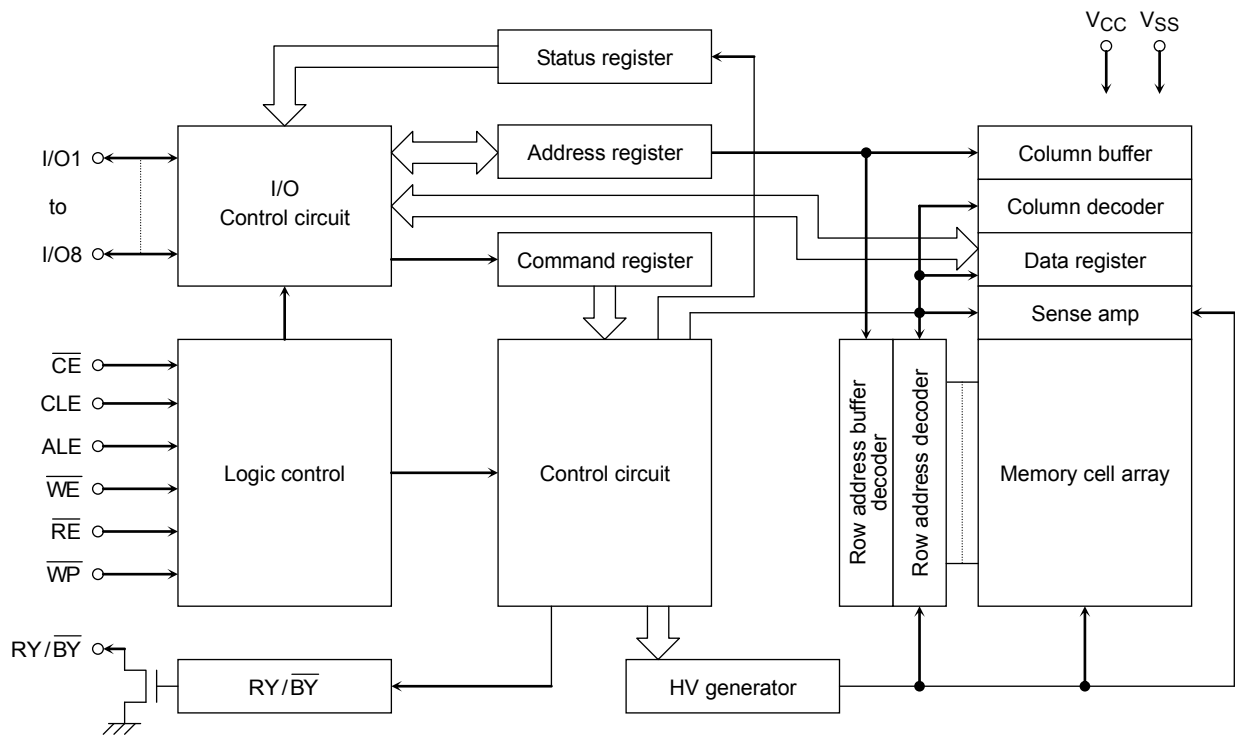
## PIN ASSIGNMENT (TOP VIEW)

	1	2	3	4	5	6	7	8
A		NC	NC			NC	NC	NC
B	NC	$\overline{WP}$	ALE	V <sub>SS</sub>	$\overline{CE}$	$\overline{WE}$	RY/ $\overline{BY}$	NC
C	NC	NC	$\overline{RE}$	CLE	NC	NC	NC	NC
D		NC	NC	NC	NC	NC	NC	
E		NC	NC	NC	NC	NC	NC	
F		NC	NC	NC	NC	NC	NC	
G		NC	I/O1	NC	NC	NC	V <sub>CC</sub>	
H	NC	NC	I/O2	NC	V <sub>CC</sub>	I/O6	I/O8	NC
J	NC	V <sub>SS</sub>	I/O3	I/O4	I/O5	I/O7	V <sub>SS</sub>	NC
K	NC	NC	NC			NC	NC	NC

## PIN NAMES

I/O1 to I/O8	I/O port
$\overline{CE}$	Chip enable
$\overline{WE}$	Write enable
$\overline{RE}$	Read enable
CLE	Command latch enable
ALE	Address latch enable
$\overline{WP}$	Write protect
RY/ $\overline{BY}$	Ready/Busy
V <sub>CC</sub>	Power supply
V <sub>SS</sub>	Ground
NC	No Connection

## BLOCK DIAGRAM



## ABSOLUTE MAXIMUM RATINGS

SYMBOL	RATING	VALUE	UNIT
V <sub>CC</sub>	Power Supply Voltage	-0.6 to 4.6	V
V <sub>IN</sub>	Input Voltage	-0.6 to 4.6	V
V <sub>I/O</sub>	Input /Output Voltage	-0.6 to V <sub>CC</sub> + 0.3 (≤ 4.6 V)	V
P <sub>D</sub>	Power Dissipation	0.3	W
T <sub>SOLDER</sub>	Soldering Temperature (10 s)	260	°C
T <sub>STG</sub>	Storage Temperature	-55 to 125	°C
T <sub>OPR</sub>	Operating Temperature	-40 to 85	°C

## CAPACITANCE \*(Ta = 25°C, f = 1 MHz)

SYMBOL	PARAMETER	CONDITION	MIN	MAX	UNIT
C <sub>IN</sub>	Input	V <sub>IN</sub> = 0 V	—	10	pF
C <sub>OUT</sub>	Output	V <sub>OUT</sub> = 0 V	—	10	pF

\* This parameter is periodically sampled and is not tested for every device.

## VALID BLOCKS

SYMBOL	PARAMETER	MIN	TYP.	MAX	UNIT
N <sub>VB</sub>	Number of Valid Blocks	2008	—	2048	Blocks

NOTE: The device occasionally contains unusable blocks. Refer to Application Note (13) toward the end of this document.

The first block (Block 0) is guaranteed to be a valid block at the time of shipment.

The specification for the minimum number of valid blocks is applicable over lifetime

The number of valid blocks is on the basis of single plane operations, and this may be decreased with two plane operations.

## RECOMMENDED DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN	TYP.	MAX	UNIT
V <sub>CC</sub>	Power Supply Voltage	2.7	—	3.6	V
V <sub>IH</sub>	High Level input Voltage	V <sub>CC</sub> x 0.8	—	V <sub>CC</sub> + 0.3	V
V <sub>IL</sub>	Low Level Input Voltage	-0.3*	—	V <sub>CC</sub> x 0.2	V

\* -2 V (pulse width lower than 20 ns)

## DC CHARACTERISTICS (Ta = -40 to 85°C, V<sub>CC</sub> = 2.7 to 3.6V)

SYMBOL	PARAMETER	CONDITION	MIN	TYP.	MAX	UNIT
I <sub>IL</sub>	Input Leakage Current	V <sub>IN</sub> = 0 V to V <sub>CC</sub>	—	—	±10	μA
I <sub>LO</sub>	Output Leakage Current	V <sub>OUT</sub> = 0 V to V <sub>CC</sub>	—	—	±10	μA
I <sub>CCO1</sub>	Serial Read Current	$\overline{CE} = V_{IL}$ , I <sub>OUT</sub> = 0 mA, t <sub>cycle</sub> = 25 ns	—	—	30	mA
I <sub>CCO2</sub>	Programming Current	—	—	—	30	mA
I <sub>CCO3</sub>	Erasing Current	—	—	—	30	mA
I <sub>CCS</sub>	Standby Current	$\overline{CE} = V_{CC} - 0.2 V$ , $\overline{WP} = 0 V/V_{CC}$	—	—	50	μA
V <sub>OH</sub>	High Level Output Voltage	I <sub>OH</sub> = -0.1 mA	V <sub>CC</sub> - 0.2	—	—	V
V <sub>OL</sub>	Low Level Output Voltage	I <sub>OL</sub> = 0.1 mA	—	—	0.2	V
I <sub>OL</sub> (RY/ $\overline{BY}$ )	Output current of RY/ $\overline{BY}$ pin	V <sub>OL</sub> = 0.2 V	—	4	—	mA

## AC CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

(Ta = -40 to 85°C, VCC = 2.7 to 3.6V)

SYMBOL	PARAMETER	MIN	MAX	UNIT
t <sub>CLS</sub>	CLE Setup Time	12	—	ns
t <sub>CLH</sub>	CLE Hold Time	5	—	ns
t <sub>CS</sub>	$\overline{CE}$ Setup Time	20	—	ns
t <sub>CH</sub>	$\overline{CE}$ Hold Time	5	—	ns
t <sub>WP</sub>	Write Pulse Width	12	—	ns
t <sub>ALS</sub>	ALE Setup Time	12	—	ns
t <sub>ALH</sub>	ALE Hold Time	5	—	ns
t <sub>DS</sub>	Data Setup Time	12	—	ns
t <sub>DH</sub>	Data Hold Time	5	—	ns
t <sub>WC</sub>	Write Cycle Time	25	—	ns
t <sub>WH</sub>	$\overline{WE}$ High Hold Time	10	—	ns
t <sub>WW</sub>	$\overline{WP}$ High to $\overline{WE}$ Low	100	—	ns
t <sub>RR</sub>	Ready to $\overline{RE}$ Falling Edge	20	—	ns
t <sub>RW</sub>	Ready to $\overline{WE}$ Falling Edge	20	—	ns
t <sub>RP</sub>	Read Pulse Width	12	—	ns
t <sub>RC</sub>	Read Cycle Time	25	—	ns
t <sub>REA</sub>	$\overline{RE}$ Access Time	—	20	ns
t <sub>CEA</sub>	$\overline{CE}$ Access Time	—	25	ns
t <sub>CLR</sub>	CLE Low to $\overline{RE}$ Low	10	—	ns
t <sub>AR</sub>	ALE Low to $\overline{RE}$ Low	10	—	ns
t <sub>RHOH</sub>	$\overline{RE}$ High to Output Hold Time	25	—	ns
t <sub>RLOH</sub>	$\overline{RE}$ Low to Output Hold Time	5	—	ns
t <sub>RHZ</sub>	$\overline{RE}$ High to Output High Impedance	—	60	ns
t <sub>CHZ</sub>	$\overline{CE}$ High to Output High Impedance	—	20	ns
t <sub>CSD</sub>	$\overline{CE}$ High to ALE or CLE Don't Care	0	—	ns
t <sub>REH</sub>	$\overline{RE}$ High Hold Time	10	—	ns
t <sub>IR</sub>	Output-High-impedance-to- $\overline{RE}$ Falling Edge	0	—	ns
t <sub>RHW</sub>	$\overline{RE}$ High to $\overline{WE}$ Low	30	—	ns
t <sub>WHC</sub>	$\overline{WE}$ High to $\overline{CE}$ Low	30	—	ns
t <sub>WHR</sub>	$\overline{WE}$ High to $\overline{RE}$ Low	60	—	ns
t <sub>R</sub>	Memory Cell Array to Starting Address	—	25	μs
t <sub>DCBSYR1</sub>	Data Cache Busy in Read Cache (following 31h and 3Fh)	—	25	μs
t <sub>DCBSYR2</sub>	Data Cache Busy in Page Copy (following 3Ah)	—	30	μs
t <sub>WB</sub>	$\overline{WE}$ High to Busy	—	100	ns
t <sub>RST</sub>	Device Reset Time (Ready/Read/Program/Erase)	—	5/5/10/500	μs

\*1: t<sub>CLS</sub> and t<sub>ALS</sub> can not be shorter than t<sub>WP</sub>

\*2: t<sub>CS</sub> should be longer than t<sub>WP</sub> + 8ns.

**AC TEST CONDITIONS**

PARAMETER	CONDITION
	$V_{CC}$ : 2.7 to 3.6V
Input level	$V_{CC} - 0.2\text{ V}$ , 0.2 V
Input pulse rise and fall time	3 ns
Input comparison level	$V_{CC} / 2$
Output data comparison level	$V_{CC} / 2$
Output load	$C_L$ (50 pF) + 1 TTL

Note: Busy to ready time depends on the pull-up resistor tied to the  $\overline{RY}/\overline{BY}$  pin.  
(Refer to Application Note (9) toward the end of this document.)

**PROGRAMMING AND ERASING CHARACTERISTICS**  
( $T_a = -40$  to  $85^\circ\text{C}$ ,  $V_{CC} = 2.7$  to  $3.6\text{V}$ )

SYMBOL	PARAMETER	MIN	TYP.	MAX	UNIT	NOTES
$t_{\text{PROG}}$	Average Programming Time	—	300	700	$\mu\text{s}$	
$t_{\text{DCBSYW1}}$	Data Cache Busy Time in Write Cache (following 11h)	—	—	10	$\mu\text{s}$	
$t_{\text{DCBSYW2}}$	Data Cache Busy Time in Write Cache (following 15h)	—	—	700	$\mu\text{s}$	(2)
N	Number of Partial Program Cycles in the Same Page	—	—	4		(1)
$t_{\text{BERASE}}$	Block Erasing Time	—	2.5	5	ms	

(1) Refer to Application Note (12) toward the end of this document.

(2)  $t_{\text{DCBSYW2}}$  depends on the timing between internal programming time and data in time.

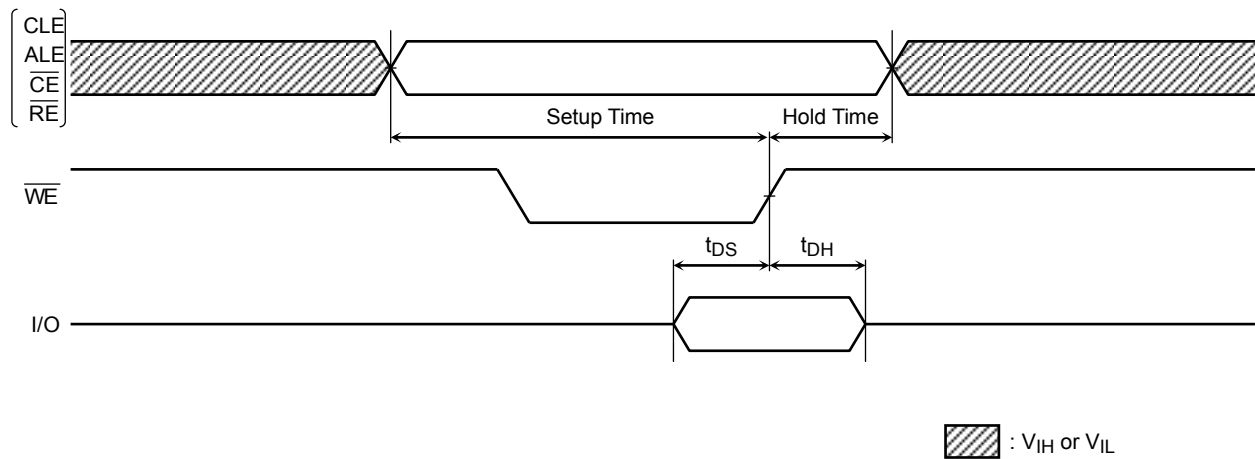
**Data Output**

When  $t_{\text{REH}}$  is long, output buffers are disabled by  $\overline{RE}=\text{High}$ , and the hold time of data output depend on  $t_{\text{RHOH}}$  (25ns MIN). On this condition, waveforms look like normal serial read mode.

When  $t_{\text{REH}}$  is short, output buffers are not disabled by  $\overline{RE}=\text{High}$ , and the hold time of data output depend on  $t_{\text{RLOH}}$  (5ns MIN). On this condition, output buffers are disabled by the rising edge of  $\overline{CLE}/\overline{ALE}/\overline{CE}$  or falling edge of  $\overline{WE}$ , and waveforms look like Extended Data Output Mode.

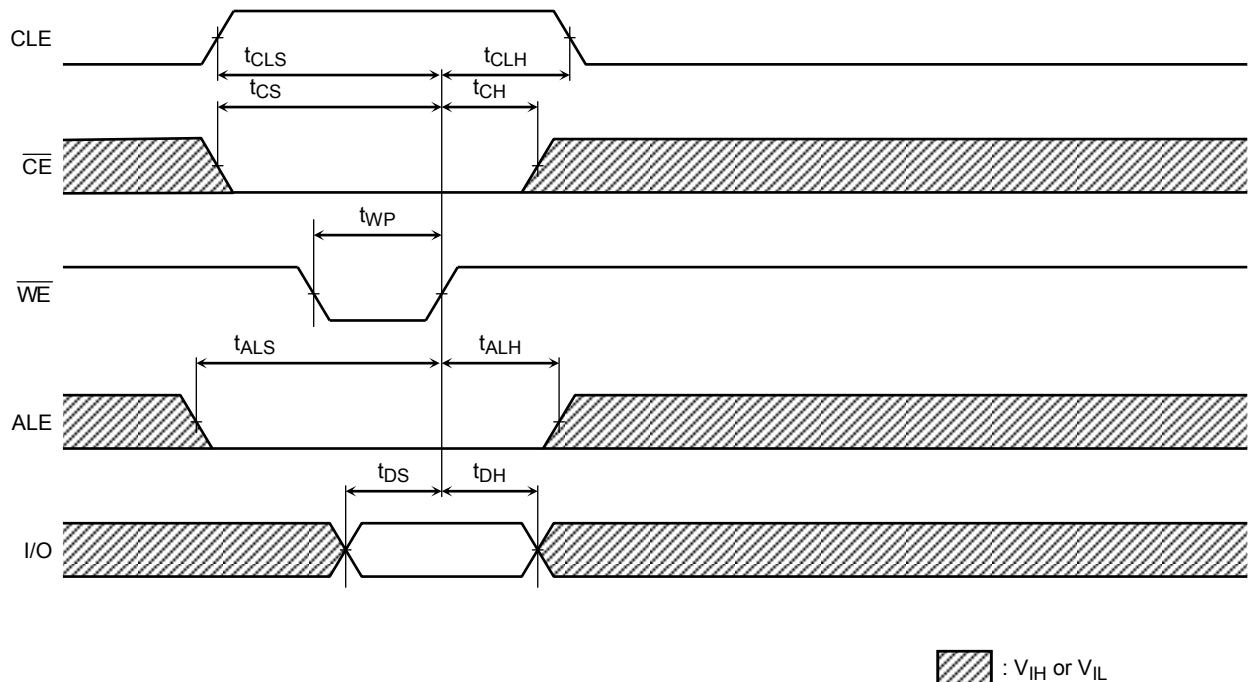
**TIMING DIAGRAMS**

Latch Timing Diagram for Command/Address/Data



:  $V_{IH}$  or  $V_{IL}$

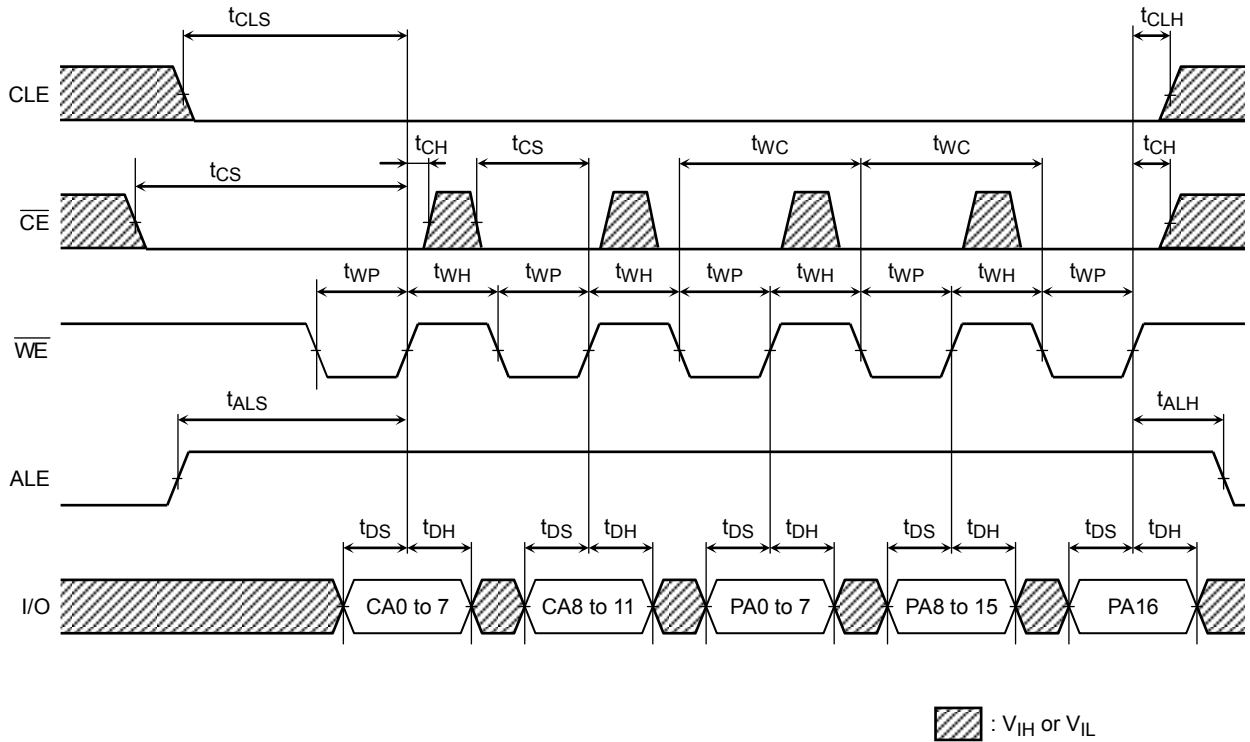
Command Input Cycle Timing Diagram



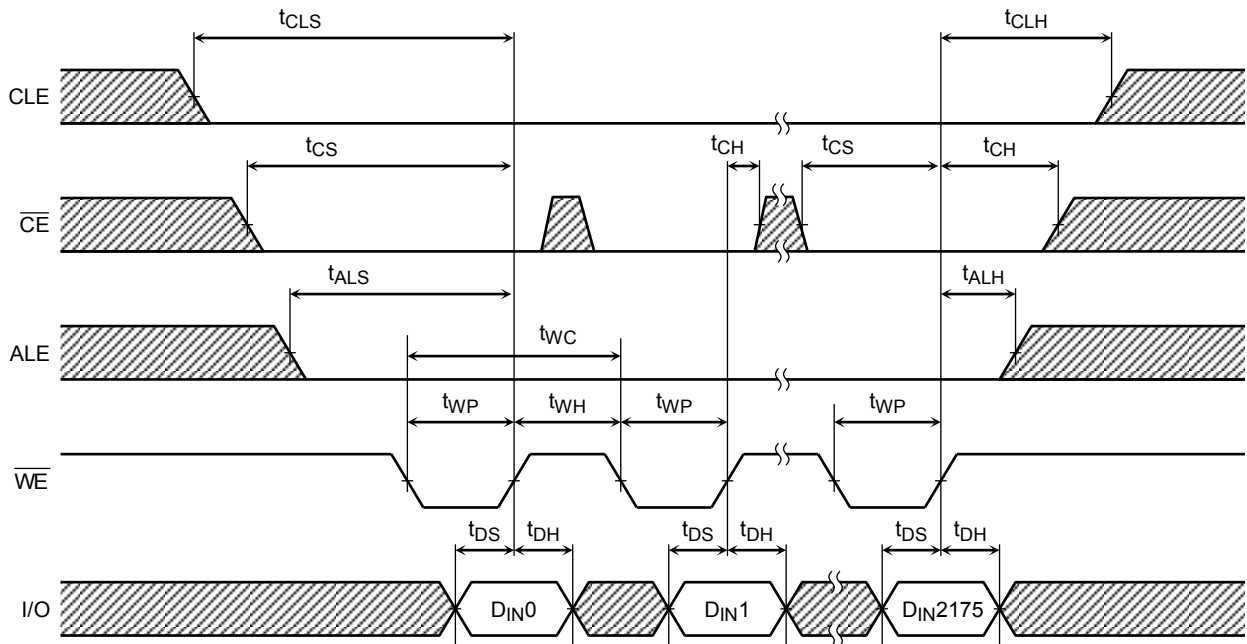
:  $V_{IH}$  or  $V_{IL}$



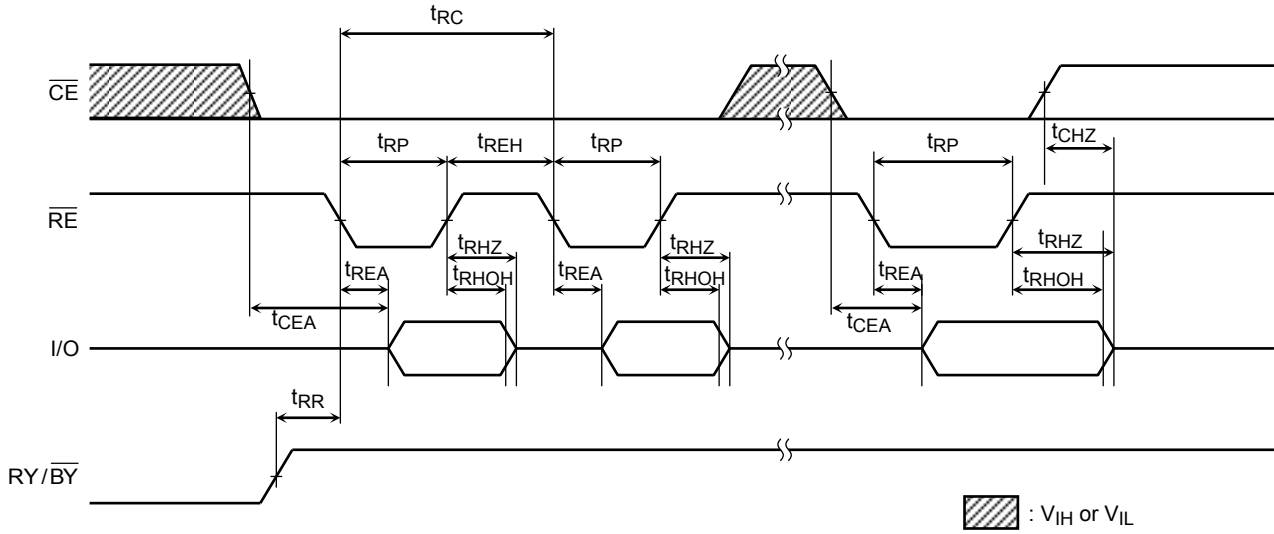
Address Input Cycle Timing Diagram



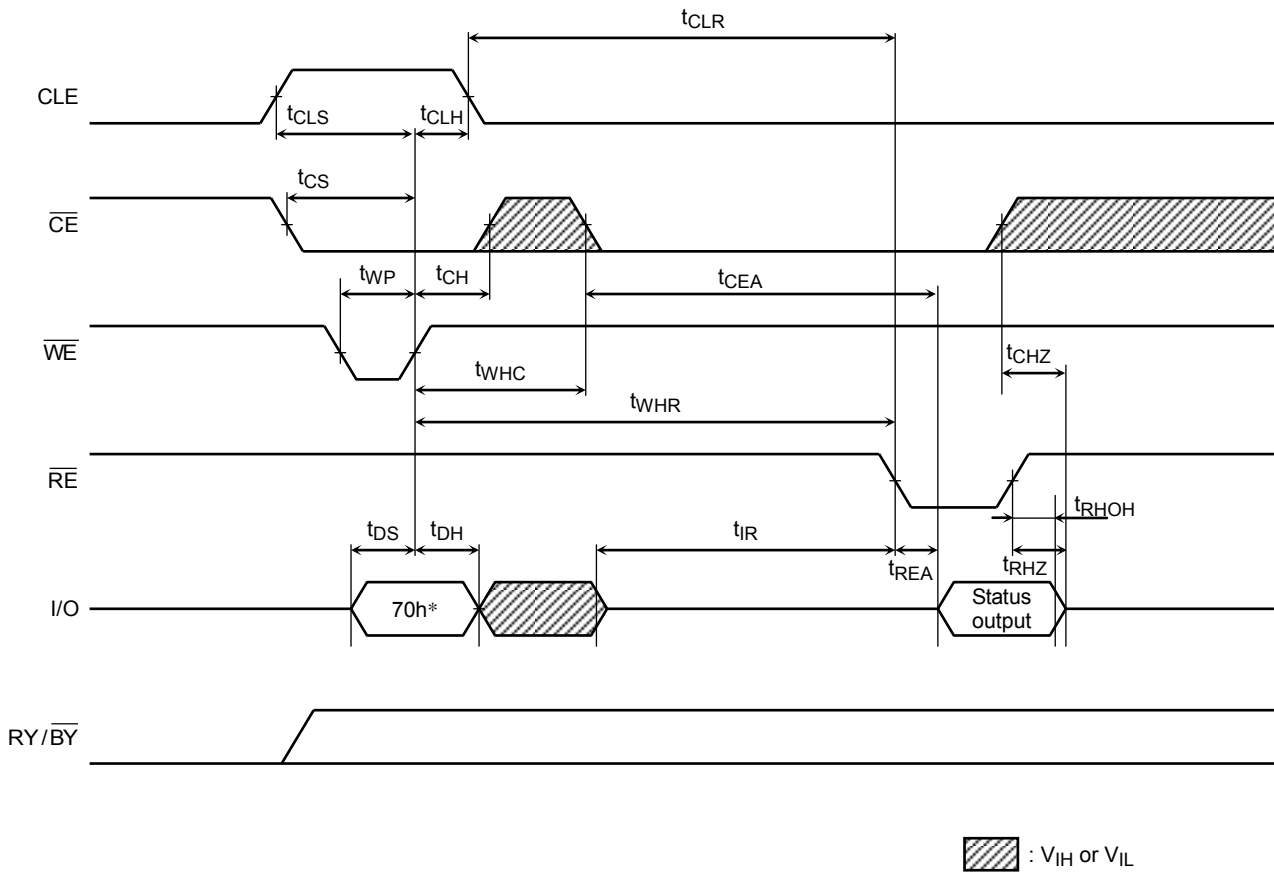
Data Input Cycle Timing Diagram



Serial Read Cycle Timing Diagram



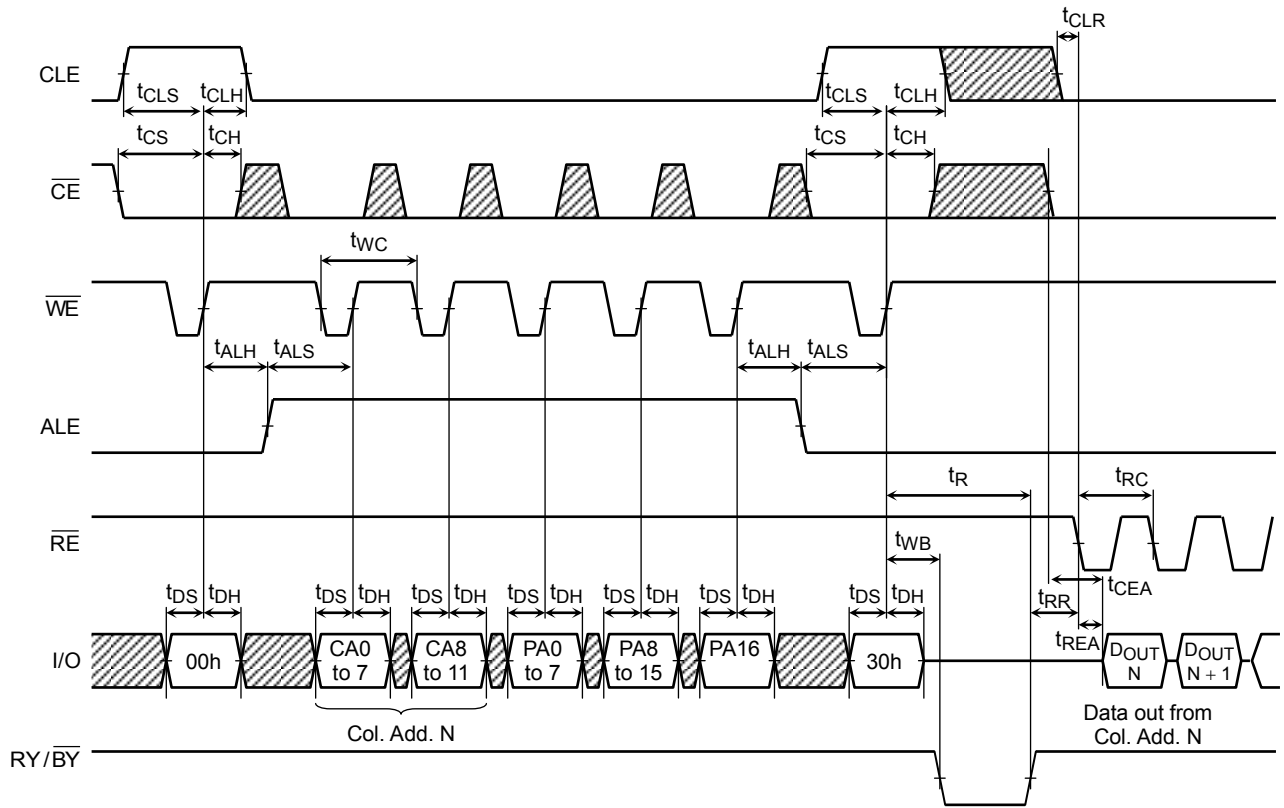
Status Read Cycle Timing Diagram



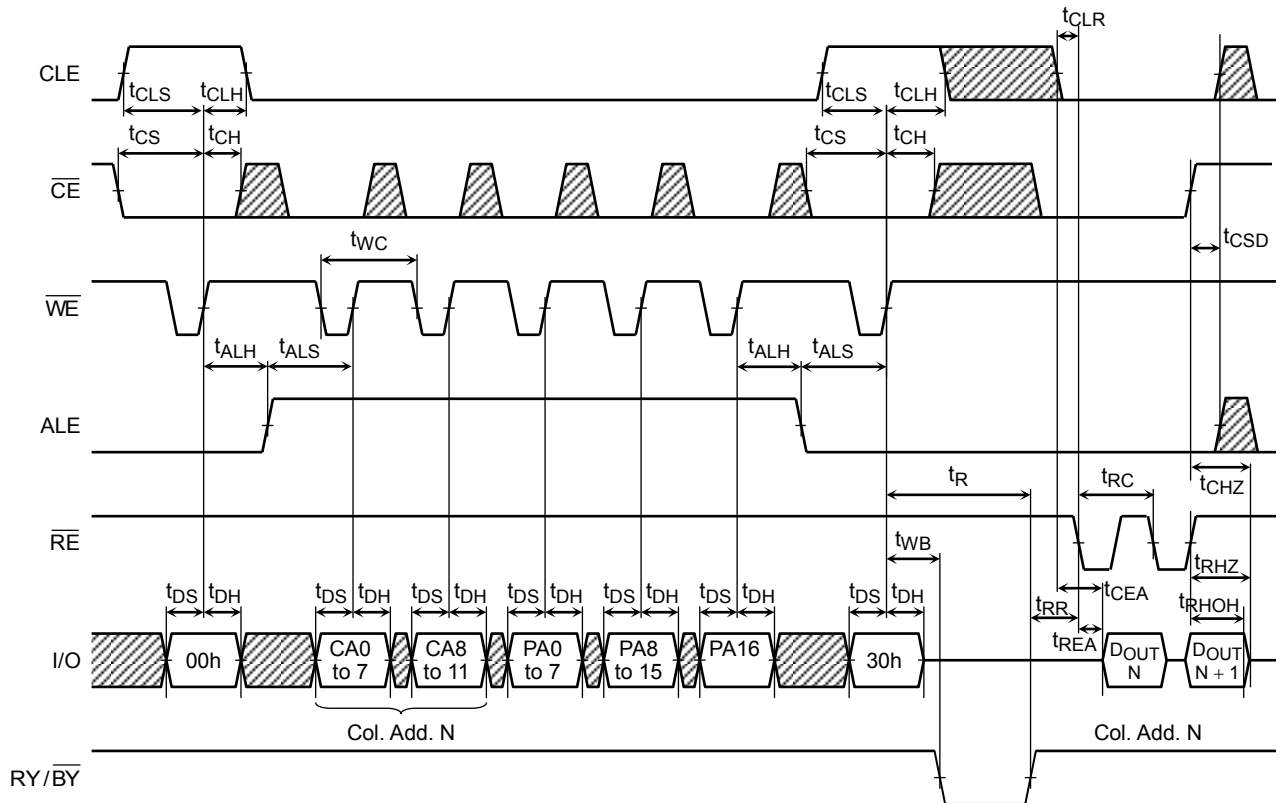
\*: 70h represents the hexadecimal number

▨ :  $V_{IH}$  or  $V_{IL}$

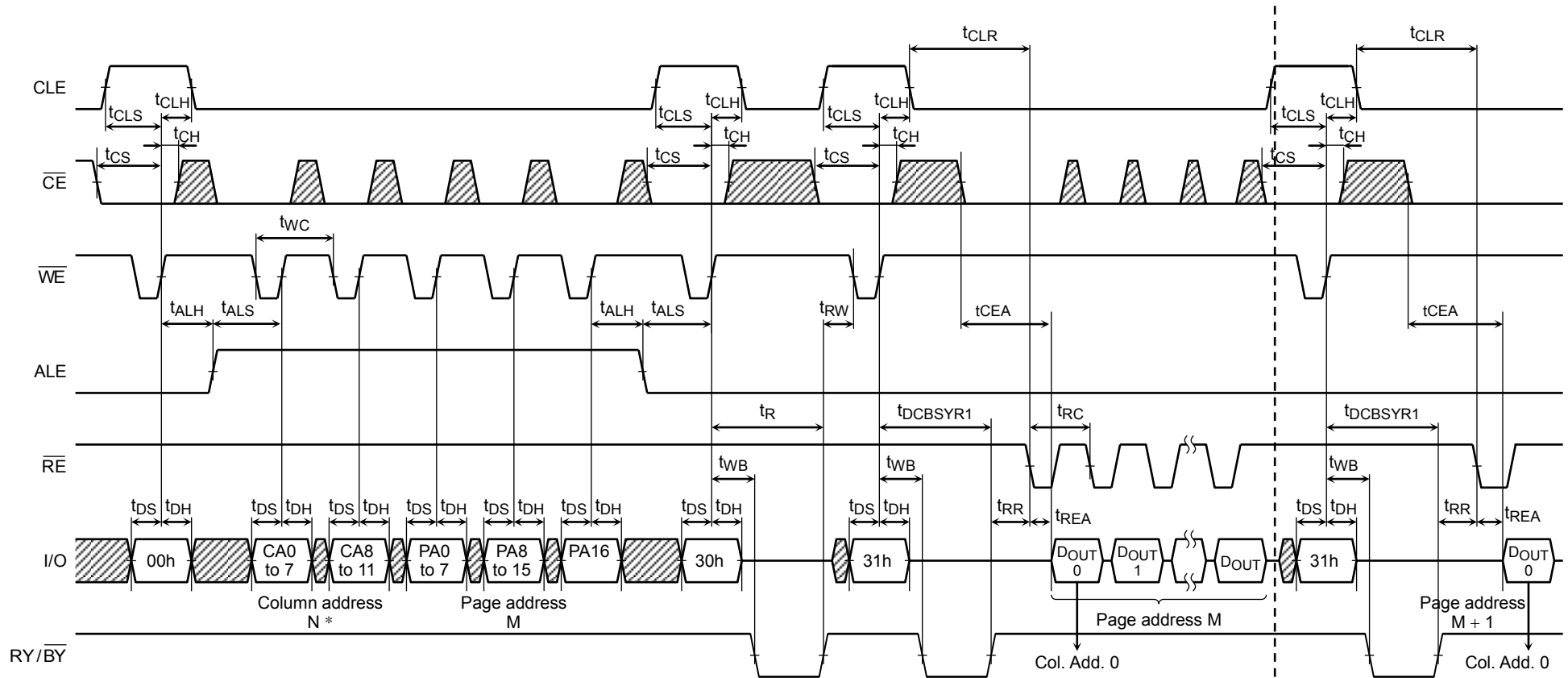
Read Cycle Timing Diagram



Read Cycle Timing Diagram: When Interrupted by  $\overline{CE}$



Read Cycle with Data Cache Timing Diagram (1/2)

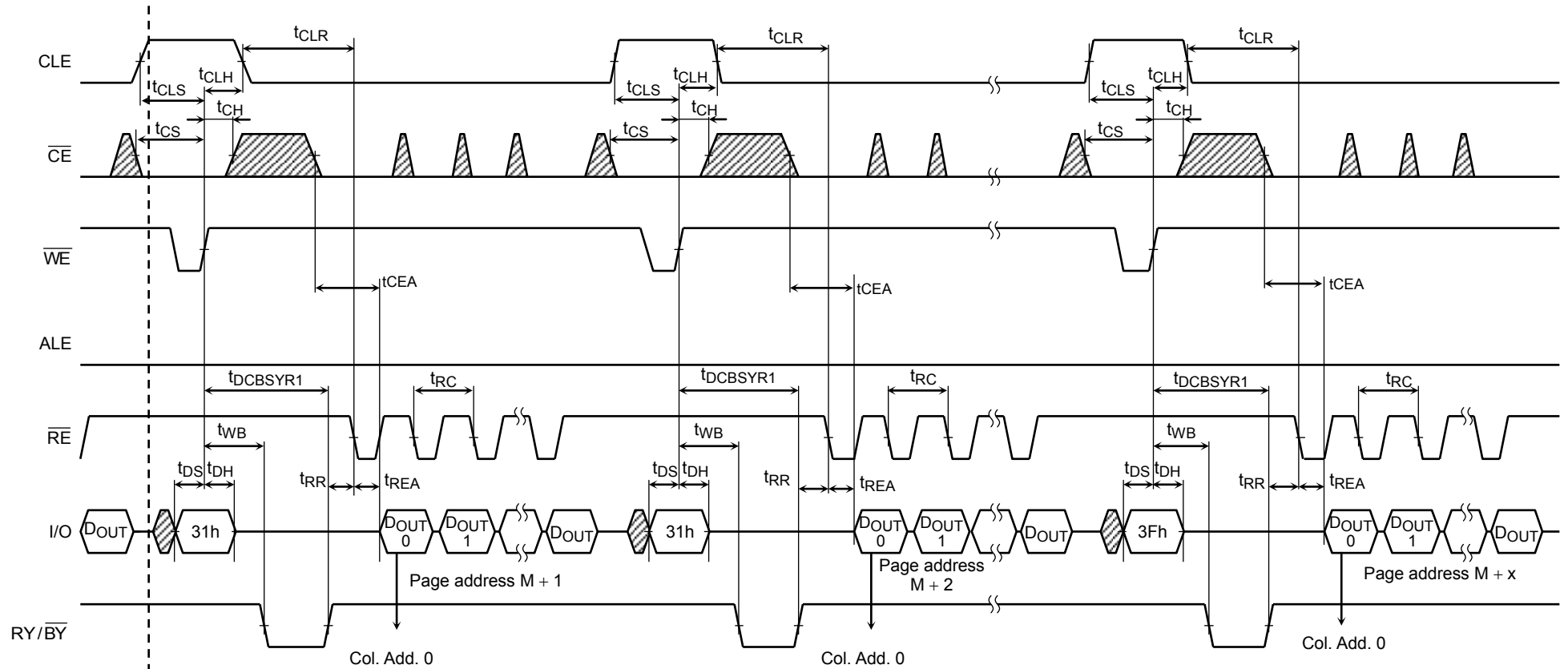


\* The column address will be reset to 0 by the 31h command input.

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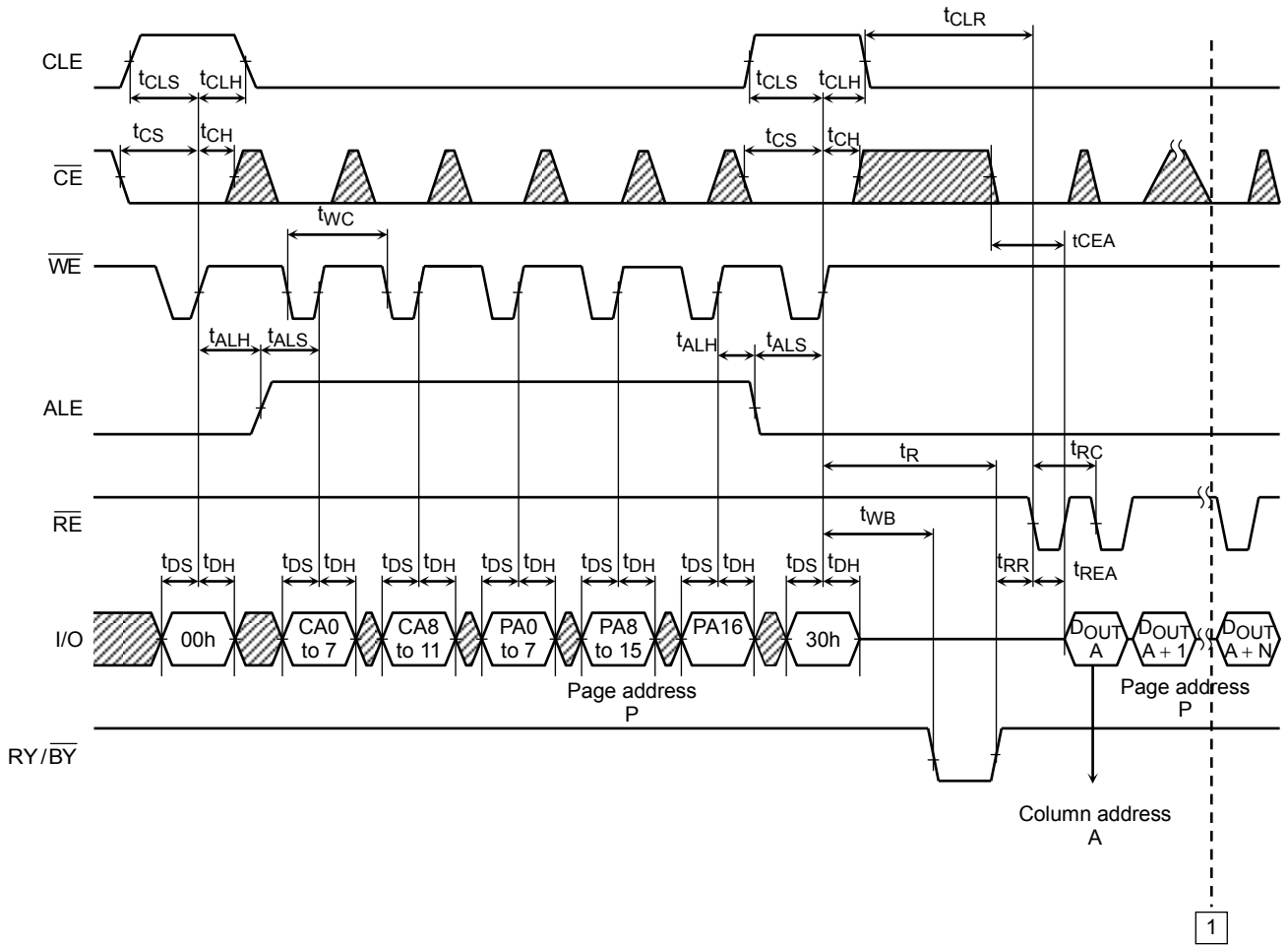
Read Cycle with Data Cache Timing Diagram (2/2)



Make sure to terminate the operation with 3Fh command.

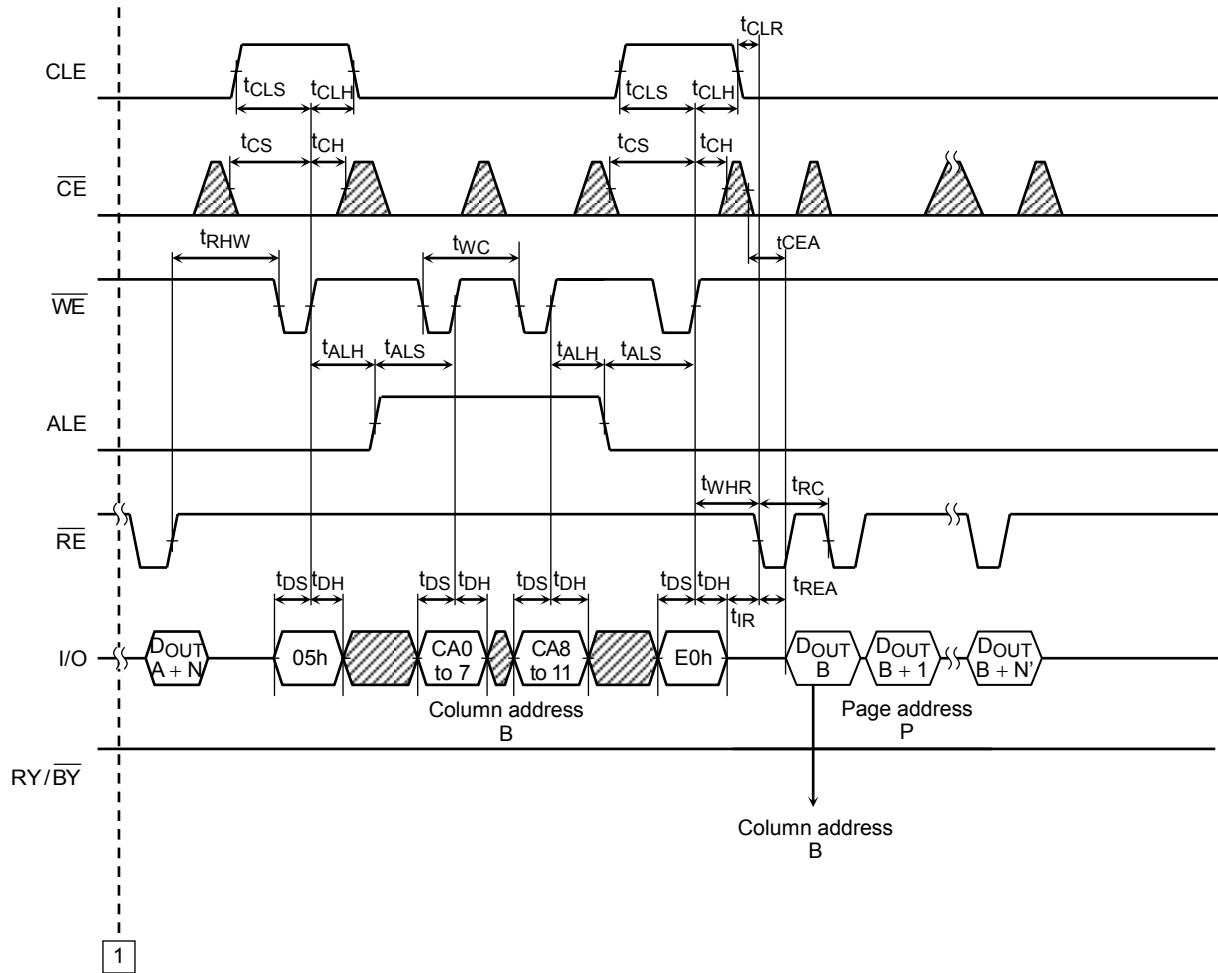
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Column Address Change in Read Cycle Timing Diagram (1/2)



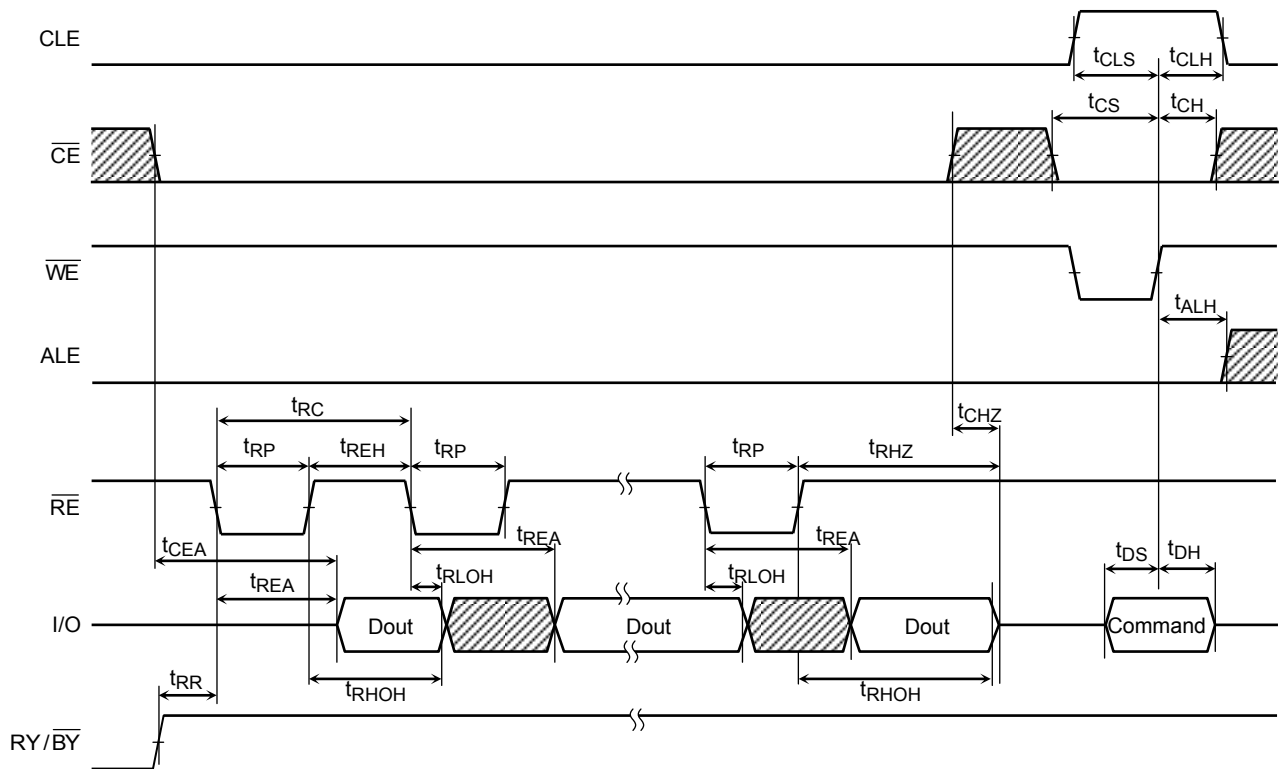
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Column Address Change in Read Cycle Timing Diagram (2/2)



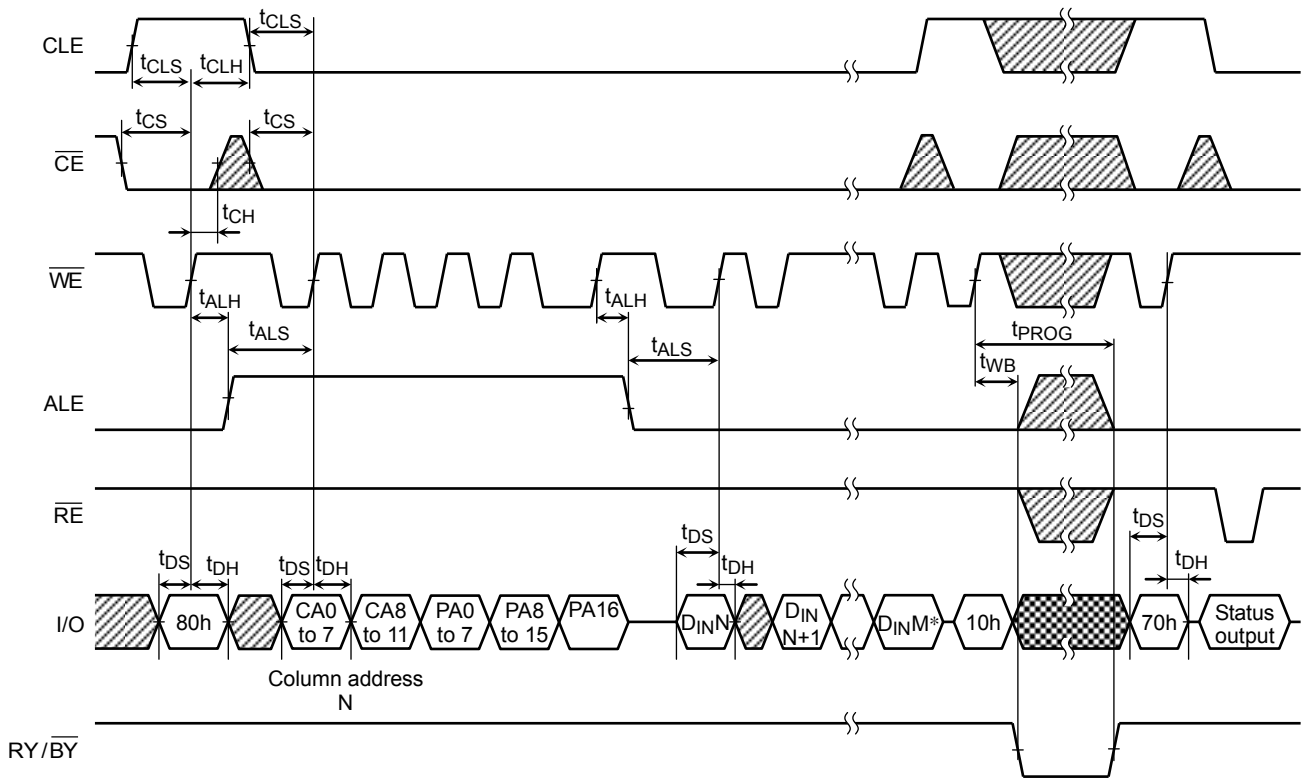
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Data Output Timing Diagram





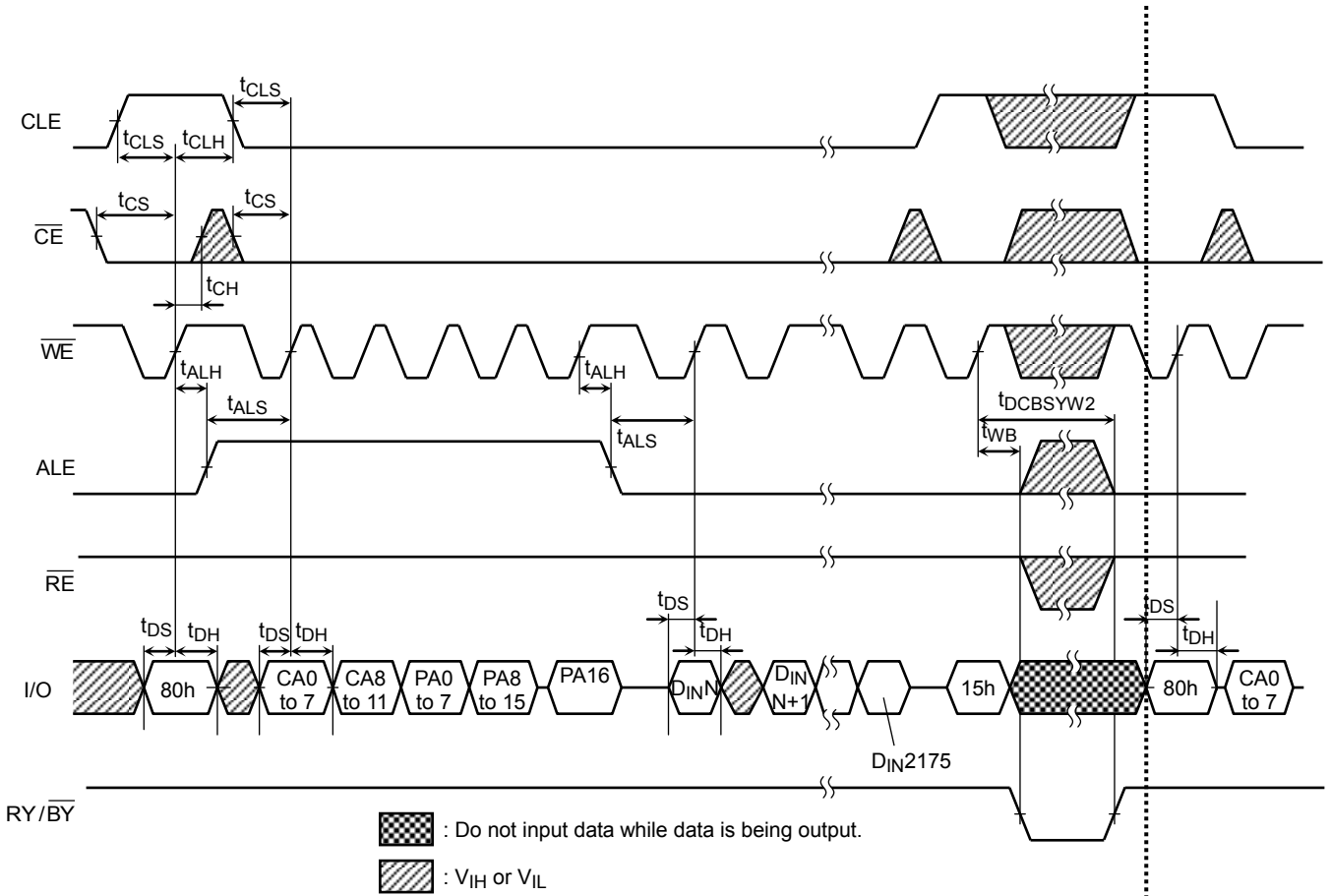
Auto-Program Operation Timing Diagram



-  : Do not input data while data is being output.
-  :  $V_{IH}$  or  $V_{IL}$

\*) M: up to 2175 (byte input data for ×8 device).

Auto-Program Operation with Data Cache Timing Diagram (1/3)

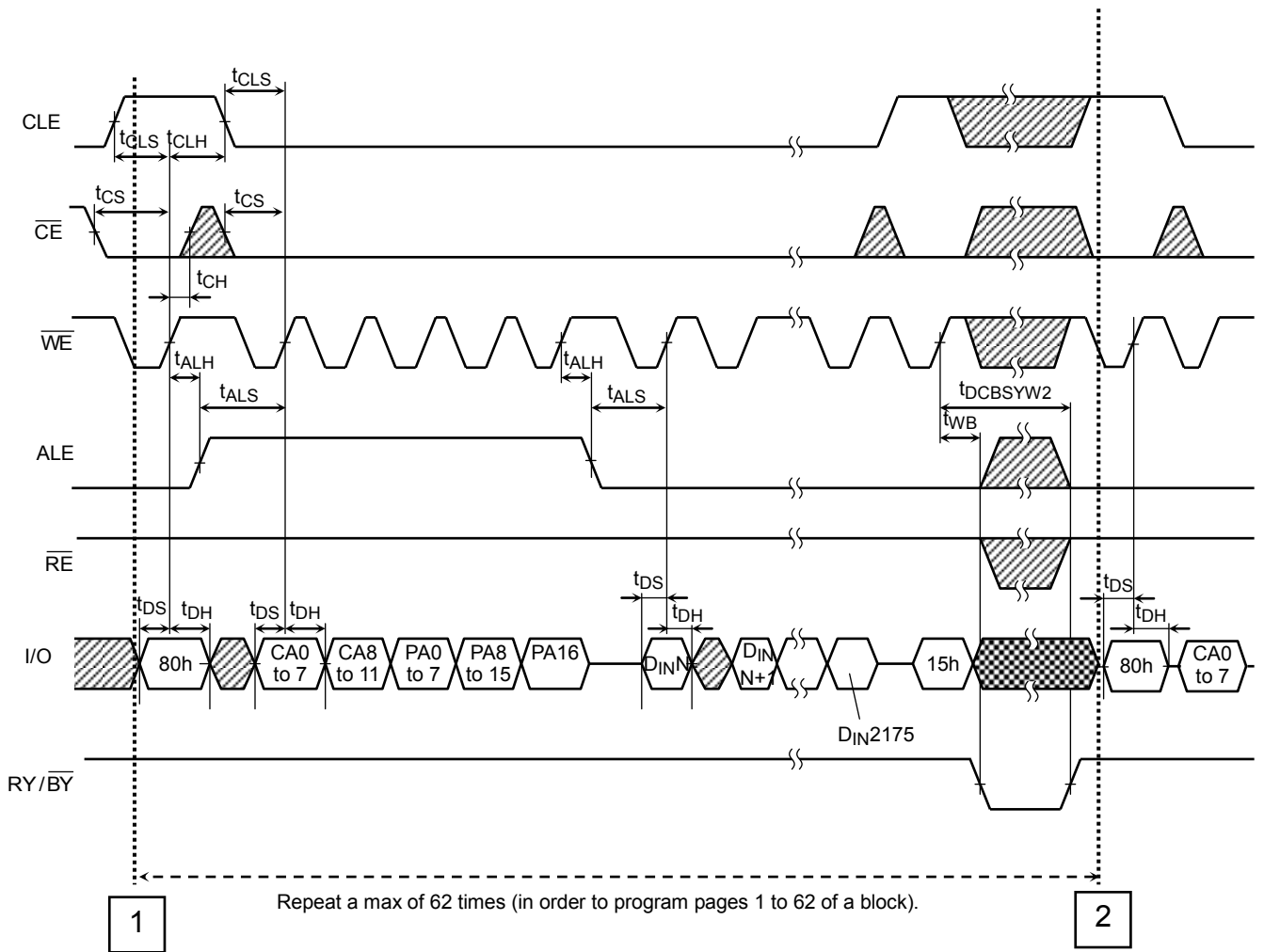


CA0 to CA11 is 0 in this diagram.

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Auto-Program Operation with Data Cache Timing Diagram (2/3)

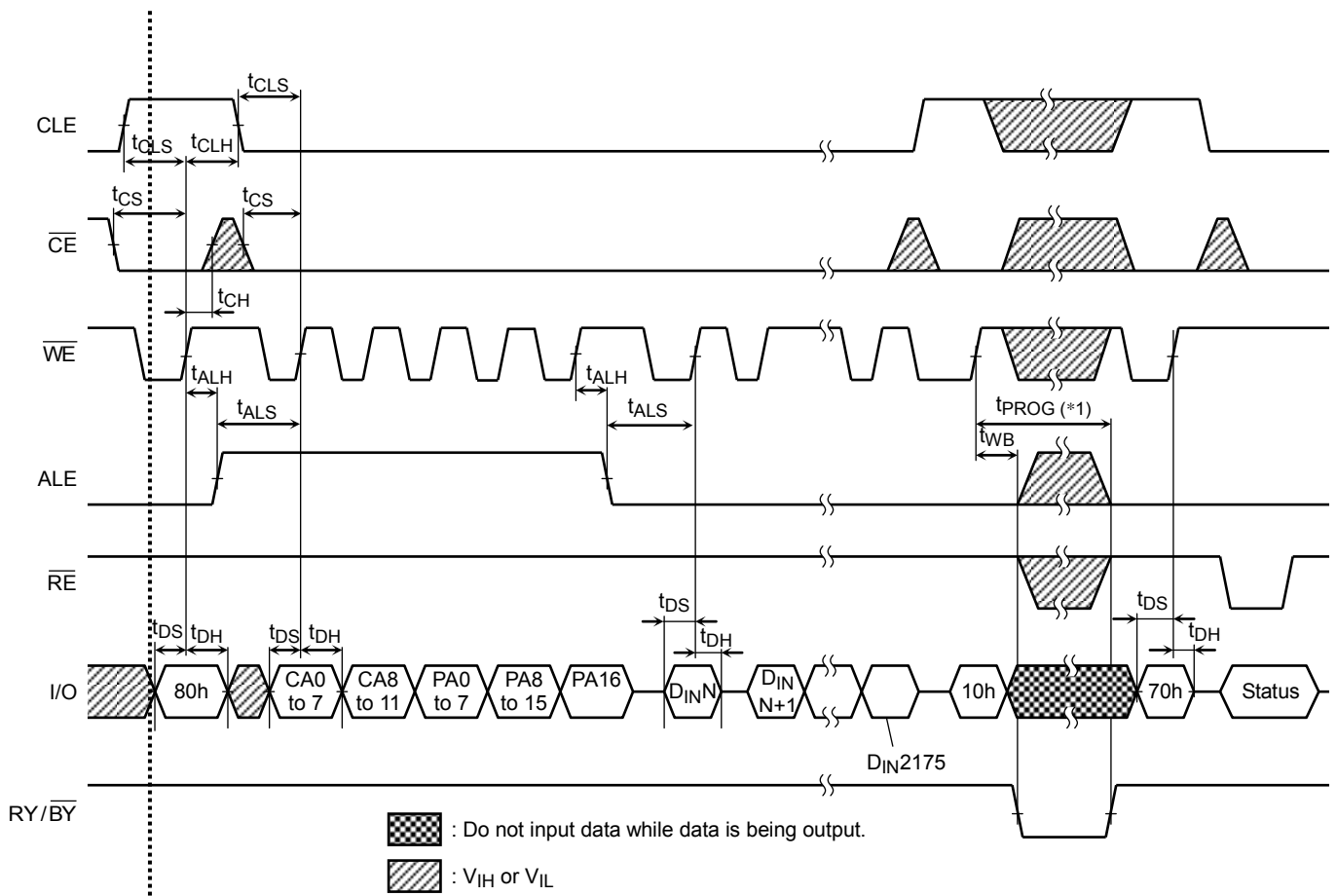


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-  : Do not input data while data is being output.
-  :  $V_{IH}$  or  $V_{IL}$

Auto-Program Operation with Data Cache Timing Diagram (3/3)



2

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(\*1)  $t_{PROG}$ : Since the last page programming by 10h command is initiated after the previous cache program, the  $t_{PROG}$  during cache programming is given by the following equation.

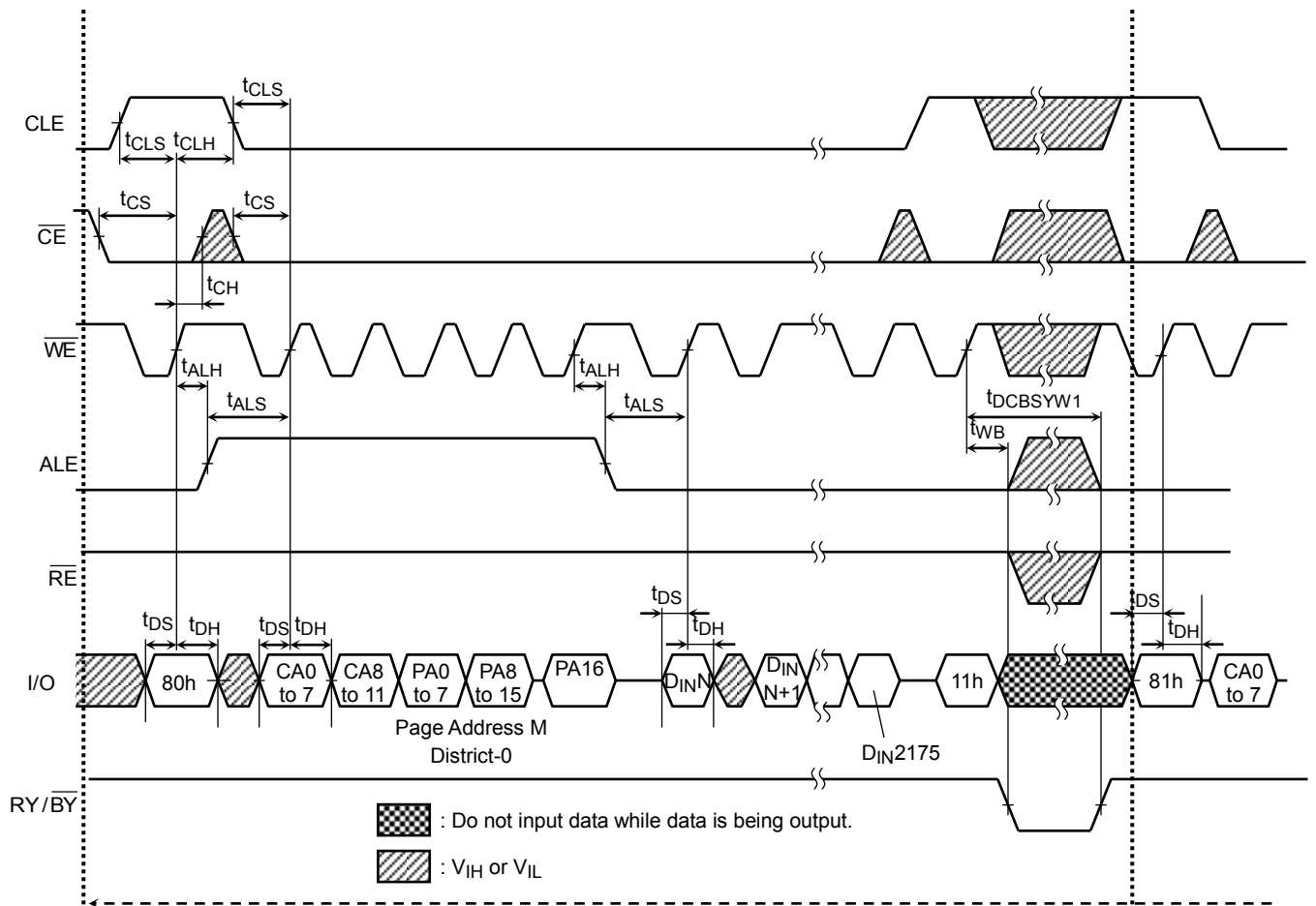
$$t_{PROG} = t_{PROG} \text{ of the last page} + t_{PROG} \text{ of the previous page} - A$$

$$A = (\text{command input cycle} + \text{address input cycle} + \text{data input cycle time of the last page})$$

If "A" exceeds the  $t_{PROG}$  of previous page,  $t_{PROG}$  of the last page is  $t_{PROG} \text{ max.}$

(Note) Make sure to terminate the operation with 80h-10h- command sequence.  
 If the operation is terminated by 80h-15h command sequence, monitor I/O 6 (Ready / Busy) by issuing Status Read command (70h) and make sure the previous page program operation is completed. If the page program operation is completed issue FFh reset before next operation.

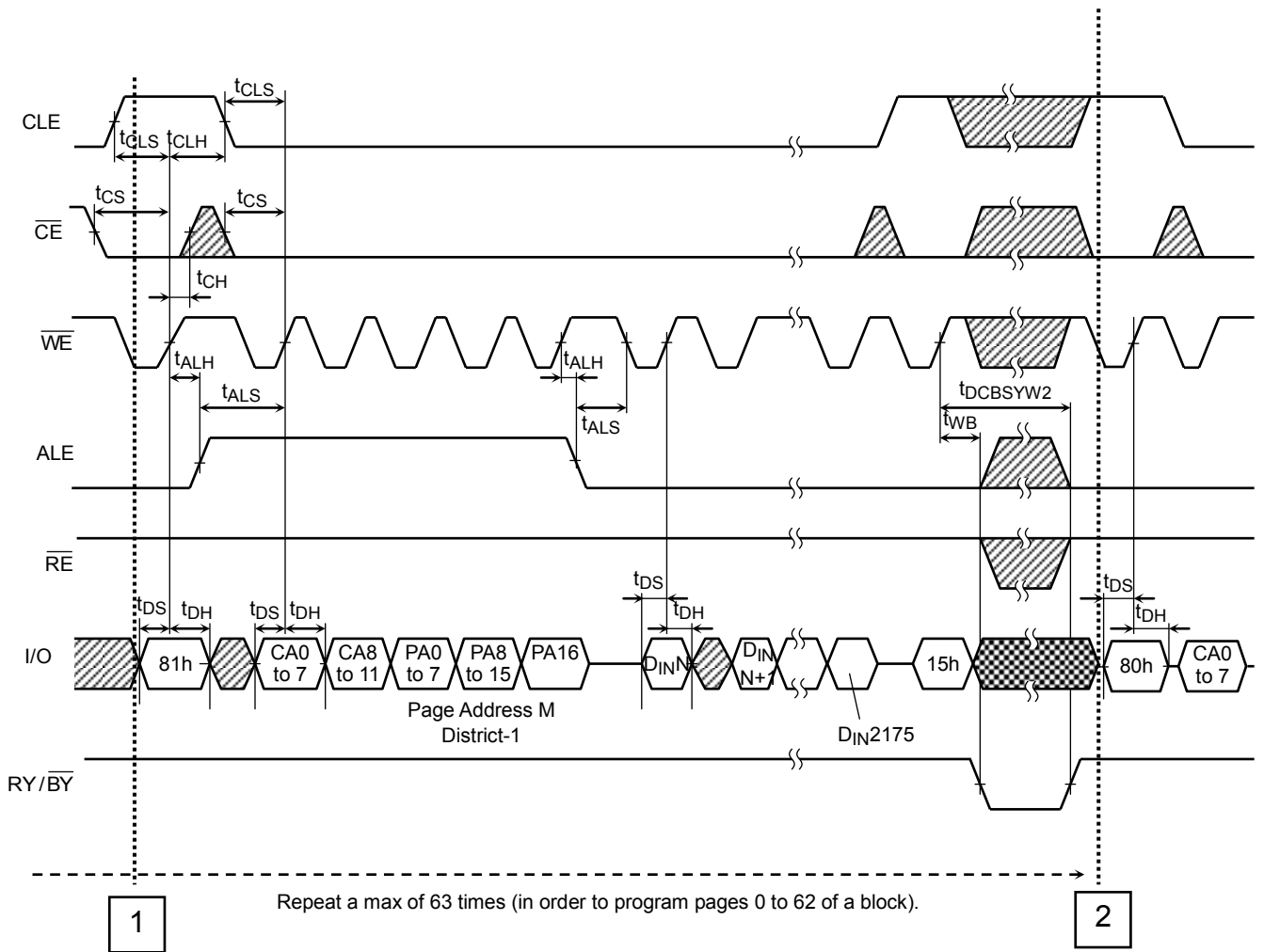
Multi-Page Program Operation with Data Cache Timing Diagram (1/4)



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Multi-Page Program Operation with Data Cache Timing Diagram (2/4)

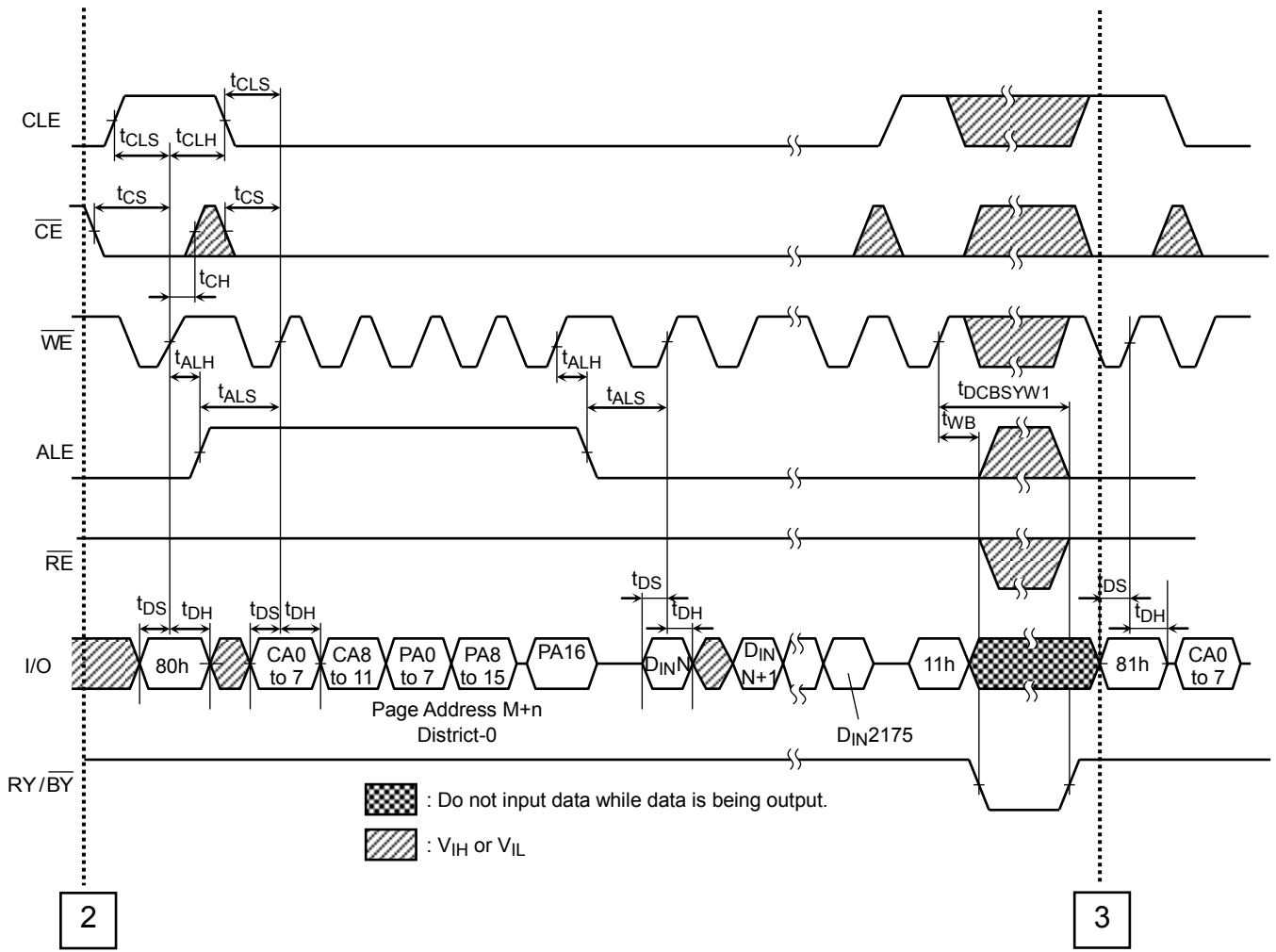


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-  : Do not input data while data is being output.
-  :  $V_{IH}$  or  $V_{IL}$

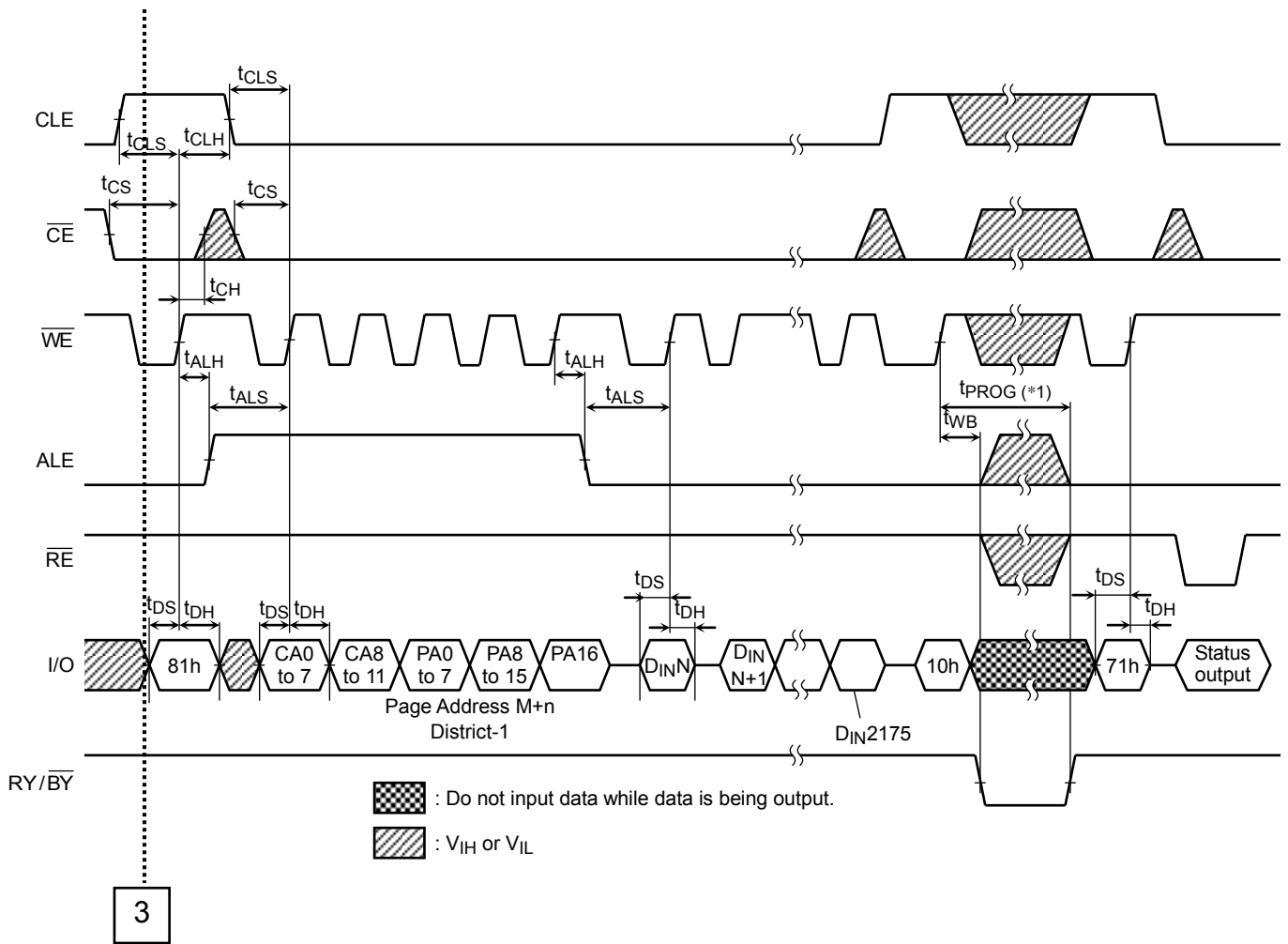
Multi-Page Program Operation with Data Cache Timing Diagram (3/4)



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Multi-Page Program Operation with Data Cache Timing Diagram (4/4)



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(\*1)  $t_{PROG}$ : Since the last page programming by 10h command is initiated after the previous cache program, the  $t_{PROG}$  during cache programming is given by the following equation.

$$t_{PROG} = t_{PROG} \text{ of the last page} + t_{PROG} \text{ of the previous page} - A$$

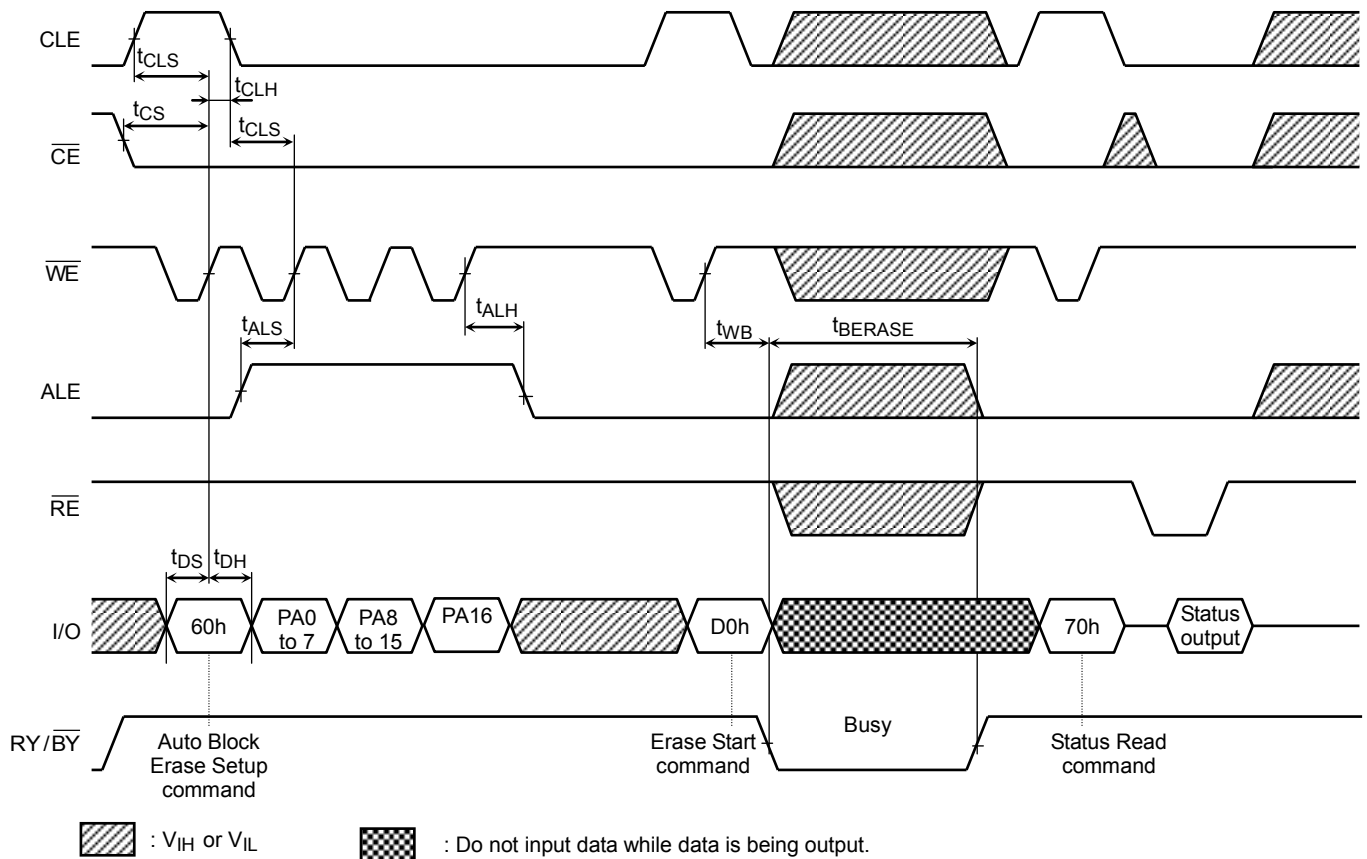
$A = (\text{command input cycle} + \text{address input cycle} + \text{data input cycle time of the last page})$

If "A" exceeds the  $t_{PROG}$  of previous page,  $t_{PROG}$  of the last page is  $t_{PROG} \text{ max}$ .

(Note) Make sure to terminate the operation with 81h-10h- command sequence.  
 If the operation is terminated by 81h-15h command sequence, monitor I/O 6 (Ready / Busy) by issuing Status Read command (70h) and make sure the previous page program operation is completed. If the page program operation is completed issue FFh reset before next operation.



## Auto Block Erase Timing Diagram



Multi Block Erase Timing Diagram

