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## Inverting Voltage Doubler

### Features:

- 99.9% Voltage Conversion Efficiency
- 92% Power Conversion Efficiency
- Wide Input Voltage Range:
  - +2.4V to +5.5V
- Only 3 External Capacitors Required
- 185  $\mu$ A Supply Current
- Space-Saving 8-Pin SOIC and 8-Pin PDIP Packages

### Applications:

- -10V from +5V Logic Supply
- -6V from a Single 3V Lithium Cell
- Portable Handheld Instruments
- Cellular Phones
- LCD Display Bias Generator
- Panel Meters
- Operational Amplifier Power Supplies

### Device Selection Table

| Part Number | Package    | Operating Temp. Range |
|-------------|------------|-----------------------|
| TC682COA    | 8-Pin SOIC | 0°C to +70°C          |
| TC682CPA    | 8-Pin PDIP | 0°C to +70°C          |
| TC682EOA    | 8-Pin SOIC | -40°C to +85°C        |
| TC682EPA    | 8-Pin PDIP | -40°C to +85°C        |

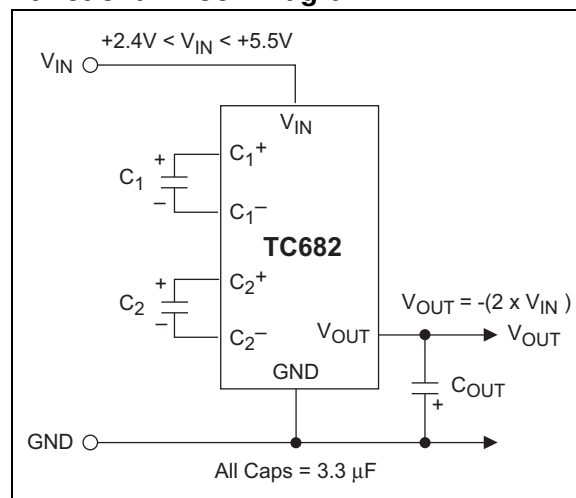
### General Description:

The TC682 is a CMOS charge pump converter that provides an inverted doubled output from a single positive supply. An on-board 12 kHz (typical) oscillator provides the clock and only 3 external capacitors are required for full circuit implementation.

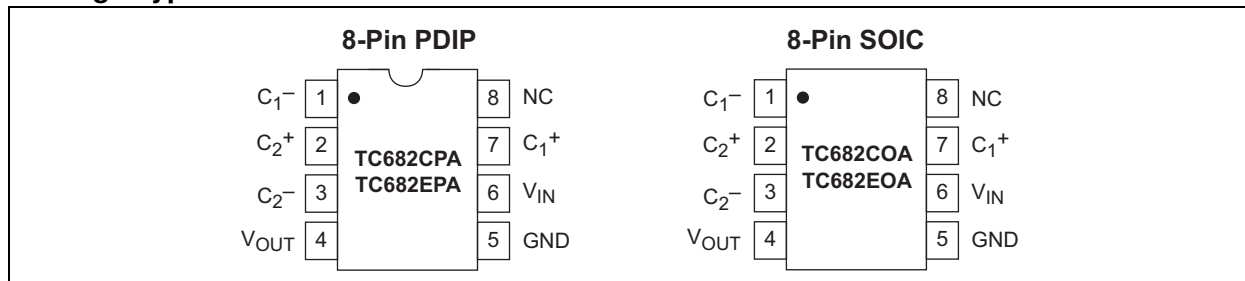
Low output source impedance (typically 140 $\Omega$ ), provides output current up to 10 mA. The TC682 features low quiescent current and high efficiency, making it the ideal choice for a wide variety of applications that require a negative voltage derived from a single positive supply (for example: generation of -6V from a 3V lithium cell or -10V generated from a +5V logic supply).

The minimum external parts count and small physical size of the TC682 make it useful in many medium-current, dual voltage analog power supplies.

### Functional Block Diagram



### Package Type



## 1.0 ELECTRICAL CHARACTERISTICS

### Absolute Maximum Ratings\*

$V_{IN}$  .....+5.8V  
 $V_{IN}$  dV/dT ..... 1V/ $\mu$ sec  
 $V_{OUT}$  .....-11.6V  
 Short-Circuit Duration -  $V_{OUT}$  ..... Continuous  
 Power Dissipation ( $T_A \leq 70^\circ\text{C}$ )  
     8-Pin PDIP .....730 mW  
     8-Pin SOIC .....470 mW  
 Operating Temperature Range.....-40°C to +85°C  
 Storage Temperature (Unbiased) .....-65°C to +150°C

\*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operation sections of the specifications is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

### TC682 ELECTRICAL SPECIFICATIONS

| Electrical Characteristics: Over operating temperature range, $V_{IN} = +5\text{V}$ , test circuit Figure 3-1 unless otherwise noted. |                               |     |      |     |               |   |
|---|-------------------------------|-----|------|-----|---------------|---|
| Symbol  | Parameter                     | Min | Typ  | Max | Units         | Test Conditions                                     |
| $V_{IN}$  | Supply Voltage Range          | 2.4 | —    | 5.5 | V             | $R_L = 2\text{ k}\Omega$                            |
| $I_{IN}$  | Supply Current                | —   | 185  | 300 | $\mu\text{A}$ | $R_L = \infty$ , $T_A = 25^\circ\text{C}$           |
|   |                               | —   | —    | 400 |               | $R_L = \infty$                                      |
| $R_{OUT}$   | $V_{OUT}$ Source Resistance   | —   | 140  | 180 | $\Omega$      | $I_L^- = 10\text{ mA}$ , $T_A = 25^\circ\text{C}$   |
|   |                               | —   | —    | 230 |               | $I_L^- = 10\text{ mA}$                              |
|   |                               |     | 170  | 320 |               | $I_L^- = 5\text{ mA}$ , $V_{IN} = 2.8\text{V}$      |
| $F_{OSC}$   | Oscillator Frequency          | —   | 12   | —   | kHz           |   |
| $P_{EFF}$   | Power Efficiency              | 90  | 92   | —   | %             | $R_L = 2\text{ k}\Omega$ , $T_A = 25^\circ\text{C}$ |
| $V_{OUTEFF}$  | Voltage Conversion Efficiency | 99  | 99.9 | —   | %             | $V_{OUT}$ , $R_L = \infty$                          |

## 2.0 PIN DESCRIPTION

The descriptions of the pins are listed in Table 2-1.

**TABLE 2-1: PIN FUNCTION TABLE**

| Pin No.<br>(8-Pin PDIP,<br>SOIC) | Symbol           | Description                                     |
|----------------------------------|------------------|---|
| 1                                | C1–              | Input. Capacitor C1 negative terminal.          |
| 2                                | C2+              | Input. Capacitor C2 positive terminal.          |
| 3                                | C2–              | Input. Capacitor C2 negative terminal.          |
| 4                                | V <sub>OUT</sub> | Output. Negative output voltage ( $-2V_{IN}$ ). |
| 5                                | GND              | Input. Ground.                                  |
| 6                                | V <sub>IN</sub>  | Input. Power supply voltage.                    |
| 7                                | C1+              | Input. Capacitor C1 positive terminal.          |
| 8                                | NC               | No connection.                                  |

### 3.1 Phase 1

[illegible]

### 3.2 Phase 2

### 3.3 Maximum Operating Limits

### 3.4 Efficiency Considerations

- The charge pump switches have virtually no offset and are extremely low on resistance.
- Minimal power is consumed by the drive circuitry.
- The impedances of the reservoir and pump capacitors are negligible.

$$\begin{aligned}\text{Voltage Efficiency} &= V_{\text{OUT}} / (-2V_{\text{IN}}) \\ V_{\text{OUT}} &= -2V_{\text{IN}} + V_{\text{DROP}} \\ V_{\text{DROP}} &= (I_{\text{OUT}})(R_{\text{OUT}})\end{aligned}$$

$$\text{Power Loss} = I_{\text{OUT}} (V_{\text{DROP}})$$

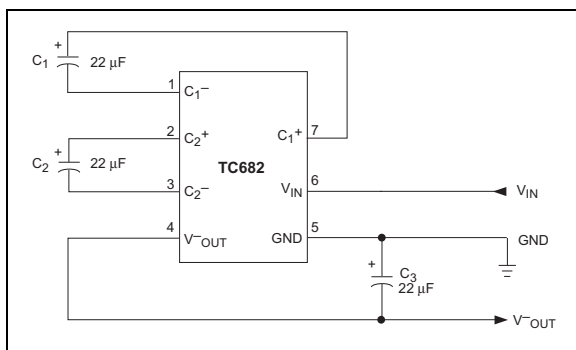
Larger values of reservoir capacitor  $C_3$  will reduce output ripple. Larger values of both pump and reservoir capacitors improve the efficiency. See **Section 4.2 “Capacitor Selection”** “Capacitor Selection”.



## 4.0 TYPICAL APPLICATIONS

### 4.1 Negative Doubling Converter

The most common application of the TC682 is as a charge pump voltage converter which provides a negative output of two times a positive input voltage (Figure 4-1).



**FIGURE 4-1:** Inverting Voltage Doubler

### 4.2 Capacitor Selection

The output resistance of the TC682 is determined, in part, by the ESR of the capacitors used. An expression for  $R_{OUT}$  is derived as shown below:

$$R_{OUT} = 2(R_{SW1} + R_{SW2} + ESR_{C1} + R_{SW3} + R_{SW4} + ESR_{C2}) + 2(R_{SW1} + R_{SW2} + ESR_{C1} + R_{SW3} + R_{SW4} + ESR_{C2}) + 1/(f_{PUMP} \times C1) + 1/(f_{PUMP} \times C2) + ESR_{C3}$$

Assuming all switch resistances are approximately equal:

$$R_{OUT} = 16R_{SW} + 4ESR_{C1} + 4ESR_{C2} + ESR_{C3} + 1/(f_{PUMP} \times C1) + 1/(f_{PUMP} \times C2)$$

$R_{OUT}$  is typically 140Ω at +25°C with  $V_{IN} = +5V$  and 3.3 μF low ESR capacitors. The fixed term ( $16R_{SW}$ ) is about 80-90Ω. It can be seen easily that increasing or decreasing values of C1 and C2 will affect efficiency by changing  $R_{OUT}$ . However, be careful about ESR. This term can quickly become dominant with large electrolytic capacitors. Table 4-1 shows  $R_{OUT}$  for various values of C1 and C2 (assume 0.5Ω ESR). C1 must be rated at 6VDC or greater while C2 and C3 must be rated at 12VDC or greater.

Output voltage ripple is affected by C3. Typically the larger the value of C3 the less the ripple for a given load current. The formula for P-P  $V_{RIPPLE}$  is given below:

$$V_{RIPPLE} = \{1/[2(f_{PUMP} \times C3)] + 2(ESR_{C3})\} (I_{OUT})$$

For a 10 μF (0.5Ω ESR) capacitor for C3,  $f_{PUMP} = 10$  kHz and  $I_{OUT} = 10$  mA the peak-to-peak ripple voltage at the output will be less than 60 mV. In most applications ( $I_{OUT} \leq 10$  mA) a 10-20 μF capacitor and 1-5 μF pump capacitors will suffice. Table 4-2 shows  $V_{RIPPLE}$  for different values of C3 (assume 1Ω ESR).

**TABLE 4-1: OUTPUT RESISTANCE VS. C1, C2**

| C1, C2 (μF) | $R_{OUT}(\Omega)$ |
|-------------|-------------------|
| 0.05        | 4085              |
| 0.10        | 2084              |
| 0.47        | 510               |
| 1.00        | 285               |
| 3.30        | 145               |
| 5.00        | 125               |
| 10.00       | 105               |
| 22.00       | 94                |
| 100.00      | 87                |

**TABLE 4-2:  $V_{RIPPLE}$  PEAK-TO-PEAK VS. C3 ( $I_{OUT} 10mA$ )**

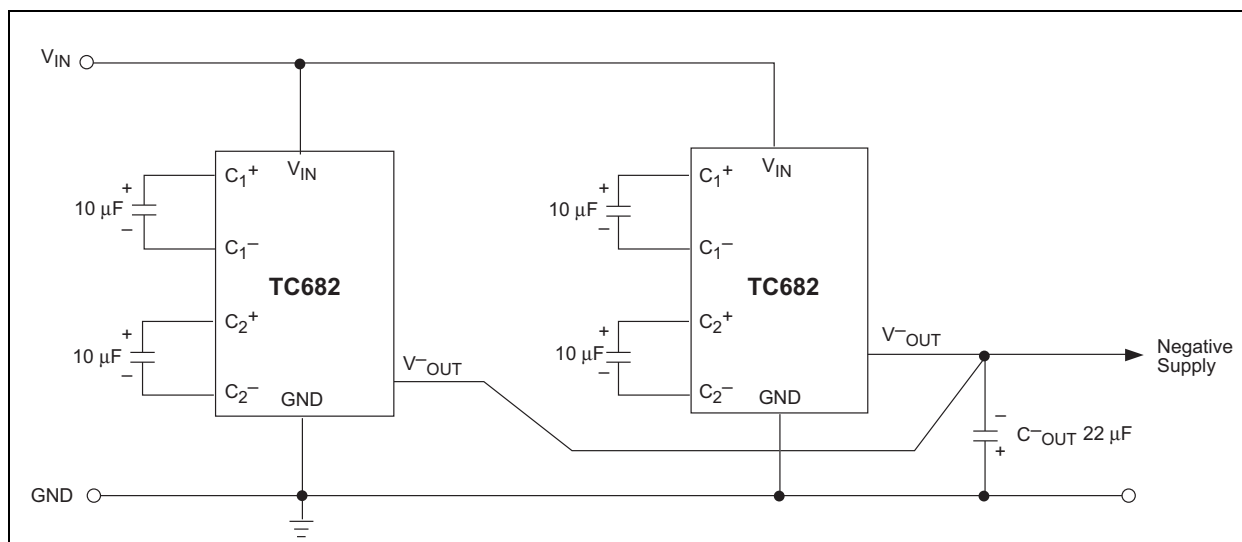
| C3 (μF) | $V_{RIPPLE} (mV)$ |
|---------|-------------------|
| 0.50    | 1020              |
| 1.00    | 520               |
| 3.30    | 172               |
| 5.00    | 120               |
| 10.00   | 70                |
| 22.00   | 43                |
| 100.00  | 25                |

## 4.3 Paralleling Devices

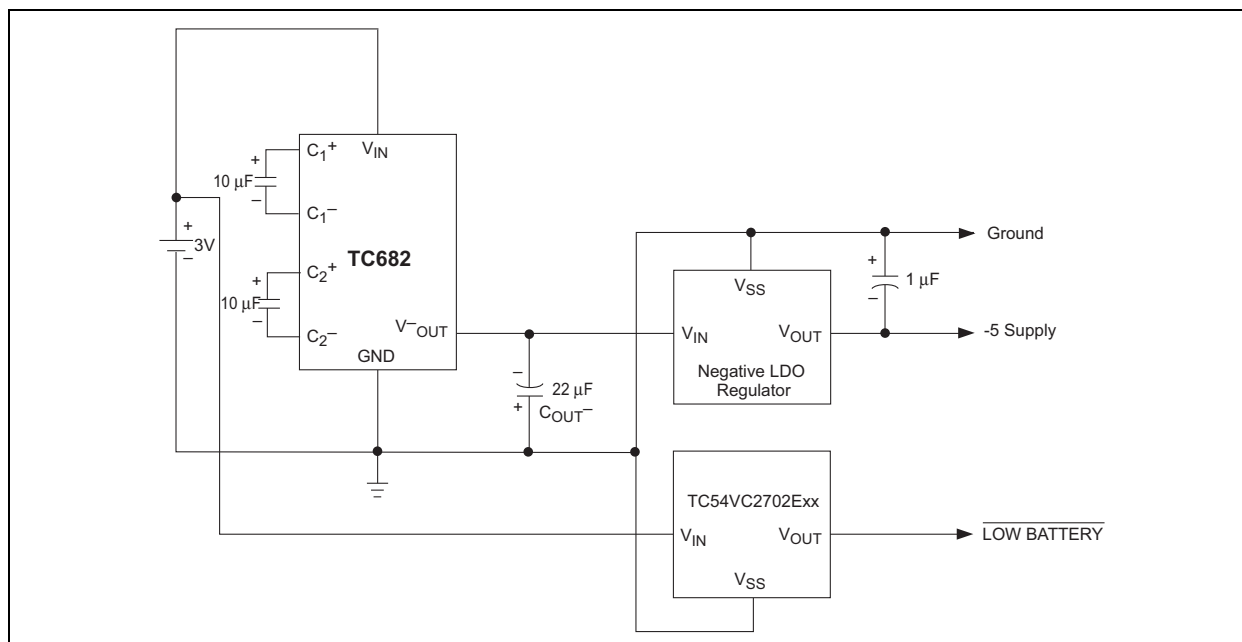
Paralleling multiple TC682s reduces the output resistance of the converter. The effective output resistance is the output resistance of a single device divided by the number of devices. As illustrated in Figure , each requires separate pump capacitors  $C_1$  and  $C_2$ , but all can share a single reservoir capacitor.

## 4.4 -5V Regulated Supply From A Single 3V Battery

Figure 4-3 shows a -5V power supply using one 3V battery. The TC682 provides -6V at  $V_{OUT}$ , which is regulated to -5V by the negative LDO. The input to the TC682 can vary from 3V to 5.5V without affecting regulation appreciably. A TC54 device is connected to the battery to detect undervoltage. This unit is set to detect at 2.7V. With higher input voltage, more current can be drawn from the outputs of the TC682. With 5V at  $V_{IN}$ , 10 mA can be drawn from the regulated output. Assuming  $150\Omega$  source resistance for the converter, with  $I_L^- = 10$  mA, the charge pump will droop 1.5V.



**FIGURE 4-2:** Paralleling TC682 for Lower Output Source Resistance

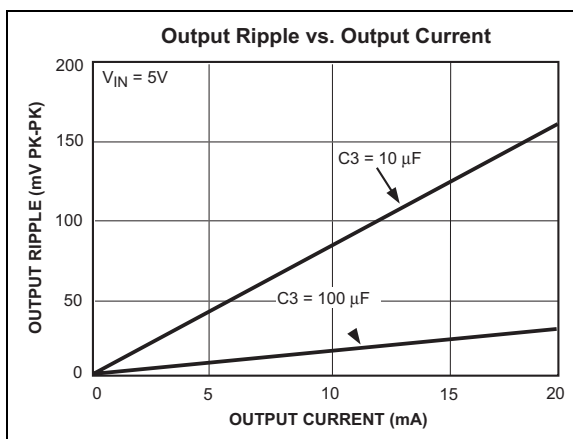
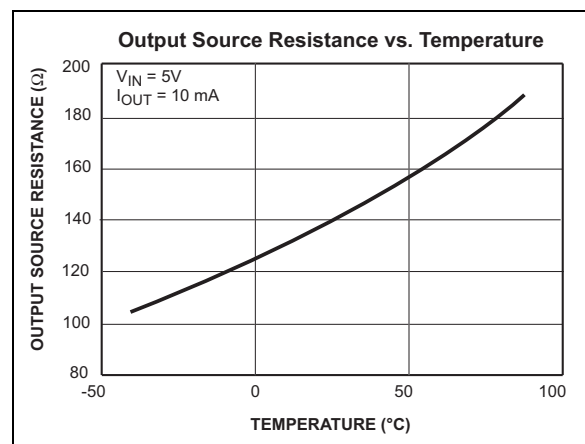
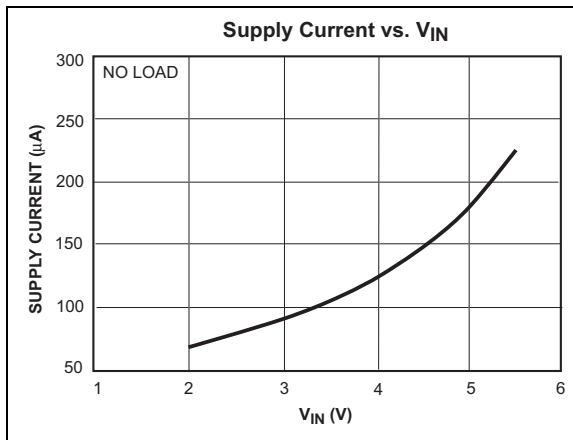
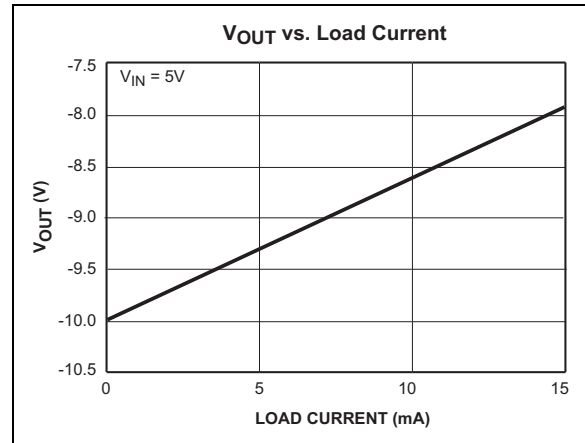
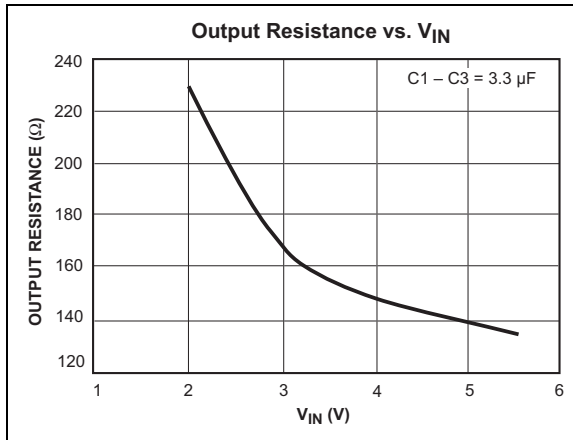


**FIGURE 4-3:** Negative Supply Derived from 3V Battery

## 5.0 TYPICAL CHARACTERISTICS

**Note:** The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

Circuit of Figure 3-1,  $C_1 = C_2 = C_{OUT} = 3.3 \mu F$ ,  $T_A = 25^\circ C$  unless otherwise noted.



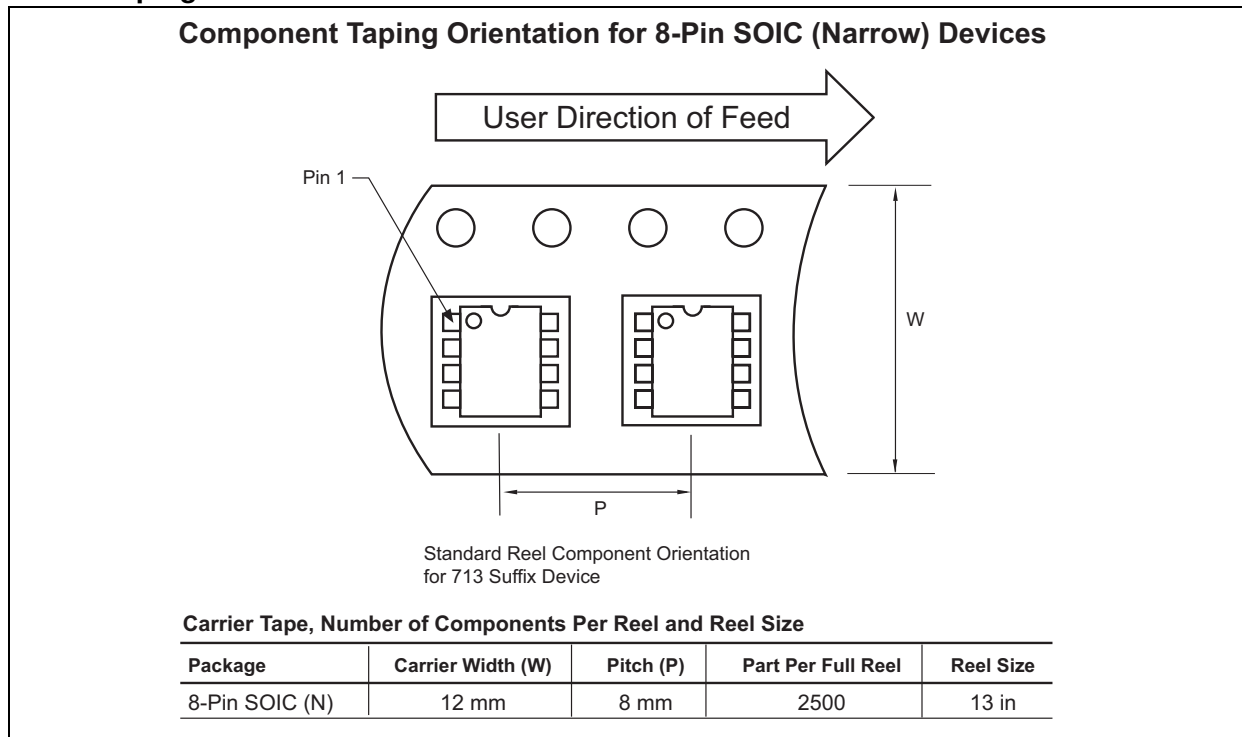


## 6.0 PACKAGING INFORMATION

### 6.1 Package Marking Information

Package marking data not available at this time.

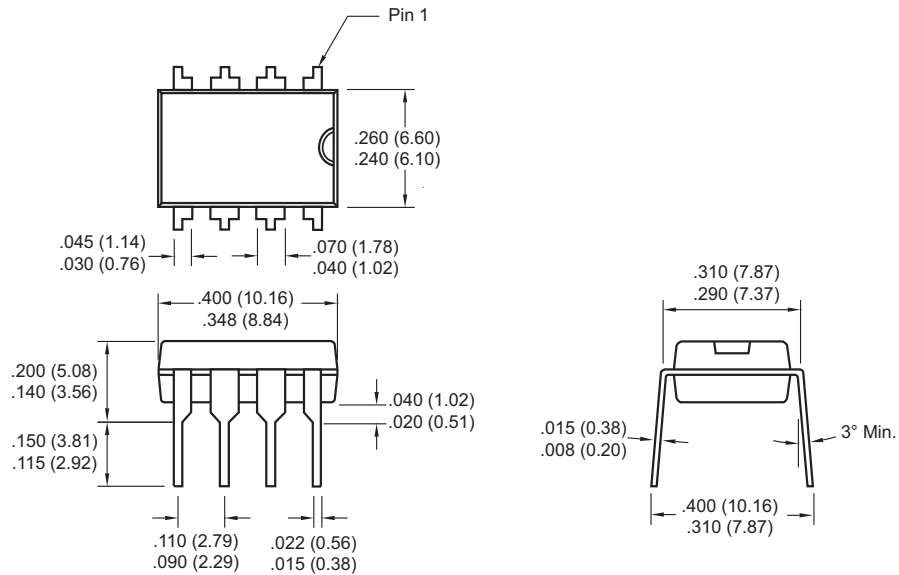
### 6.2 Taping Form



## 6.3 Package Dimensions

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>

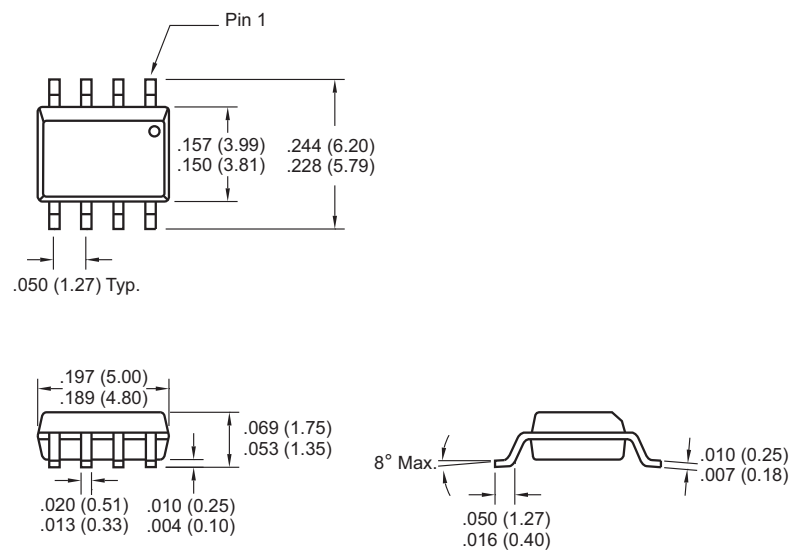
### 8-Pin Plastic DIP



Dimensions: inches (mm)

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>

### 8-Pin SOIC



Dimensions: inches (mm)

## 7.0 REVISION HISTORY

### Revision D

Added a note to each package outline drawing.

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