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Obsolete Device

TC820

3-3/4 Digit A/D Converter with Frequency Counter and Logic Probe

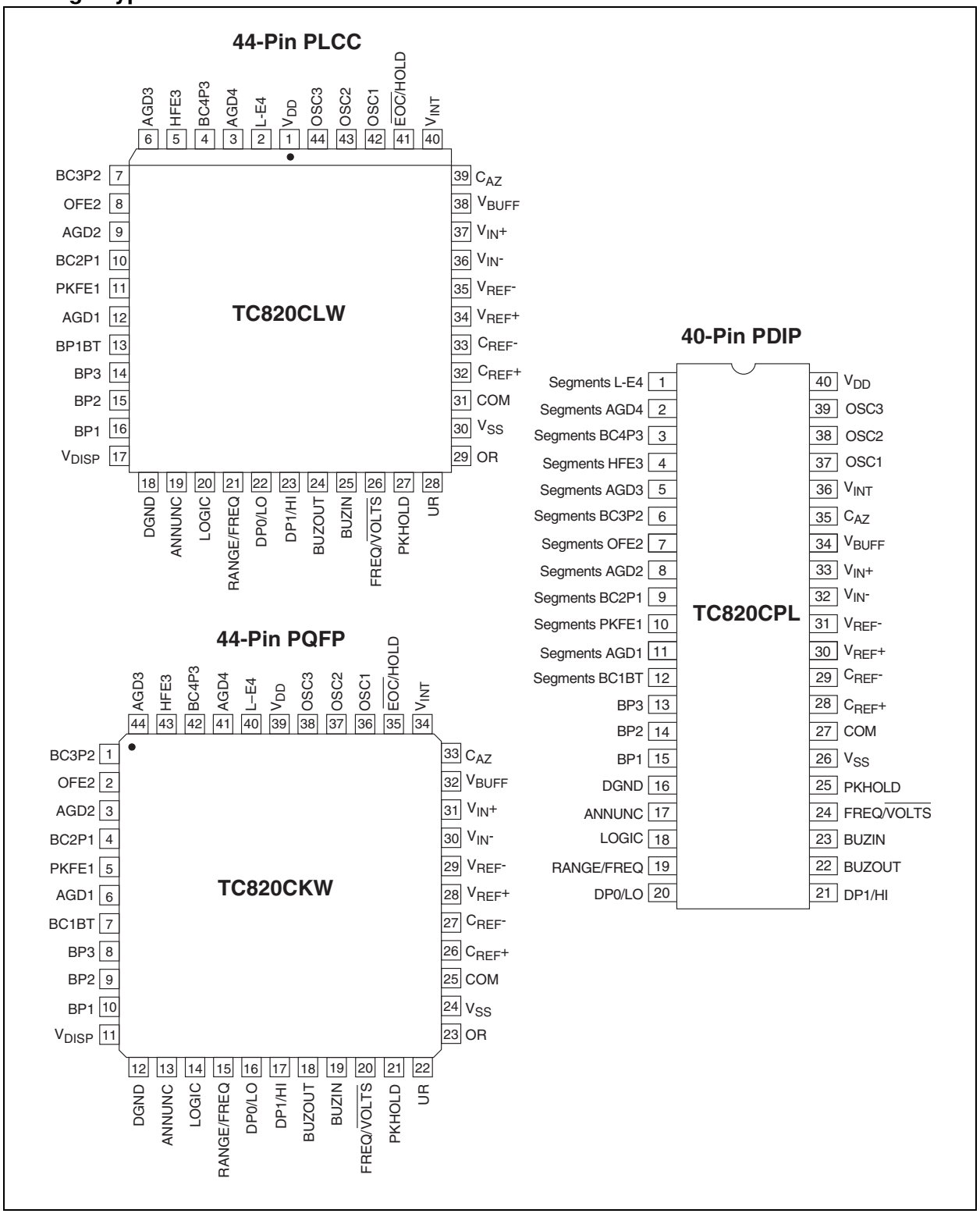
Features

- Multiple Analog Measurement System
  - Digit A/D Converter
  - Frequency Counter
  - Logic Probe
- Low Noise A/D Converter:
  - Differential Inputs: (1 pA Bias Current)
  - On-Chip 50 ppm/°C Voltage Reference
- Frequency Counter:
  - 4 MHz Maximum Input Frequency
  - Auto-Ranging Over Four Decade Range
- Logic Probe:
  - Two LCD Annunciators
  - Buzzer Driver
- 3-3/4 Digit Display with Over Range Indicator
- LCD Display Driver with Built-in Contrast Control
- Data Hold Input for Comparison Measurements
- Low Battery Detect with LCD Annunciator
- Under Range and Over Range Outputs
- On-Chip Buzzer Driver with Control Input
- 40-Lead Plastic DIP, 44-Lead Plastic Flat Pack, or 44-Lead PLCC Packages

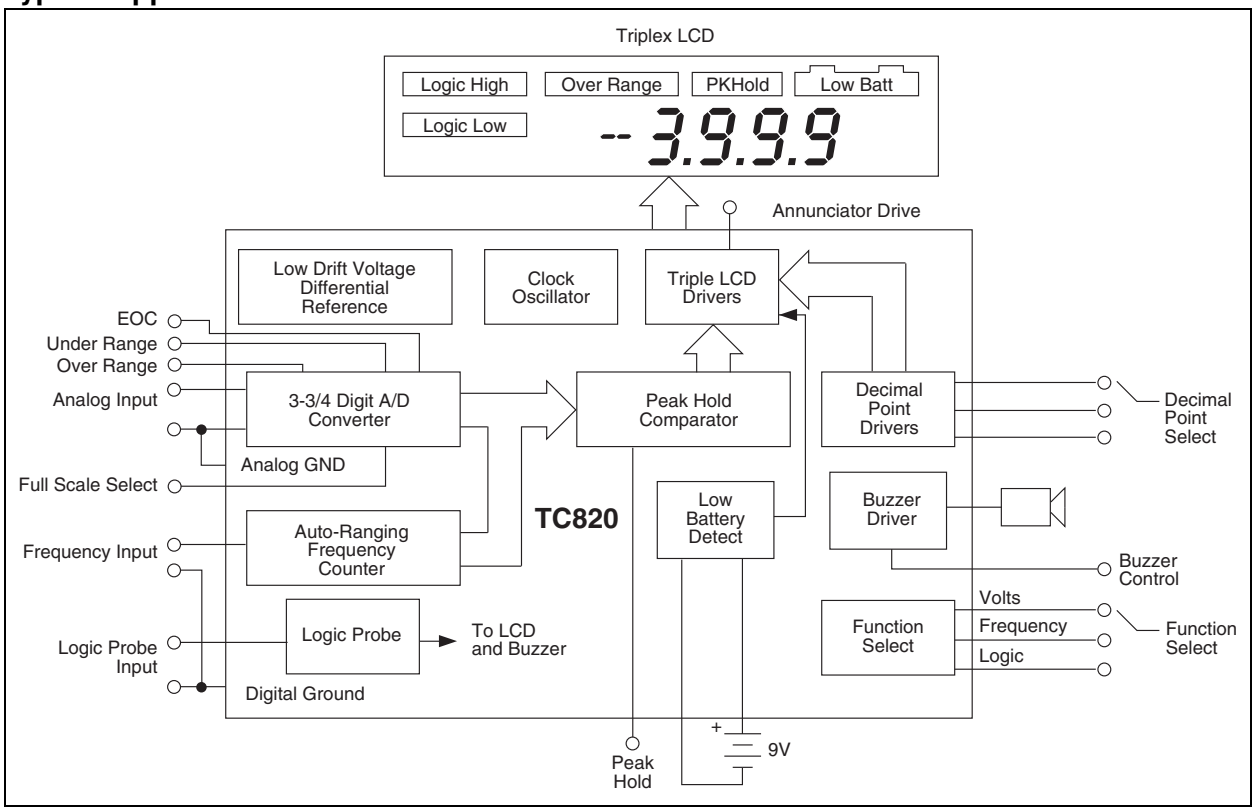
General Description

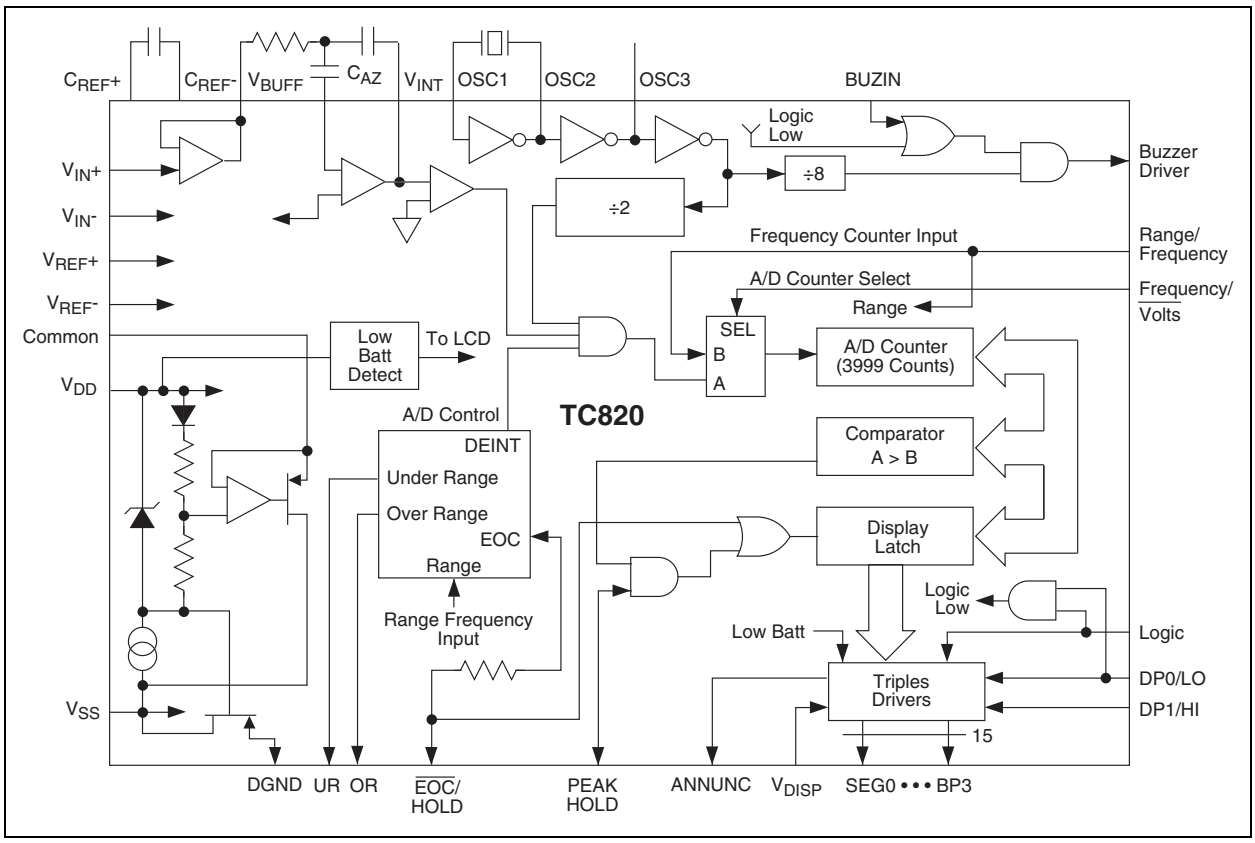
The TC820 is a 3-3/4 digit, multi-measurement system especially suited for use in portable instruments. It integrates a dual slope A/D converter, auto-ranging frequency counter and logic probe into a single 44-pin surface mount, or 40-pin through hole package. The operates from a single 9V input voltage (battery) and features a built-in battery low flag. Function and decimal point selection are accomplished with simple logic inputs designed for direct connection to an external microcontroller or rotary switch.

Package Type:



Typical Applications





1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings*

Supply Voltage (V_{DD} to GND) 15V
Analog Input Voltage:
(Either Input) **(Note 1)** ..... V_{DD} to V_{SS}
Reference Input Voltage (Either Input) ..... V_{DD} to V_{SS}
Digital Inputs ..... V_{DD} to DGND
V_{DISP} ..... V_{DD} to (DGND – 0.3V)
Package Power Dissipation (T_A – 70°C) **(Note 2)**:
40-Lead Plastic DIP 1.23W
44-Lead PLCC 1.23W
44-Lead Plastic Flat Package (PQFP) 1.00W
Operating Temperature Range:
"C" Devices .....0°C to +70°C
"E" Devices .....-40°C to +85°C
Storage Temperature Range .....-65°C to +150°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operation sections of the specifications is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

Electrical Characteristics: Unless otherwise specified, V_{SS} = 9V, T_A = +25°C

Parameter	Sym	Min	Typ	Max	Units	Test Conditions
Zero Input Reading		-000	±000	+000	Digital Reading	V_{IN} = 0V Full Scale = 400 mV
Rollover Error	RE	-1	±0.2	+1	Counts	V_{IN} = ±390 mV Full Scale = 400 mV
Nonlinearity (Maximum Deviation From Best Straight Line Fit)	NL	-1	±0.2	+1	Count	Full Scale = 400 mV
Ratiometric Reading		1999	1999/2000	2000	—	$V_{IN} = V_{REF}$
Common Mode Rejection Ratio	CMRR	—	50	—	µV/V	V_{CM} = ±1V, V_{IN} = 0V Full Scale = 400 mV (V_{FS} = 200 mV)
Common Mode Voltage Range	VCMR	V_{SS} + 1.5	—	V_{DD} – 1		Input High, Input Low
Noise (P-P Value Not Exceeded 95% of Time)	e_N	—	15	—	µV	V_{IN} = 0V Full Scale = 400 mV
Input Leakage Current	I_{IN}	—	—	—	—	V_{IN} = 0V
		—	1	10	pA	T_A = +25°C
		—	20	—	pA	0°C ≤ T_A ≤ +70°C
		—	100	—	pA	-40°C ≤ T_A ≤ +85°C
Analog Common Voltage	V_{COM}	3.15	3.3	3.45	V	25 kΩ between Common and V_{DD} (V_{SS} - V_{COM})
Common Voltage Temperature Coefficient	V_{CTC}	—	—	—	—	25 kΩ Between Common and V_{DD}
		—	35	50	ppm/°C	0°C ≤ T_A ≤ +70°C
		—	50	—	—	-40°C ≤ T_A ≤ +85°C
Zero Reading Drift	TC_{ZS}	—	—	—	—	V_{IN} = 0V
		—	0.2	—	—	0°C ≤ T_A ≤ +70°C
		—	1	—	—	-40°C ≤ T_A ≤ +85°C

Note 1: Input voltages may exceed the supply voltages provided that input current is limited to ±100 µA. Current above this value may result in invalid display readings, but will not destroy the device if limited to ±1 mA.

2: Dissipation ratings assume device is mounted with all leads soldered to printed circuit board.

ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical Characteristics: Unless otherwise specified, V_{SS} = 9V, T_A = +25°C

Parameter	Sym	Min	Typ	Max	Units	Test Conditions
Scale Factor Temperature Coefficient	TC_{FS}	—	—	—	—	V_{IN} = 399 mV
		—	1	5	ppm/°C	0°C ≤ T_A ≤ +70°C
		—	5	—	ppm/°C	-40°C ≤ T_A ≤ +85°C Ext Ref = 0 ppm/°C
Supply Current	I_S	—	1	1.5	mA	V_{IN} = 0V
Peak-to-Peak Backplane Drive Voltage		4.25	4.7	5.3	V	V_S = 9V V_{DISP} = DGND
Buzzer Frequency		—	5	—	kHz	F_{OSC} = 40 kHz
Counter TIme-Base Period		—	1	—	Second	F_{OSC} = 40 kHz
Low Battery Flag Voltage		6.7	7	7.3	V	V_{DD} to V_{SS}
Input Low Voltage	V_{IL}	—	—	DGND + 1.5	V	
Input High Voltage	V_{IH}	V_{DD} – 1.5	—	—	V	
Output Low Voltage, UR, OR Outputs	V_{OL}	V_{DD} – 1.5	—	DGND + 0.4	V	I_L = 50 µA
Control Pin Pull-down Current		—	5	—	µA	V_{IN} = V_{DD}

Note 1: Input voltages may exceed the supply voltages provided that input current is limited to ±100 µA. Current above this value may result in invalid display readings, but will not destroy the device if limited to ±1 mA.

2: Dissipation ratings assume device is mounted with all leads soldered to printed circuit board.

2.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 2-1.

TABLE 2-1: PIN FUNCTION TABLE

Pin Number (40-PDIP)	Pin Number (44-PQFP)	Symbol	Description
1	40	L-E4	LCD segment driver for L ("logic LOW"), polarity, and "e" segment of most significant digit (MSD).
2	41	AGD4	LCD segment drive for "a," "g," and "d" segments of MSD.
3	42	BC4P3	LCD segment drive for "b" and "c" segments of MSD and decimal point 3.
4	43	HFE3	LCD segment drive for H ("logic HIGH"), and "f" and "e" segments of third LSD.
5	44	AGD3	LCD segment drive for "a," "g," and "d" segments of third LSD.
6	1	BC3P2	LCD segment drive for "b" and "c" segments of third LSD and decimal point 2.
7	2	OFE2	LCD segment drive for "over range," and "f" and "e" segments of second LSD.
8	3	AGD2	LCD segment drive for "a," "g," and "d" segments of second LSD.
9	4	BC2P1	LCD segment drive for "b " and "c" segments of second LSD and decimal point 1.
10	5	PKFE1	LCD segment drive for "hold peak reading," and "f" and "e" segments of LSD.
11	6	AGD1	LCD segment drive for "a," "g," and "d" segments of LSD.
12	7	BC1BT	LCD segment drive for "b" and "c" segments of LSD and "low battery."
13	8	BP3	LCD backplane #3.
14	9	BP2	LCD backplane #2.
15	10	BP1	LCD backplane #1.
—	11	V_{DISP}	Sets peak LCD drive signal: $V_{PEAK} = (V_{DD}) - V_{DISP}$. V_{DISP} may also be used to compensate for temperature variation of LCD crystal threshold voltage.
16	12	DGND	Internal logic digital ground, the logic "0" level. Nominally 4.7V below V_{DD}.
17	13	ANNUNC	Square-wave output at the backplane frequency, synchronized to BP1. ANNUNC can be used to control display annunciators. Connecting an LCD segment to ANNUNC turns it on; connecting it to its backplane turns it off.
18	14	LOGIC	Logic mode control input. When connected to V_{DD}, the converter is in Logic mode. The LCD displays "OL" and the decimal point inputs control the HIGH and LOW annunciators. When the "low" annunciator is on, the buzzer will also be on. When unconnected or connected to DGND, the is in the Voltage/Frequency Measurement mode. This pin has a 5 µA internal pull-down to DGND.
19	15	RANGE/ FREQ	Dual purpose input. In Range mode, when connected to V_{DD}, the integration time will be 200 counts instead of 2000 counts.
20	16	DP0/LO	Dual purpose input. Decimal point select input for voltage measurements. In logic mode, connecting this pin to V_{DD} will turn on the "low" LCD segment. There is an internal 5 µA pull-down to DGND in Volts mode only. Decimal point logic:
21	17	DP1/HI	Dual purpose input. Decimal point select input for voltage measurements. In Logic mode, connecting this pin to V_{DD} will turn on the "high" LCD segment. There is an internal 5 µA pull-down to DGND in Volts mode only.
22	18	BUZOUT	Buzzer output. Audio frequency, 5kHz, output which drives a piezoelectric buzzer.
23	19	BUZIN	Buzzer control input. Connecting BUZIN to V_{DD} turns the buzzer on. BUZIN is logically OR'ed (internally) with the "logic level low" input. There is an internal 5 µA pull-down to DGND.

DP1	DPQ	Decimal Point Selected
0	0	None
0	1	DP1
1	0	DP2
1	1	DP3

TABLE 2-1: PIN FUNCTION TABLE (CONTINUED)

Pin Number (40-PDIP)	Pin Number (44-PQFP)	Symbol	Description
24	20	$\overline{\text{FREQ}}$/VOLTS	Voltage or frequency measurement select input. When unconnected, or connected VOLTS to DGND, the A/D converter function is active. When connected to V_{DD}, the frequency counter function is active. This pin has an internal 5 μA pull-down to DGND.
25	21	PKHOLD	Peak hold input. When connected to V_{DD}, the converter will only update the display if a new conversion value is greater than the preceding value. Thus, the peak reading will be stored and held indefinitely. When unconnected, or connected to DGND, the converter will operate normally. This pin has an internal 5 μA pull-down to DGND.
—	22	UR	Under range output. This output will be HIGH when the digital reading is 380 counts or less.
—	23	OR	Over range output. This output will be HIGH when the analog signal input is greater than full scale. The LCD will display "OL" when the input is over ranged.
26	24	V_{SS}	Negative supply connection. Connect to negative terminal of 9V battery.
27	25	COM	Analog circuit ground reference point. Nominally 3.3V below V_{DD}.
28	26	C_{REF}+	Positive connection for reference capacitor.
29	27	C_{REF}-	Negative connection for reference capacitor.
30	28	V_{REF}+	High differential reference input connection.
31	29	V_{REF}-	Low differential reference input connection.
32	30	V_{IN}-	Low analog input signal connection.
33	31	V_{IN}+	High analog input signal connection.
34	32	V_{BUFF}	Buffer output. Connect to integration resistor.
35	33	C_{AZ}	Auto-zero capacitor connection.
36	34	V_{INT}	Integrator output. Connect to integration capacitor.
—	35	$\overline{\text{EOC}}$/HOLD	Bi-directional pin. Pulses low (i.e., from V_{DD} to DGND) at the end of each conversion. If connected to V_{DD}, conversions will continue, but the display is not updated.
37	36	OSC1	Crystal oscillator (input) connection.
38	37	OSC2	Crystal oscillator (output) connection.
39	38	OSC3	RC oscillator connection.
40	39	V_{DD}	LCD segment drive for "a," "g," and "d" segments of MSD.

3.0 DETAILED DESCRIPTION

The is a 3-3/4 digit measurement system combining an integrating analog-to-digital converter, frequency counter, and logic level tester in a single package. The TC820 supersedes the TC7106 in new designs by improving performance and reducing system cost. The TC820 adds features that are difficult, expensive, or impossible to provide with older A/D converters (see Table 3-1). The high level of integration permits TC820 based instruments to deliver higher performance and more features, while actually reducing parts count. Fabricated in low power CMOS, the TC820 directly drives a 3-3/4 digit (3999 maximum) LCD.

With a maximum range of 3999 counts, the TC820 provides 10 times greater resolution in the 200 mV to 400 mV range than traditional 3-1/2 digit meters. An auto-zero cycle ensures a zero reading with a 0V input. CMOS processing reduces analog input bias current to only 1 pA. Rollover error (the difference in readings for equal magnitude but opposite polarity input signals) is less than ±1 count. Differential reference inputs permit ratiometric measurements for ohms or bridge transducer applications.

The TC820's frequency counter option simplifies design of an instrument well-suited to both analog and digital troubleshooting: voltage, current, and resistance measurements, plus precise frequency measurements to 4MHz (higher frequencies can be measured with an external prescaler), and a simple logic probe. The frequency counter will automatically adjust its range to match the input frequency, over a four-decade range.

Two logic level measurement inputs permit a TC820 based meter to function as a logic probe. When combined with external level shifters, the TC820 will display logic levels on the LCD and also turn on a piezoelectric buzzer when the measured logic level is low.

Other TC820 features simplify instrument design and reduce parts count. On-chip decimal point drivers are included, as is a low battery detection annunciator. A piezoelectric buzzer can be controlled with an external switch or by the logic probe inputs. Two oscillator options are provided: a crystal can be used if high accuracy frequency measurements are desired, or a simple RC option can be used for low-end instruments.

A "peak reading hold" input allows the TC820 to retain the highest A/D or frequency reading. This feature is useful in measuring motor starting current, maximum temperature, and similar applications.

A family of instruments can be created with the TC820. No additional design effort is required to create instruments with 3-3/4 digit resolution.

The TC820 operates from a single 9V battery, with typical power of 10mW. Packages include a 40-lead plastic DIP, 44-lead plastic flat package (PQFP), and 44-lead PLCC.

TABLE 3-1: COMPETITIVE EVALUATION

Features Comparison	TC820	7106
3-3/4 Digit Resolution	Yes	No
Auto-Ranging Frequency Counter	Yes	No
Logic Probe	Yes	No
Decimal Point Drive	Yes	No
Peak Reading Hold **(Frequency or Voltage)**	Yes	No
Display Hold	Yes	No
Simple 10:1 Range Change	Yes	No
Buzzer Drive	Yes	No
Low Battery Detection with Annunciator	Yes	No
Over Range Detection with Annunciator	Yes	No
Low Drift Reference	Yes	No
Under Range/Over Range Logic Output	Yes	No
Input Overload Display	"OL"	"1"
LCD Annunciator Driver	Yes	No
LCD Drive Type	Triplexed	Direct
LCD Pin Connections	15	24
LCD Elements	36	23

3.1 General Theory of Operation

3.1.1 DUAL SLOPE CONVERSION PRINCIPLES

The TC820 analog-to-digital converter operates on the principle of dual slope integration. An understanding of the dual slope conversion technique will aid the user in following the detailed TC820 theory of operation following this section. A conventional dual slope converter measurement cycle has two distinct phases:

1. Input Signal Integration.
2. Reference Voltage Integration (De-integration).

Referring to Figure 3-1, the unknown input signal to be converted is integrated from zero for a fixed time period (t_{INT}), measured by counting clock pulses. A constant reference voltage of the opposite polarity is then integrated until the integrator output voltage returns to zero. The reference integration (de-integration) time (t_{DEINT}) is then directly proportional to the unknown input voltage (V_{IN}).

In a simple dual slope converter, a complete conversion requires the integrator output to "ramp-up" from zero and "ramp-down" back to zero. A simple mathematical equation relates the input signal, reference voltage, and integration time.

EQUATION 3-1:

$$\frac{1}{R_{INT}C_{INT}}\int_0^{t_{INT}} V_{IN}(t)dt = \frac{V_{REF}t_{DEINT}}{R_{INT}C_{INT}}$$

Where: V_{REF} = Reference Voltage
t_{INT} = Integration Time
t_{DEINT} = De-integration Time

For a constant V_{INT}:

EQUATION 3-2:

$$V_{IN} = V_{REF}\frac{t_{DEINT}}{t_{INT}}$$

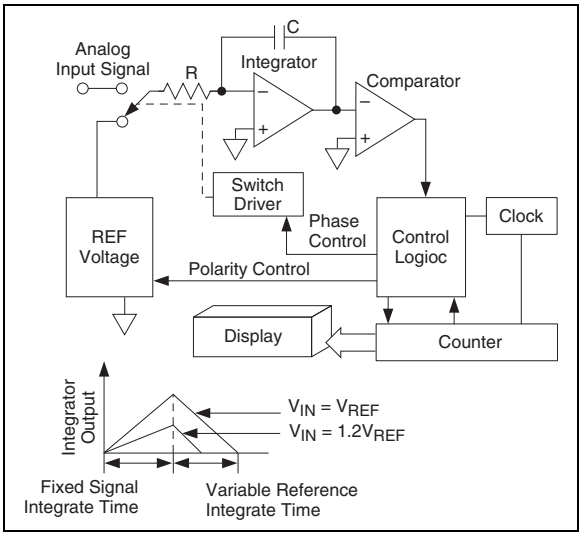


FIGURE 3-1: *Basic Dual Slope Converter.*

Accuracy in a dual slope converter is unrelated to the integrating resistor and capacitor values as long as they are stable during a measurement cycle. An inherent benefit of the dual slope technique is noise immunity. Noise spikes are integrated or averaged to zero during the integration periods, making integrating ADCs immune to the large conversion errors that plague successive approximation converters in high noise environments. Interfering signals, with frequency components at multiples of the averaging (integrating) period, will be attenuated (Figure 3-2). Integrating ADCs commonly operate with the signal integration period set to a multiple of the 50/60Hz power line period.

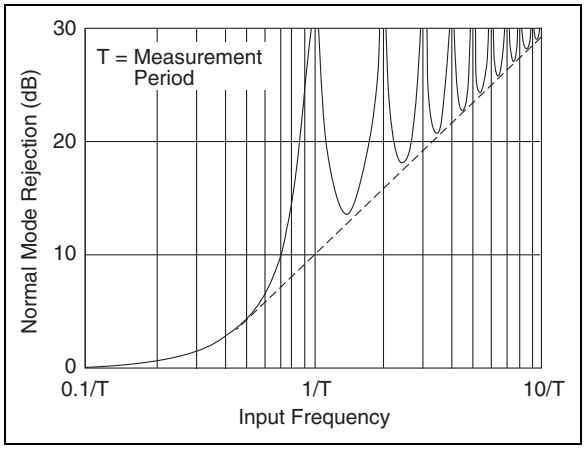


FIGURE 3-2: *Normal Mode Rejection of Dual Slope Converter.*

3.2 Analog Section

In addition to the basic integrate and de-integrate dual slope phases discussed above, the TC820 design incorporates a "zero integrator output" phase and an "auto-zero" phase. These additional phases ensure that the integrator starts at 0V (even after a severe over range conversion), and that all offset voltage errors (buffer amplifier, integrator and comparator) are removed from the conversion. A true digital zero reading is assured without any external adjustments.

A complete conversion consists of four distinct phases:

1. Zero Integrator Output.
2. Auto-Zero.
3. Signal Integrate.
4. Reference De-integrate.

3.2.1 ZERO INTEGRATOR OUTPUT PHASE

This phase guarantees that the integrator output is at 0V before the system zero phase is entered, ensuring that the true system offset voltages will be compensated for even after an over range conversion. The duration of this phase is 500 counts plus the unused de-integrate counts.

3.2.2 AUTO-ZERO PHASE

During the auto-zero phase, the differential input signal is disconnected from the measurement circuit by opening internal analog switches, and the internal nodes are shorted to Analog Common ($0V_{REF}$) to establish a zero input condition. Additional analog switches close a feedback loop around the integrator and comparator to permit comparator offset voltage error compensation. A voltage established on C_{AZ} then compensates for internal device offset voltages during the measurement cycle. The auto-zero phase residual is typically 10 µV to 15 mV. The auto-zero duration is 1500 counts.

3.2.3 SIGNAL INTEGRATION PHASE

Upon completion of the auto-zero phase, the auto-zero loop is opened and the internal differential inputs connect to $V_{IN}+$ and $V_{IN}-$. The differential input signal is then integrated for a fixed time period, which is 2000 counts (4000 clock periods). The externally set clock frequency is divided by two before clocking the internal counters.

The integration time period is:

EQUATION 3-3:

$$t_{INT} = \frac{4000}{F_{OSC}}$$

The differential input voltage must be within the device's Common mode range when the converter and measured system share the same power supply common (ground). If the converter and measured system do not share the same power supply common, as in battery powered applications, $V_{IN}-$ should be tied to analog common.

Polarity is determined at the end of signal integration phase. The sign bit is a "true polarity" indication, in that signals less than 1LSB are correctly determined. This allows precision null detection that is limited only by device noise and auto-zero residual offsets.

3.2.4 REFERENCE INTEGRATE (DE-INTEGRATE) PHASE

The reference capacitor, which was charged during the auto-zero phase, is connected to the input of the integrating amplifier. The internal sign logic ensures the polarity of the reference voltage is always connected in the phase opposite to that of the input voltage. This causes the integrator to ramp back to zero at a constant rate, determined by the reference potential.

The amount of time required (t_{DEINT}) for the integrating amplifier to reach zero is directly proportional to the amplitude of the voltage that was put on the integrating capacitor (V_{INT}) during the integration phase.

EQUATION 3-4:

$$t_{DEINT} = \frac{R_{INT}C_{INT}V_{INT}}{V_{REF}}$$

The digital reading displayed by the TC820 is:

$$Digital\ Count = 2000\ \frac{V_{IN}+V_{IN}-}{V_{REF}}$$

The oscillator frequency is divided by 2 prior to clocking the internal decade counters. The four-phase measurement cycle takes a total of 8000 (4000) counts or 16,000 clock pulses. The 8000 count phase is independent of input signal magnitude or polarity.

Each phase of the measurement cycle has the following length:

TABLE 3-2: MEASUREMENT CYCLE PHASE LENGTH

Conversion Phase	Counts
1) Auto-Zero	1500
2) Signal Integrate **(Notes 1, 2)**	2000
3) Reference Integrate	1 to 4001
4) Integrator Output Zero	499 to 4499

Note 1: This time period is fixed. The integration period for theTC820 is: INT (TC820) = $4000/F_{OSC}$ = 2000 counts. Where F_{OSC} is the clock oscillator frequency.

2: Times shown are the RANGE/FREQ at logic low (normal operation). When RANGE/FREQ is logic high, signal integrate times are 200 counts. See **Section 3.2.7 "10:1 Range Change"**.

3.2.5 INPUT OVER RANGE

When the analog input is greater than full scale, the LCD will display "OL" and the "OVER RANGE" LCD annunciator will be on.

3.2.6 PEAK READING HOLD

The TC820 provides the capability of holding the highest (or peak) reading. Connecting the PK HOLD input to V_{DD} enables the peak hold feature. At the end of each conversion, the contents of the TC820 counter are compared to the contents of the display register. If the new reading is higher than the reading being displayed, the higher reading is transferred to the display register. A "higher" reading is defined as the reading with the higher absolute value.

The peak reading is held in the display register, so the reading will not "droop" or slowly decay with time. The held reading will be retained until a higher reading occurs, the PK HOLD input is disconnected from V_{DD}, or power is removed.

The peak signal to be measured must be present during the TC820 signal integrate period. The TC820 does not perform transient peak detection of the analog input signal. However, in many cases, such as measuring temperature or electric motor starting current, the TC820 "acquisition time" will not be a limitation. If true peak detection is required, a simple circuit will suffice. See the applications section for details.

The peak reading function is also available when the TC820 is in the Frequency Counter mode. The counter auto-ranging feature is disabled when peak reading hold is selected.

3.2.7 10:1 RANGE CHANGE

The analog input full scale range can be changed with the RANGE/FREQ input. Normally, RANGE/FREQ is held low by an internal pull-down. Connecting this pin to V_S+ will increase the full scale voltage by a factor of 10. No external component changes are required.

The RANGE/FREQ input operates by changing the integrate period. When RANGE/FREQ is connected to V_{DD}, the signal integration phase of the conversion is reduced by a factor of 10 (i.e., from 2000 counts to 200 counts).

For the TC820, the 10:1 range change will result in ±4V full scale. This full scale range will exceed the Common mode range of the input buffer when operating from a 9V battery. If range changing is required for the TC820, a higher supply voltage can be provided, or the input voltage can be divided by 2 externally.

3.3 Frequency Counter

In addition to serving as an analog-to-digital converter, the TC820 internal counter can also function as a frequency counter (Figure 3-3). In the Counter mode, pulses at the RANGE/FREQ input will be counted and displayed.

The frequency counter derives its time-base from the clock oscillator. The counter time-base is:

EQUATION 3-5:

$$t_{COUNT} = \frac{F_{OSC}}{40{,}000}$$

Thus, the counter will operate with a 1-second time-base when a 40 kHz oscillator is used. The frequency counter accuracy is determined by the oscillator accuracy. For accurate frequency measurements, a crystal oscillator is recommended.

The frequency counter will automatically select the proper range. Auto-range operation extends over four decades, from 3.999 kHz to 3.999 MHz. Decimal points are set automatically in the Frequency mode (Figure 3-2). The logic switching levels of the RANGE/FREQ input are CMOS levels. For best counter operation, an external buffer is recommended. See the applications section for details.

3.4 Logic Probe

The TC820 can also function as a simple logic probe (Figure 3-5). This mode is selected when the LOGIC input is high. Two dual purpose pins, which normally control the decimal points, are used as logic inputs. Connecting either input to a logic high level will turn on the corresponding LCD annunciator. When the "low" annunciator is on, the buzzer will be on. As with the frequency counter input, external level shifters/buffers are recommended for the logic probe inputs.

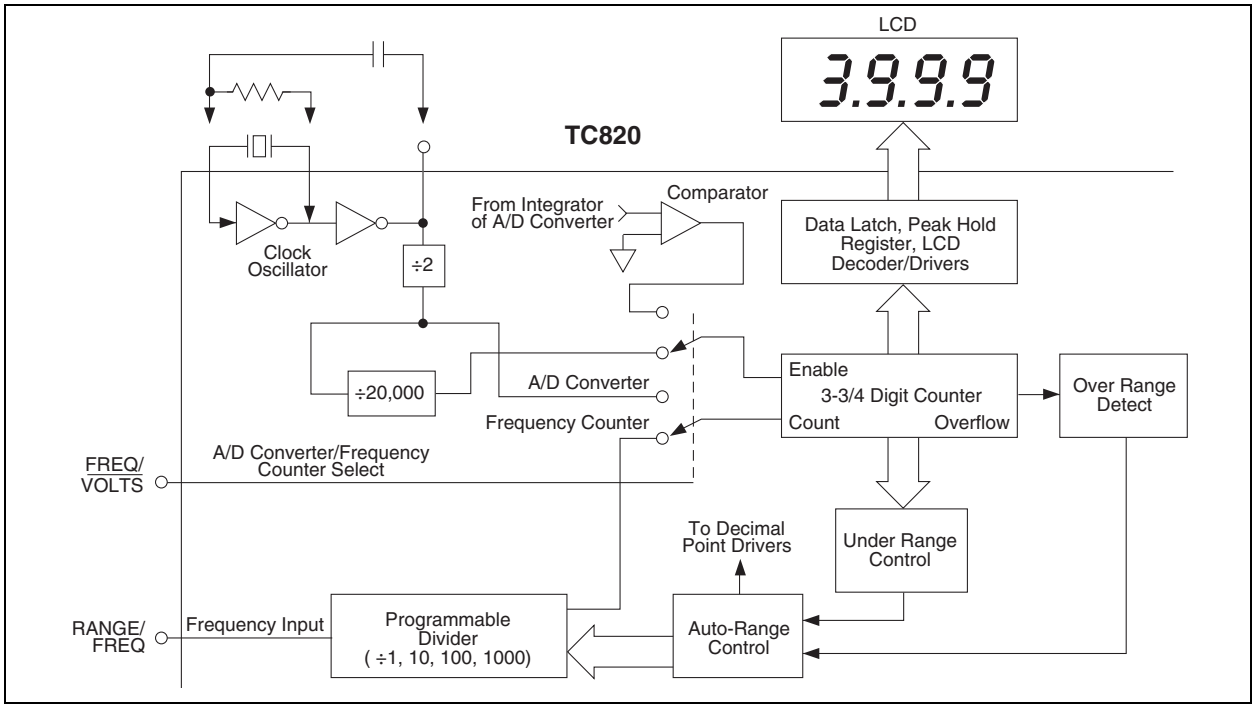


FIGURE 3-3: *TC820 Counter Operation.*

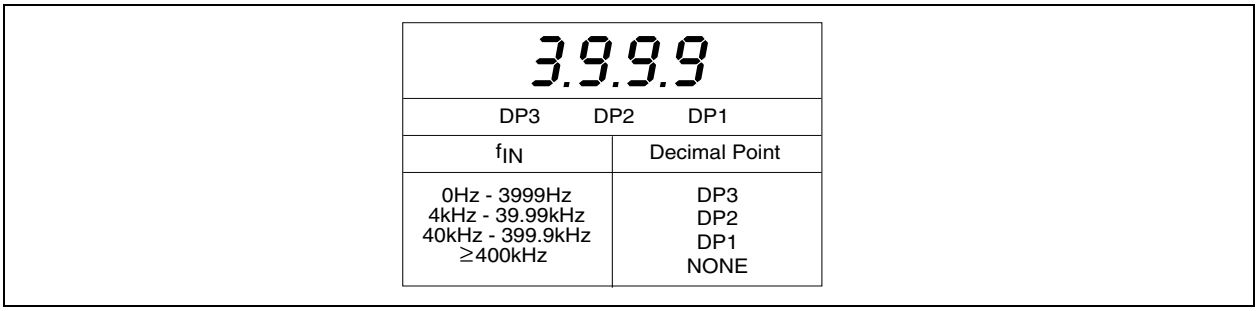


FIGURE 3-4: *Auto-range Decimal Point Selection vs. Frequency Counter Input.*

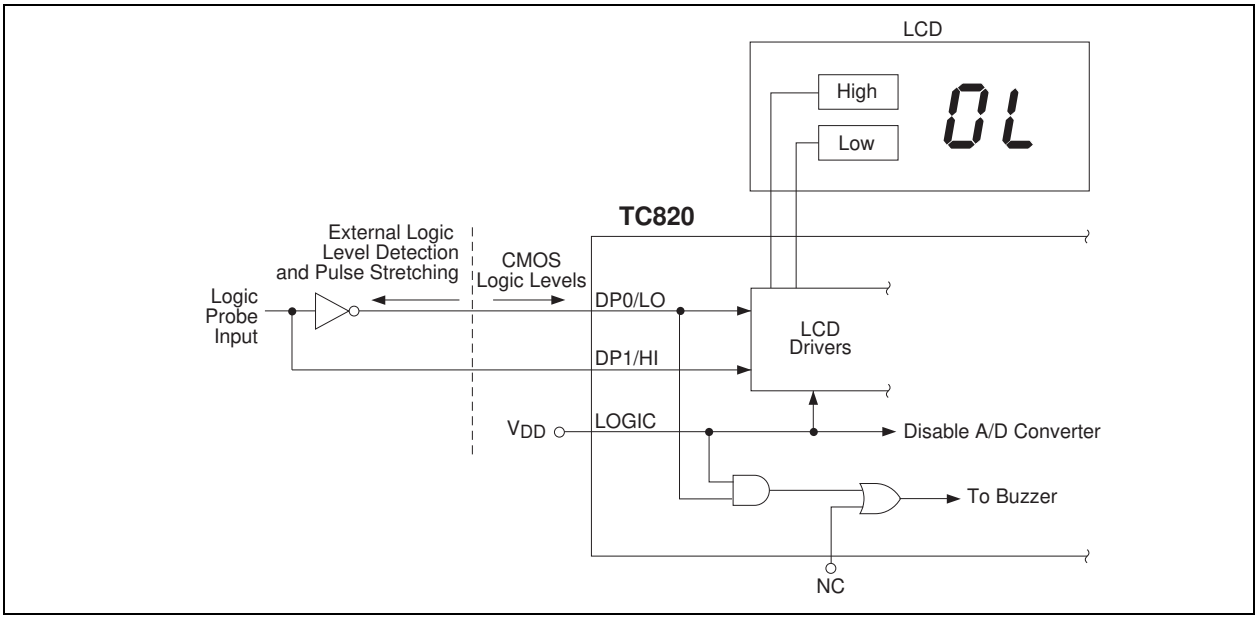


FIGURE 3-5: *Logic Probe Simplified Schematic.*

When the logic probe function is selected while FREQ/$\overline{\text{VOLTS}}$ is low (A/D mode), the ADC will remain in the Auto-Zero mode. The LCD will read "OL" and all decimal points will be off (Figure).

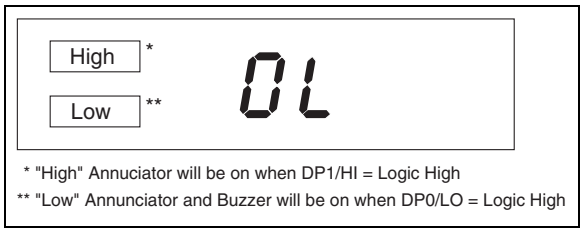


FIGURE 3-6: *LCD Reading.*

If the logic probe is active while FREQ/$\overline{\text{VOLTS}}$ is high (Counter mode), the frequency counter will continue to operate. The display will read "OL" but the decimal points will be visible. If the logic probe input is also connected to the RANGE/FREQ input, bringing the LOGIC input low will immediately display the frequency at the logic probe input.

3.5 Analog Pin Functional Description

3.5.1 DIFFERENTIAL SIGNAL INPUTS (V_{IN}+), (V_{IN}-)

The TC820 is designed with true differential inputs, and accepts input signals within the Input Stage Common mode voltage (V_{CM}) range. The typical range is V_{DD} – 1V to V_{SS} + 1.5V. Common mode voltages are removed from the system when the TC820 operates from a battery or floating power source (isolated from measured system) and V_{SS} is connected to analog common (see Figure 3-5).

In systems where Common mode voltages exist, the 86 dB Common mode rejection ratio minimizes error. Common mode voltages do, however, affect the integrator output level. A worst case condition exists if a large, positive V_{CM} exists in conjunction with a full scale, negative differential signal. The negative signal drives the integrator output positive along with V_{CM} (Figure 3-6). For such applications, the integrator output swing can be reduced below the recommended 2V full scale swing. The integrator output will swing within 0.3V of V_{DD}, or V_{DD} without increased linearity error.

3.5.2 REFERENCE (V_{DD}, V_{SS})

The TC820 reference, like the analog signal input, has true differential inputs. In addition, the reference voltage can be generated anywhere within the power supply voltage of the converter. The differential reference inputs permit ratiometric measurements and simplify interfacing with sensors, such as load cells and temperature sensors.

To prevent rollover type errors from being induced by large Common mode voltages, C_{REF} should be large compared to stray node capacitance. A 0.1 µF capacitor is typical.

The TC820 offers a significantly improved analog common temperature coefficient, providing a very stable voltage suitable for use as a voltage reference. The temperature coefficient of analog common is typically 35 ppm/°C.

3.5.3 ANALOG COMMON

The analog common pin is set at a voltage potential approximately 3.3V below V_{DD}. This potential is between 3.15V and 3.45V below V_{DD}. Analog common is tied internally to an N-channel FET capable of sinking 3 mA. This FET will hold the common line at 3.3V below V_{DD} should an external load attempt to pull the common line toward V_{DD}. Analog common source current is limited to 12 µA, and is, therefore, easily pulled to a more negative voltage (i.e., below V_{DD} – 3.3V).

The TC820 connects the internal V_{IN}+ and V_{IN}- inputs to analog common during the auto-zero cycle. During the reference integrate phase, V_{IN}- is connected to analog common. If V_{IN}- is not externally connected to analog common, a Common mode voltage exists.

This is rejected by the converter's 86 dB Common mode rejection ratio. In battery powered applications, analog common and V_{IN}- are usually connected, removing Common mode voltage concerns. In systems where V_{IN}- is connected to the power supply ground or to a given voltage, analog common should be connected to V_{IN}-.

The analog common pin serves to set the analog section reference or common point. The TC820 is specifically designed to operate from a battery, or in any “measurement" system where input signals are not referenced (float), with respect to the TC820 power source. The analog common potential of V_{DD} – 3.3V gives a 7V end of battery life voltage. The analog common potential has a voltage coefficient of 0.001%.

With a sufficiently high total supply voltage (V_{DD} – V_{SS} > 7V), analog common is a very stable potential with excellent temperature stability (typically 35ppm/°C). This potential can be used to generate the TC820 reference voltage. An external voltage reference will be unnecessary in most cases, because of the 35 ppm/°C temperature coefficient. See the applications section for details.

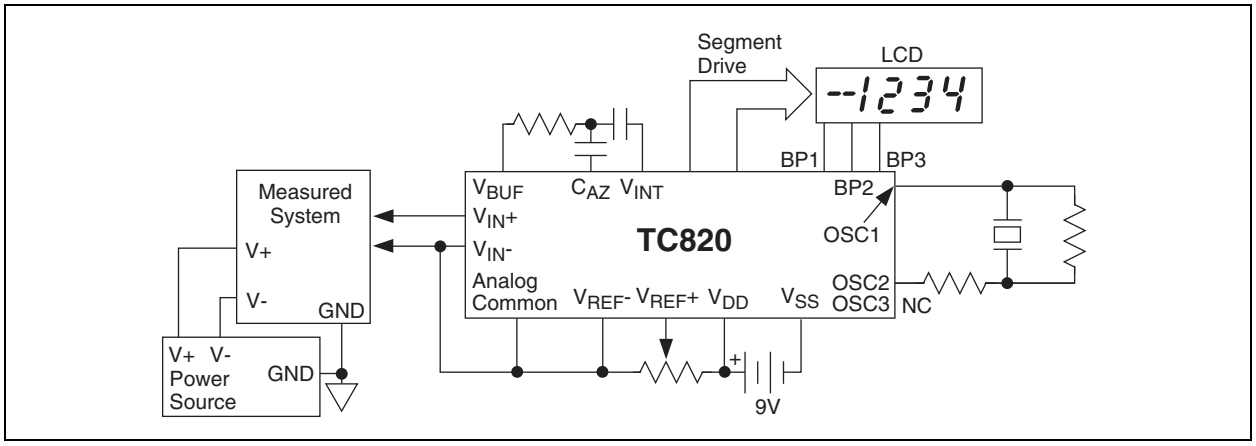


FIGURE 3-7: *Common Mode Voltage Removed In Battery Operation With V_{IN} = Analog Common.*

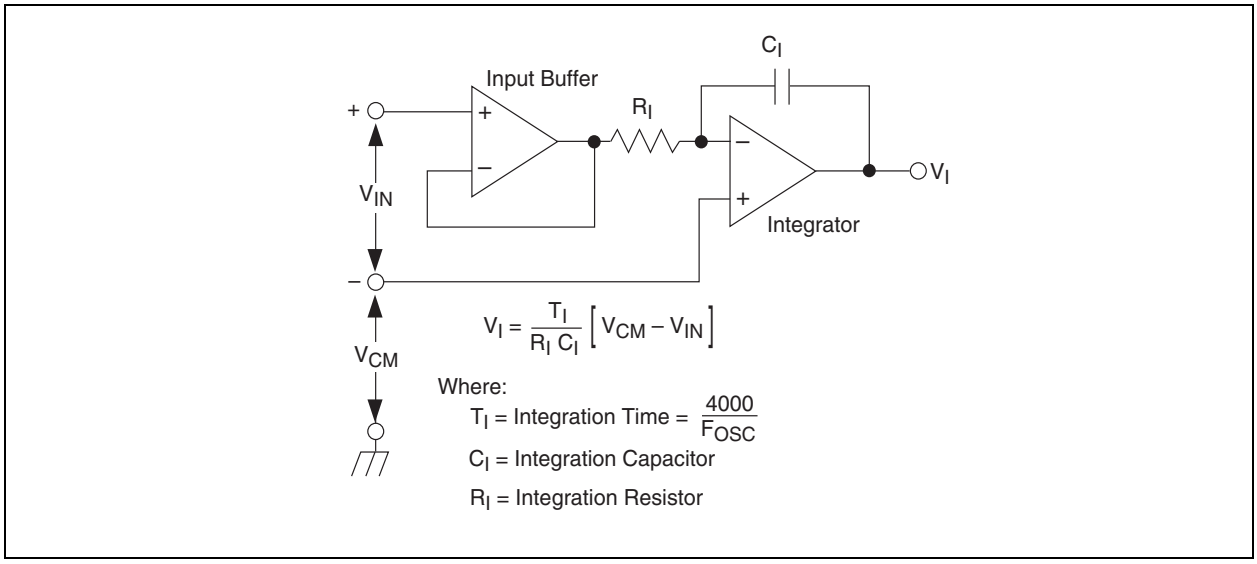


FIGURE 3-8: *Common Mode Voltage Reduces Available Integrator Swing ($V_{COM} \neq V_{IN}$).*

4.0 FUNCTION CONTROL INPUTS PIN

4.1 Functional Description

The TC820 Operating modes are selected with the function control inputs. See the control input truth, Table 4-1. The high logic threshold is ≥ V_{DD} – 1.5V and the low logic level is ≤ DGND +1.5V.

TABLE 4-1: TC820 CONTROL INPUT TRUTH TABLE

Logic Input			TC820 **Function**
FREQ/VOLTS	**RANGE/FREQ**	**LOGIC**	
X	X	1	Logic Probe
0	0	0	A/D Converter, $V_{FULL\ SCALE} = 2 \times V_{REF}$
0	1	0	A/D Converter, $V_{FULL\ SCALE} = 20 \times V_{REF}$
1	Frequency Counter Input	0	Frequency Counter

Note 1: Logic "0" = DGND
2: Logic "1" = V_{DD}-

4.1.1 FREQ/$\overline{\text{VOLTS}}$

This input determines whether the TC820 is in the Analog-to-Digital Conversion mode, or in the Frequency Counter mode. When FREQ/$\overline{\text{VOLTS}}$ is connected to V_{DD}, the TC820 will measure frequency at the RANGE/FREQ input. When unconnected, or connected to DGND, the TC820 will operate as an analog-to-digital converter. This input has an internal 5 µA pull-down to DGND.

4.1.2 LOGIC

The LOGIC input is used to activate the logic probe function. When connected to V_{DD}, the TC820 will enter the Logic Probe mode. The LCD will show "OL" and all decimal points will be off. The decimal point inputs directly control "high" and "low" display annunciators. When LOGIC is unconnected, or connected to DGND, the TC820 will perform analog-to-digital or frequency measurements, as selected by the FREQ/$\overline{\text{VOLTS}}$ input. The LOGIC input has an internal 5 µA pull-down to DGND.

4.1.3 RANGE/FREQ

The function of this dual purpose pin is determined by the FREQ/$\overline{\text{VOLTS}}$ input. When FREQ/$\overline{\text{VOLTS}}$ is connected to V_{DD}, RANGE/FREQ is the input for the frequency counter function. Pulses at this input are counted with a time-base equal to F_{OSC}/40,000. Since this input has CMOS input levels (V_{DD} – 1.5V and DGND +1.5V), an external buffer is recommended.

When the TC820 analog-to-digital converter function is selected, connecting RANGE/FREQ to V_{DD} will divide the integration time by 10. Therefore, the RANGE/FREQ input can be used to perform a 10:1 range change without changing external components.

4.1.4 DP0/LO, DP1/HI

The function of these dual purpose pins is determined by the LOGIC input. When the TC820 is in the Analog-to-Digital Converter mode, these inputs control the LCD decimal points. See the decimal point truth, Table 4-1. These inputs have internal 5 µA pull-downs to DGND when the Voltage/Frequency Measurement mode is active.

TABLE 4-1: TC820 DECIMAL POINT TRUTH TABLE

DP1	DP0	LCD
0	0	3999
0	1	399.9
1	0	39.99
1	1	3.999

Connecting the LOGIC input to V_{DD} places the TC820 in the Logic Probe mode. In this mode, the DP0/LO and DP1/HI inputs control the LCD "low" and "high" annunciators directly. When DP1/HI is connected to V_{DD}, the "high" annunciator will turn on. When DP0/LO is connected to V_{DD}, the "low" annunciator and the buzzer will turn on. The internal pull-downs on these pins are disabled when the logic probe function is selected.

These inputs have CMOS logic switching thresholds. For optimum performance as a logic probe, external level shifters are recommended. See the applications section for details.

4.1.5 BUZIN

This input controls the TC820 on-chip buzzer driver. Connecting BUZIN to V_{DD} will turn the buzzer on. There is an external pull-down to DGND. BUZIN can be used with external circuitry to provide additional functions, such as a fast, audible continuity indication.

4.2 Additional Features

The TC820 is available in 40-pin and 44-pin packages. Several additional features are available in the 44-pin package.

4.2.1 $\overline{EOC}$/HOLD

$\overline{EOC}$/HOLD is a dual purpose, bi-directional pin. As an output, this pin goes low for 10 clock cycles at the end of each conversion. This pulse latches the conversion data into the display driver section of the TC820.

$\overline{EOC}$/HOLD can be used to hold (or "FREEZE") the display. Connecting this pin to V_{DD} inhibits the display update process. Conversions will continue, but the display will not change. $\overline{EOC}$/HOLD will hold the display reading for either analog-to-digital, or frequency measurements.

The input/output structure of the $\overline{EOC}$/HOLD pin is shown in Figure 4-2. The output drive current is only a few microAmps, so $\overline{EOC}$/HOLD can easily be over-driven by an open collector logic gate, as well as a FET, bipolar transistor, or mechanical switch. When used as an output, $\overline{EOC}$/HOLD will have a slow rise and fall time due to the limited output current drive. A CMOS Schmitt trigger buffer is recommended.

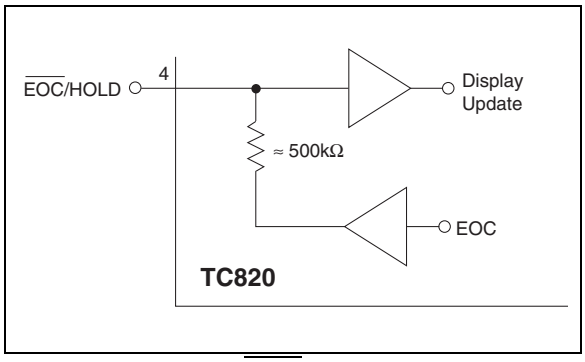


FIGURE 4-2: *$\overline{EOC}$/HOLD Pin.*

4.2.2 OVER RANGE (OR), UNDER RANGE (UR)

The OR output will be high when the analog input signal is greater than full scale (3999 counts). The UR output will be high when the display reading is 380 counts or less.

The OR and UR outputs can be used to provide an auto-ranging meter function. By logically ANDing these outputs with the inverted $\overline{EOC}$/HOLD output, a single pulse will be generated each time an under ranged or over ranged conversion occurs (Figure 4-2).

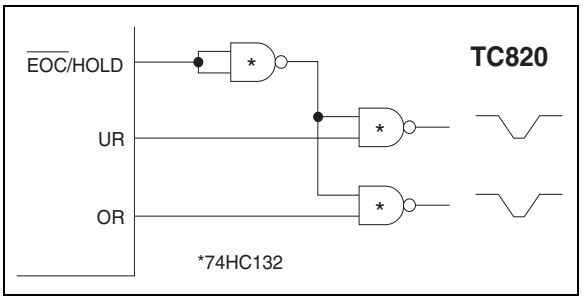


FIGURE 4-3: *Generating Under Range And Over Range Pulses.*

4.2.3 V_{DISP}

The V_{DISP} input sets the peak-to-peak LCD drive voltage. In the 40-pin package, V_{DISP} is connected internally to DGND, providing a typical LCD drive voltage of $5V_{P-P}$. The 44-pin package includes a separate V_{DISP} input for applications requiring a variable or temperature compensated LCD drive voltage. See the applications information for suggested circuits.

5.0 TYPICAL APPLICATIONS

5.1 Power Supplies

The TC820 is designed to operate from a single power supply such as a 9V battery (Figure 5-1). The converter will operate over a range of 7V to 15V. For battery operation, analog common (COM) provides a Common mode bias voltage (see analog common discussion in the theory of operation section). However, measurements cannot be referenced to battery ground. To do so will exceed the Negative Common mode voltage limit.

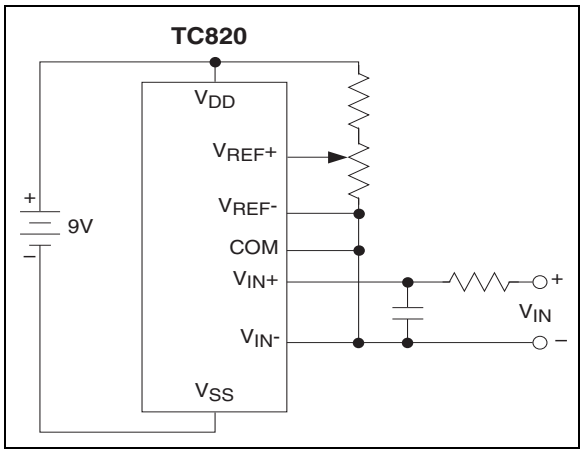


FIGURE 5-1: *Powering the TC820 from a Single 9V Battery.*

A battery with voltage between 3.5V and 7V can be used to power the TC820, when used with a voltage doubler, as shown in Figure 5-2. The voltage doubler uses the TC7660 and two external capacitors. With this configuration, measurements can be referenced either to analog common or to battery ground.

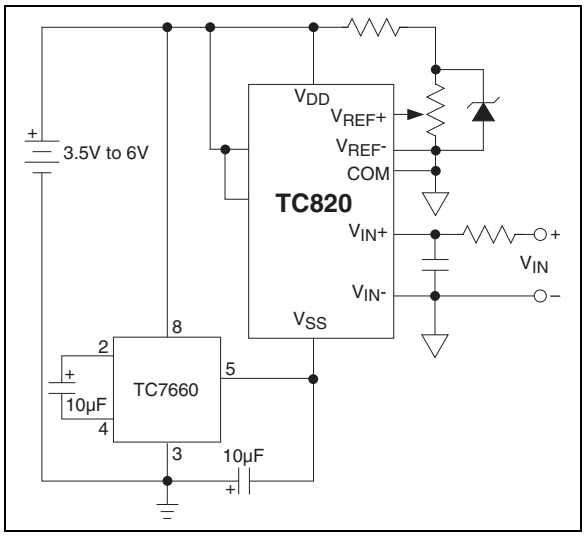


FIGURE 5-2: *Powering the TC820 from a Low Voltage Battery.*

5.2 Digital Ground (DGND)

Digital ground is generated from an internal zener diode (Figure 5-3). The voltage between V_{DD} and DGND is the internal supply voltage for the digital section of the TC820. DGND will sink a minimum of 3 mA.

DGND establishes the low logic level reference for the TC820 mode select inputs, and for the frequency and logic probe inputs. The DGND pin can be used as the negative supply for external logic gates, such as the logic probe buffers. To ensure correct counter operation at high frequency, connect a 1 µF capacitor from DGND to V_{DD}.

DGND also provides the drive voltage for the LCD. The TC820 40-pin package internally connects the LCD V_{DISP} pin to DGND, and provides an LCD drive voltage of about $5V_{P-P}$. In the 44-pin package, connecting the V_{DISP} pin to DGND will provide a 5V LCD drive voltage.

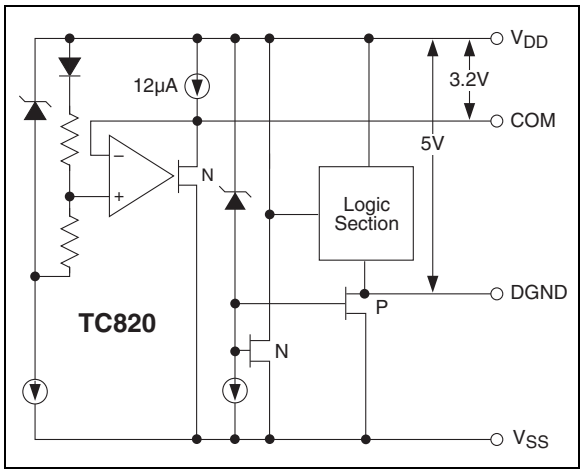


FIGURE 5-3: *DGND and Com Outputs.*

5.3 Digital Input Logic Levels

Logic levels for the TC820 digital inputs are referenced to V_{DD} and DGND. The high level threshold is $V_{DD} - 1.5V$, and the low logic level is DGND + 1.5V. In most cases, digital inputs will be connected directly to V_{DD} with a mechanical switch. CMOS gates can also be used to control the logic inputs, as shown in the logic probe inputs section.

5.4 Clock Oscillator

The TC820 oscillator can be controlled with either a crystal, or with an inexpensive resistor capacitor combination. The crystal circuit, shown in Figure 5-4, is recommended when high accuracy is required in the Frequency Counter mode. The 40 kHz crystal is a standard frequency for ultrasonic alarms, and will provide a 1-second time-base for the counter or 2.5 analog-to-digital conversions per second. Consult the crystal manufacturer for detailed applications information.

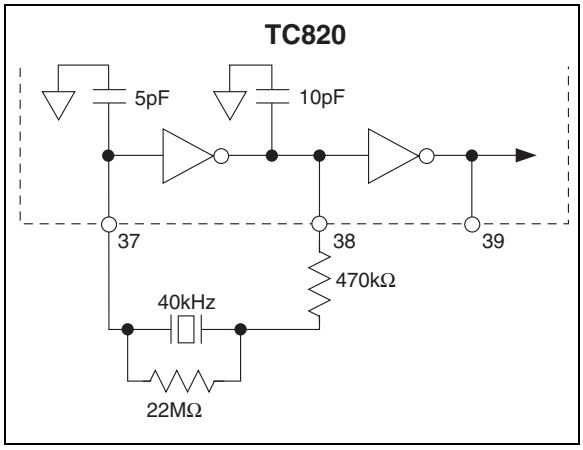


FIGURE 5-4: *Suggested Crystal Oscillator Circuit.*

Where low cost is important, the RC circuit of Figure 5-5 can be used. The frequency of this circuit will be approximately:

EQUATION 5-1:

$$T_{OSC} = \frac{0.3}{RC}$$

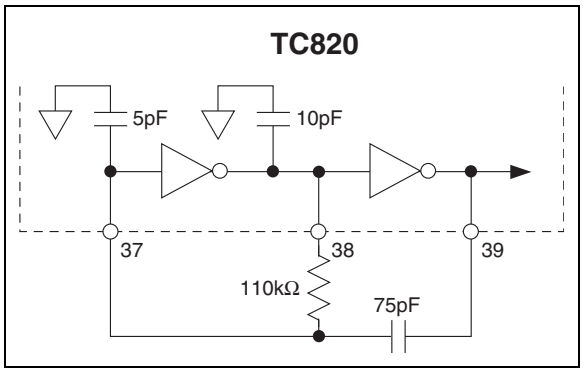


FIGURE 5-5: *RC Oscillator Circuit.*

Typical values are R = 10 kΩ and C = 68pF. The resistor value should be ≥ 100 kΩ. For accurate frequency measurement, an RC oscillator frequency of 40 kHz is required.

5.5 System Timing

All system timing is derived from the clock oscillator. The clock oscillator is divided by 2 prior to clocking the A/D counters. The clock is also divided by 8 to drive the buzzer, by 240 to generate the LCD backplane frequency, and by 40,000 for the frequency counter time-base. A simplified diagram of the system clock is shown in Figure 5-6.

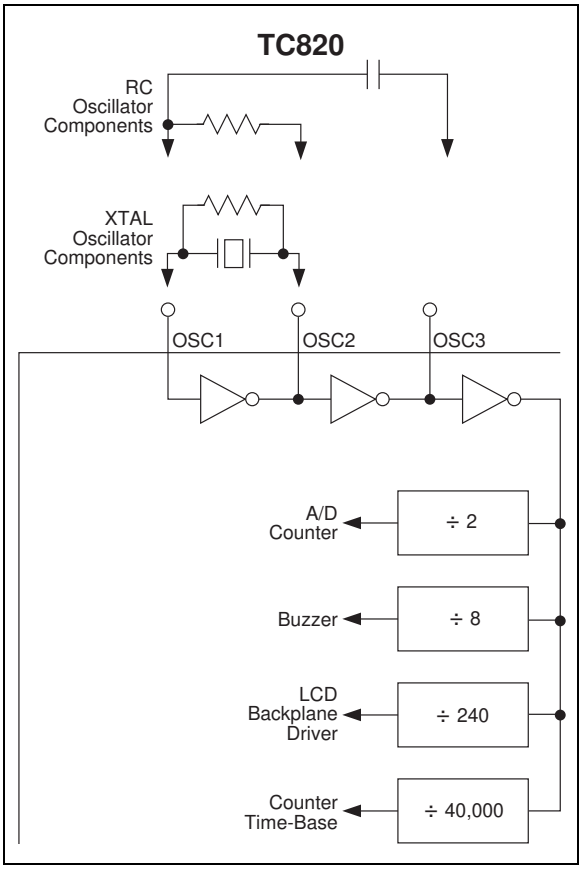


FIGURE 5-6: *System Clock Generation.*

5.6 Component Value Selection

5.6.1 AUTO-ZERO CAPACITOR - C_{AZ}

The value of the auto-zero capacitor (C_{AZ}) has some influence on system noise. A 0.47 µF capacitor is recommended; a low dielectric absorption capacitor (Mylar) is required.

5.6.2 REFERENCE VOLTAGE CAPACITOR - C_{REF}

The reference voltage capacitor used to ramp the integrator output voltage back to zero during the reference integrate cycle is stored on C_{REF}. A 0.1 µF capacitor is typical. A good quality, low leakage capacitor (such as Mylar) should be used.

5.6.3 INTEGRATING CAPACITOR - C_{INT}

C_{INT} should be selected to maximize integrator output voltage swing without causing output saturation. Analog common will normally supply the differential voltage reference. For this case, a ±2V integrator output swing is optimum when the analog input is near full scale. For 2.5 readings/second (F_{OSC} = 40 kHz) and V_{FS} = 400 mV, a 0.22 µF value is suggested. If a different oscillator frequency is used, C_{INT} must be changed in inverse proportion to maintain the nominal ±2V integrator swing.

An exact expression for C_{INT} is:

EQUATION 5-2:

$$C_{INT} = \frac{4000\ V_{FS}}{V_{INT}\ R_{INT}\ F_{OSC}}$$

Where:

F_{OSC}	=	Clock Frequency
V_{FS}	=	Full-Scale Input Voltage
R_{INT}	=	Integrating Resistor
V_{INT}	=	Desired Full-Scale Integrator Output Swing

C_{INT} must have low dielectric absorption to minimize rollover error. A polypropylene capacitor is recommended.

5.6.4 INTEGRATING RESISTOR - R_{INT}

The input buffer amplifier and integrator are designed with class A output stages. The integrator and buffer can supply 40 µA drive currents with negligible linearity errors. R_{INT} is chosen to remain in the output stage linear drive region, but not so large that printed circuit board leakage currents induce errors. For a 400 mV full-scale, R_{INT} should be about 100 kΩ.

5.7 Reference Voltage Selection

A full-scale reading (4000 counts for TC820) requires the input signal be twice the reference voltage. See Reference Voltage Selection, Table 5-1 below.

TABLE 5-1: REFERENCE VOLTAGE SELECTION

Full Scale Input Voltage (V_{FS}) (Note 1)	V_{REF}	Resolution
200 mV	**(Note 2)**	—
400 mV	200 mV	10 µV
1V	500 mV	250 µV
2V **(Notes 3, 4)**	1V	500 µV

Note 1: TC820 in A/D Converter mode, RANGE/FREQ = logic low.

2: Not recommended.

3: V_{FS} > 2V may exceed the Input Common mode range. See **Section 3.2.7 "10:1 Range Change"**.

4: Full-scale voltage values are not limited to the values shown. For example, TC820 V_{FS} can be any value from 400 mV to 2V.

In some applications, a scale factor other than unity may exist between a transducer output voltage and the required digital reading. Assume, for example, that a pressure transducer output is 800 mV for 4000 lb/in^2. Rather than dividing the input voltage by two, the reference voltage should be set to 400 mV. This permits the transducer input to be used directly.

The internal voltage reference potential available at analog common will normally be used to supply the converter's reference voltage. This potential is stable whenever the supply potential is greater than approximately 7V. The low battery detection circuit and analog common operate from the same internal reference. This ensures that the low battery annunciator will turn on at the time the internal reference begins to lose regulation.

The TC820 can also operate with an external reference. Figure 5-7 shows internal and external reference applications.

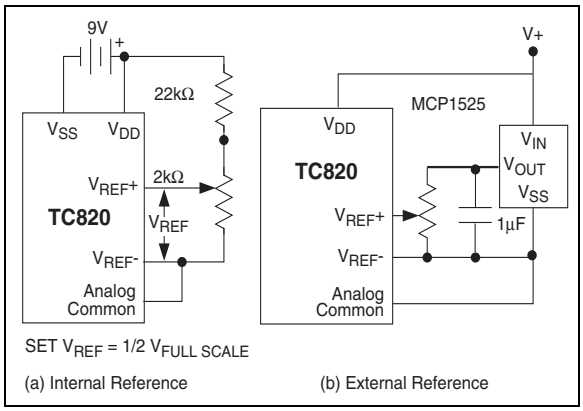


FIGURE 5-7: *Reference Voltage Connections.*

5.8 Ratiometric Resistance Measurements

The TC820 true differential input and differential reference make ratiometric readings possible. In ratiometric operation, an unknown resistance is measured with respect to a known standard resistance. No accurately defined reference voltage is needed.

The unknown resistance is put in series with a known standard and a current is passed through the pair (Figure 5-8). The voltage developed across the unknown is applied to the input and voltages across the known resistor applied to the reference input. If the unknown equals the standard, the input voltage will equal the reference voltage and the display will read 2000. The displayed reading can be determined from the following expression:

EQUATION 5-3:

$$\text{Displayed Reading} = \frac{R_{UNKNOWN}}{R_{STANDARD}}$$

The display will over range for values of $R_{UNKNOWN} \geq 2 \times R_{STANDARD}$.

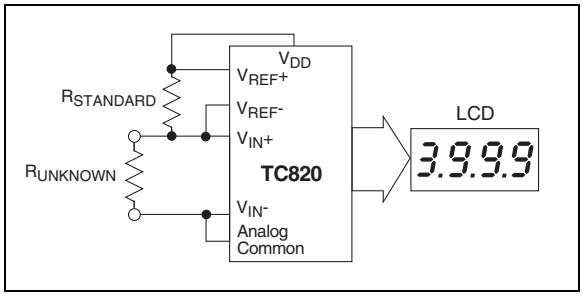


FIGURE 5-8: *Low Parts Count Ratiometric Resistance Measurement.*

5.9 Buffering the FREQ Input

When the FREQ/$\overline{\text{VOLTS}}$ input is high and the LOGIC input is low, the TC820 will count pulses at the RANGE/FREQ input. The time-base will be $F_{OSC}/40{,}000$, or 1 second with a 40kHz clock. The signal to be measured should swing from V_{DD} to DGND. The RANGE/FREQ input has CMOS input levels without hysteresis. For best results, especially with low frequency sine-wave inputs, an external buffer with hysteresis should be added. A typical circuit is shown in Figure 5-9.

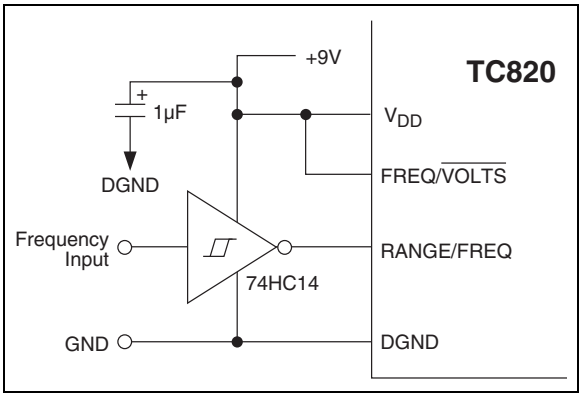


FIGURE 5-9: *Frequency Counter External Buffer.*

5.10 Logic Probe Inputs

The DP0/LO and DP1/HI inputs provide the logic probe inputs when the LOGIC input is high. Driving either DP0/LO or DP1/HI to a logic high will turn on the appropriate LCD annunciator. When DP0/LO is high, the buzzer will be on.

To provide a "single input" logic probe function, external buffers should be used. A simple circuit is shown in Figure 5-10. This circuit will turn the appropriate annunciator on for high and low level inputs.

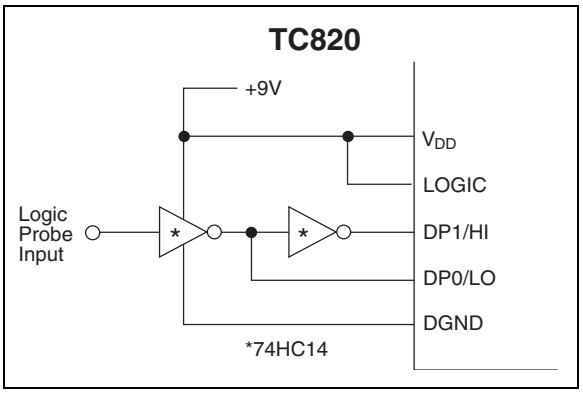


FIGURE 5-10: *Simple External Logic Probe Buffer.*

If carefully controlled logic thresholds are required, a window comparator can be used. Figure 5-11 shows a typical circuit. This circuit will turn on the high or low annunciators when the logic thresholds are exceeded, but the resistors connected from DP0/LO and DP1/HI to DGND will turn both annunciators off when the logic probe is unconnected.

The TC820 logic inputs are not latched internally, so pulses of short duration will usually be difficult or impossible to see. To display short pulses properly, the input pulse should be "stretched." The circuit of Figure 5-11 shows capacitors added across the input pull-down resistors to stretch the input pulse and permit viewing short duration input pulses.

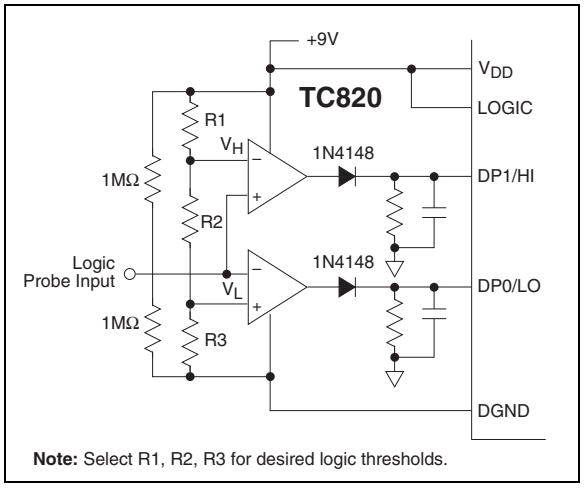


FIGURE 5-11: *Window Comparator Logic Probe.*

5.11 External Peak Detection

The TC820 will hold the highest A/D conversion or frequency reading indefinitely when the PKHOLD input is connected to V_{DD}. However, the analog peak input must be present during the A/D converter's signal integrate period. For slowly changing signals, such as temperature, the peak reading will be properly converted and held.

If rapidly changing analog signals must be held, an external peak detector should be added. An inexpensive circuit can be made from an op amp and a few discrete components, as shown in Figure 5-12. The droop rate of the external peak detector should be adjusted so that the held voltage will not decay below the desired accuracy level during the converter's 400 ms conversion time.

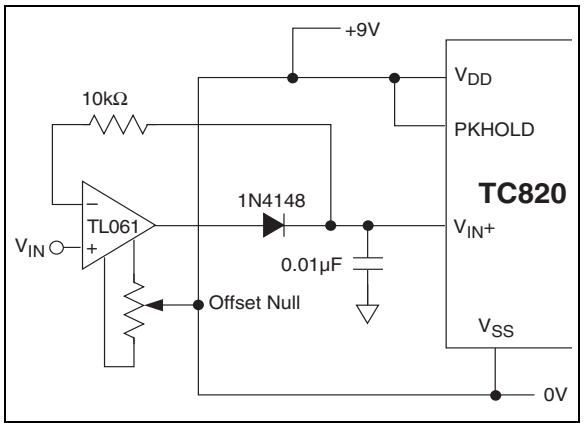


FIGURE 5-12: *External Peak Detector.*

5.12 Liquid Crystal Display (LCD)

The TC820 drives a triplex (multiplexed 3:1) LCD with three backplanes. The LCD can include decimal points, polarity sign, and annunciators for over range, peak hold, high and low logic levels, and low battery.

Table 5-2 shows the assignment of the display segments to the backplanes and segment drive lines. The backplane drive frequency is obtained by dividing the oscillator frequency by 240.

Backplane waveforms are shown in Figure 5-13. These appear on outputs BP1, BP2, and BP3. They remain the same, regardless of the segments being driven.

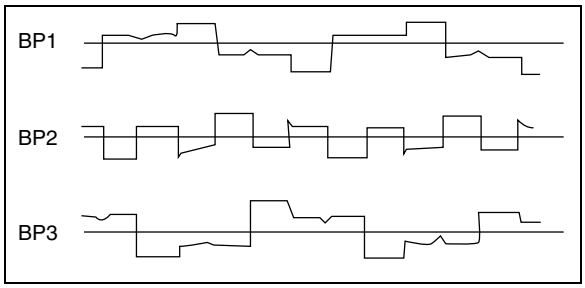


FIGURE 5-13: *Backplane Waveforms.*

Other display output lines have waveforms that vary depending on the displays values. Figure 5-13 shows a set of waveforms for the a, g, d outputs of one digit for several combinations of "on" segments.

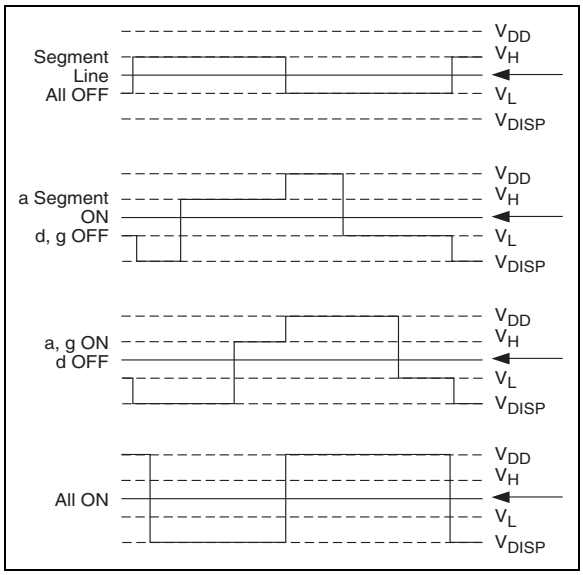


FIGURE 5-14: *Typical Display Output Waveforms.*

TABLE 5-2: LCD BACKPLANE AND SEGMENT ASSIGNMENTS

40-Pin (PDIP)	44-Pin (PQFP)	LCD Display Pin Number	BP1	BP2	BP3
1	40	3	LOW		
2	41	4	A4	"—"	
3	42	5	B4	G4	E4
4	43	6	HIGH	C4	D4
5	44	7	A3	F3	DP3
6	1	8	B3	G3	E3
7	2	9	OVER	C3	D3
8	3	10	A2	F2	DP2
9	4	11	B2	G2	E2
10	5	12	PEAK	C2	D2
11	6	13	A1	F1	DP1
12	7	14	B1	G1	E1
13	8	2,16*	—	C1	D1
14	9	1	BP1	—	BATT
15	10	15	LOW	BP2	BP3

* Connect both pins 2 and 16 of LCD to TC820 BP3 of output.

5.13 LCD Source

Although most users will design their own custom LCD, a standard display for the TC820 (Figure 5-15), Part No. ST-1355-M1, is available from the following sources:

Crystaloid (USA)
Crystaloid Electronics
P.O. Box 628
5282 Hudson Drive
Hudson, OH 44238
Phone: 216-655-2429

Crystaloid (Europe)
Rep. France
102, rue des Nouvelles
F92150 Suresnes France
Phone: 33-1-42-04-29-25
Fax: 33-1-45-06-46-99

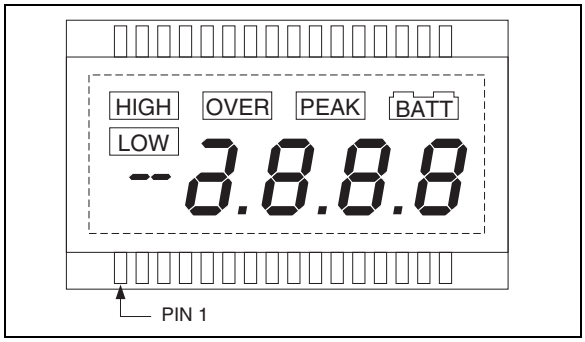


FIGURE 5-15: *Typical TC820 LCD.*

5.14 Annunciator Output

The annunciator output is a square wave running at the backplane frequency (for example, 167Hz when F_{OSC} = 40kHz). The peak-to-peak amplitude is equal to ($V_{DD} – V_{DISP}$). Connecting an annunciator of the LCD to the annunciator output turns it on; connecting it to its backplane turns it off.

5.15 LCD Drive Voltage (V_{DISP})

The peak-to-peak LCD drive voltage is equal to ($V_{DD} – V_{DISP}$). In the 40-pin dual in-line package (DIP), V_{DISP} is internally connected to DGND, providing a typical LCD drive voltage of $5V_{P-P}$.

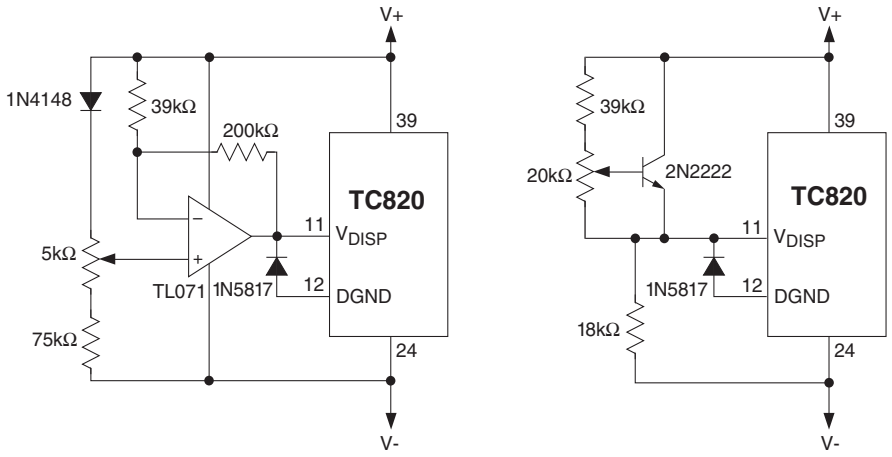
For applications with a wide temperature range, some LCDs require that the drive levels vary with temperature to maintain good viewing angle and display contrast. In this case, the TC820 44-pin package provides a pin connection for V_{DISP}. Figure 5-16 shows TC820 circuits that can be adjusted to give a temperature compensation of about 10mV/°C between V_{DD} and V_{DISP}. The diode between GND and V_{DISP} should have a low turn on voltage because V_{DISP} cannot exceed 0.3V below GND.

5.16 Crystal Source

Two sources of the 40kHz crystal are:

Statek Corp.
512 N. Main St.
Orange, CA 92668
Phone: 714-639-7810
Fax: 714-997-1256
Part #: CX-1V-40.0

SPK Electronics
2F-1, No. 312, Sec, 4, Jen Ai Rd.
Taipei, Taiwan R.O.C.
Phone: (02) 754-2677
Fax: 886-2-708-4124
Part #: QRT-38-40.0kHz



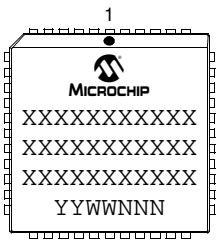
Note: Pin numbers shown are for 44-pin flat package.

FIGURE 5-16: *Temperature Compensating Circuits.*

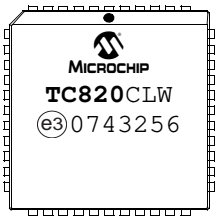
6.0 PACKAGING INFORMATION

6.1 Package Marking Information

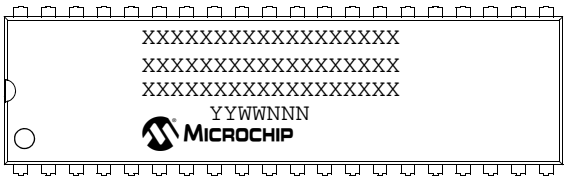
44-Pin PLCC



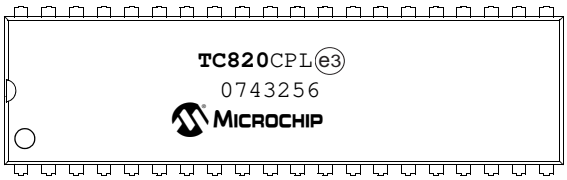
Example:



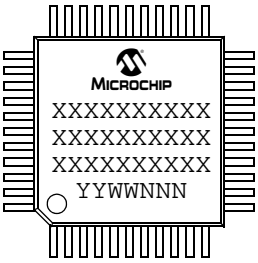
40-Pin PDIP



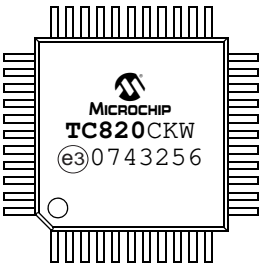
Example:



44-Pin MQFP



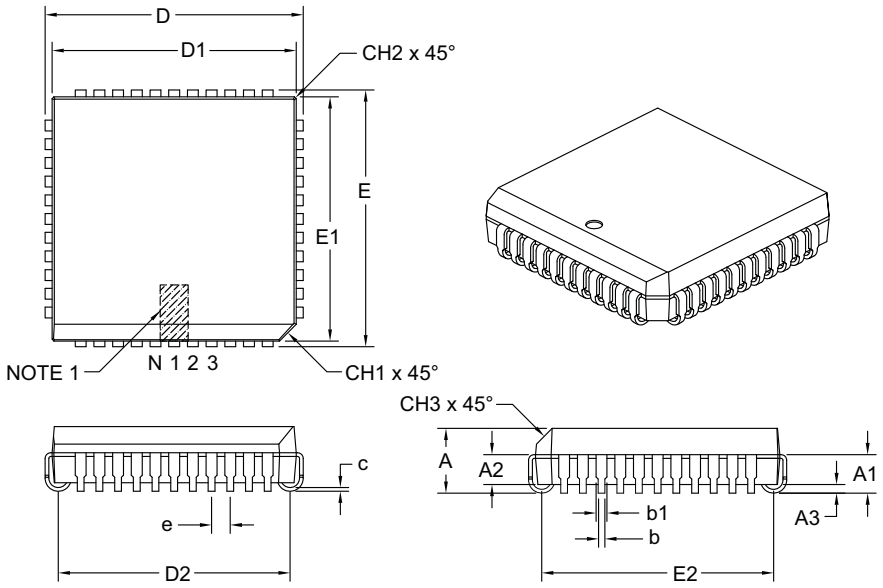
Example:



Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.
Note:	In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.	

44-Lead Plastic Leaded Chip Carrier (LW) – Square [PLCC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		INCHES		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		44	
Pitch	e		.050	
Overall Height	A	.165	.172	.180
Contact Height	A1	.090	.105	.120
Molded Package to Contact	A2	.062	–	.083
Standoff §	A3	.020	–	–
Corner Chamfer	CH1	.042	–	.048
Chamfers	CH2	–	–	.020
Side Chamfer	CH3	.042	–	.056
Overall Width	E	.685	.690	.695
Overall Length	D	.685	.690	.695
Molded Package Width	E1	.650	.653	.656
Molded Package Length	D1	.650	.653	.656
Footprint Width	E2	.582	.610	.638
Footprint Length	D2	.582	.610	.638
Lead Thickness	c	.0075	–	.0125
Upper Lead Width	b1	.026	–	.032
Lower Lead Width	b	.013	–	.021

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic.
3. Dimensions D1 and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" per side.
4. Dimensioning and tolerancing per ASME Y14.5M.

Microchip Technology Drawing C04-048B