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General Description

The MAX24101 restores high-frequency signal level at the decision-feedback equalizer (DFE) receiver for high-loss backplane and cable channels. This permits the DFE receiver to meet BER goals. At 15Gbps, the MAX24101 can operate in channels with FR4 and cable HF loss more of than 30dB at 7.5GHz. The linear transfer function is transparent to Adaptive DFE equalizers, permitting DFE adaptation to track temperature and changing channel conditions.

Together with the DFE, integrated into Serializer/Deserializer (SERDES), the device adds increased margin rather than full signal regeneration. Unlike conventional equalizers with limiting output stages, the device preserves the linear channel characteristics, allowing the DFE to linearly operate over the entire channel. This permits extending total channel reach and/or improving signal-to-noise ratio (SNR). The device typically compensates for up to 19dB of the total loss in a long channel, effectively reducing the channel length seen by the DFE receiver.

The device has 8 channels and is packaged in a space-saving, 4mm x 13mm, FCLGA package.

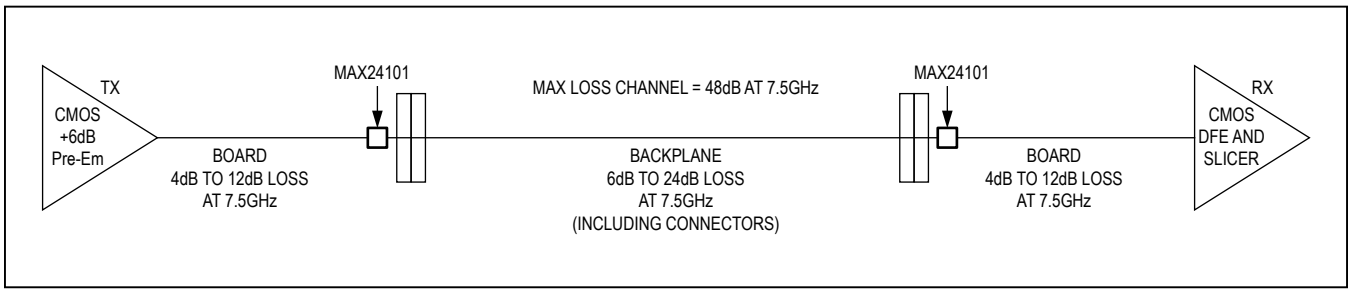
Applications

- 1Gbps to 15Gbps High-Speed Backplanes and Cables
- 12.5Gbps Quad XAUI Interconnect
- 14Gbps 16G Fiber Channel
- 12Gbps SAS III

Benefits and Features

- 1Gbps to 15Gbps Linear EQ
- Increases High-Frequency Signal Level To Help Rx DFE Achieve BER Goals
- Lower Power, Lower Cost, And Smaller Board Footprint Than CDR Solutions
- Transparent-to-Link Training, OOB And Idle
- Plug and Play—Set Control Pins (All Channels Set the Same) or Independent Control of Each Channel through I^2C Bus
- I^2C Daisy Chain For Addressing Up to 63 ICs
- Selectable EQ Peaking Spanning +6dB to +19dB at 7.5GHz
- Selectable Flat Gain Spanning -2.9dB to +1.7dB
- Selectable Output Linear Swing Spanning 700mV_{P-P} to 1000mV_{P-P}
- Low Input-Referred Noise < 1mV_{RMS}
- Data-Rate and Coding Agnostic
- Input Return Loss Better Than 16dB Typical Up to 7.5GHz
- Power-Down Mode Saves Power When Not In Use
- 4mm x 13mm FCLGA Package
- Single 2.5V Supply
- 131mW Per Channel Power Dissipation with a 700mV_{P-P} Output

Typical Application Circuit



***Ordering Information* appears at end of data sheet.**

For related parts and recommended products to use with this part, refer to www.maximintegrated.com/MAX24101.related.

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Absolute Maximum Ratings

Power-Supply Voltage ..... -0.5V to +4.0V
DC Input Voltage Applied (all control pins except SDA and SCL) ..... -0.5V to (V_{CC} + 0.3V)
DC Input Voltage Applied (SDA, SCL) ..... -0.5V to +4.0V
Output Current ..... -90mA to +90mA
Operating Junction Temperature ..... +125ºC
Storage Temperature Range ..... -40ºC to +150°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Thermal Characteristics (Note 1)

FCLGA
Junction-to-Case Thermal Resistance (θ_{JC}) ..... 10°C/W
Junction-to-Ambient Thermal Resistance (θ_{JA}) (EIA/JESD51-2 standard) ..... 29°C/W

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

Operating Conditions

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage	V_{CCR}, V_{CCT}, V_{CCP}		2.312	2.5	2.75	V
Operating Ambient Temperature	T_A		-40	+25	+85	°C
Data Rate			1		15	Gbps
Source Data Coding and CID		DC balanced NRZ, 8B10B or Scrambled; PRBS31			66	CID
Differential Source Diff Low-Frequency Voltage	V_{LAUNCH}	LF Baseline (without PE) measured at source; source HF pre-emphasis swing can be higher			1200	mV_{P-P}
Source Rise/Fall Time		Test source 10% to 90%		26		ps
Source Common-Mode Noise		DC - 200MHz			150	mV_{P-P}
Supply Noise		DC - 1MHz		50		mV_{P-P}

Electrical Characteristics

(Typical values are at V_{CCR} = V_{CCT} = V_{CCP} = 2.5V, T_A = +25°C. See Figure 1 for typical supply filtering.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Supply Current	I_{CCR} + I_{CCT} + I_{CCP}	Total supply current with all 8 channels enabled	TXAx[1:0] = 00		420	550	mA
			TXAx[1:0] = 11		511	610	
Supply Current During Power-Down					4.8		mA

Electrical Characteristics (continued)

(Typical values are at V_{CCR} = V_{CCT} = V_{CCP} = 2.5V, T_A = +25°C. See Figure 1 for typical supply filtering.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Inrush Current		Beyond steady-state supply current with supply ramp-up time less than 200µs			< 10		%
Residual Deterministic Jitter (Notes 3, 4)	DJ_{RX}	Over-bit rate with EQ peaking optimized for loss channel, in linear range			9		ps_{P-P}
Peaking Gain (Compensation at 7.5GHz, relative to 100MHz, 100mV_{P-P} Sine Wave Input)	GN_P	EQx[3:0] = 1110			18.5		dB
		EQx[3:0] = 1001			15.7		
		EQx[3:0] = 0101			13.2		
		Variation around typical	T_A = +85°C	-3.67		+0.82	
			T_A = +25°C	-1.61		+1.96	
			T_A = -40°C	-1.62		+3.60	
Flat Gain (100MHz, EQx[3:0] = 1000, TXAx[1:0] = 10)	GN_F	FGx[1:0] = 11			1.68		dB
		FGx[1:0] = 10			0.14		
		FGx[1:0] = 01			-1.36		
		FGx[1:0] = 00			-2.87		
		Variation around typical	T_A = +85°C	-4.05		+0.95	
			T_A = +25°C	-3.32		+1.83	
			T_A = -40°C	-3.40		+2.86	
-1dB Compression Point Output Swing (at 100MHz)	V_{1dB_OUT}	TXAx[1:0] = 11		1000	1370		mV_{P-P}
		TXAx[1:0] = 10			1280		
		TXAx[1:0] = 01			1040		
		TXAx[1:0] = 00			920		
-1dB Compression Point Output Swing (Note 5) (at 7.5GHz)	V_{1dB_OUT}	TXAx[1:0] = 11			1000		mV_{P-P}
		TXAx[1:0] = 10			940		
		TXAx[1:0] = 01			700		
		TXAx[1:0] = 00			600		
Input-Referred Noise	V_{NOISE}	100MHz to 7.5GHz, FGx[1:0] = 11, EQx[3:0] = 0000, Figure 3			0.6		mV_{RMS}
		100MHz to 7.5GHz, FGx[1:0] = 11, EQx[3:0] = 1010, Figure 3			0.5		
Output-Referred Noise (Note 3)	V_{NOISE}	100MHz to 7.5GHz, FGx[1:0] = 11, EQx[3:0] = 0000, Figure 3			0.8		mV_{RMS}
		100MHz to 7.5GHz, FGx[1:0] = 11, EQx[3:0] = 1010, Figure 3			1.0	1.97	

Electrical Characteristics (continued)

(Typical values are at V_{CCR} = V_{CCT} = V_{CCP} = 2.5V, T_A = +25°C. See Figure 1 for typical supply filtering.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
HIGH SPEED I/O							
Input Common-Mode Voltage	V_{ICM}					2.05	V
Input Resistance	R_{IN}	DC differential resistance			100		Ω
		AC common-mode (single-ended) resistance			50		
Input Return Loss	S_{11}	10MHz to 7.5GHz	Differential		> 16		dB
		1GHz to 7.5GHz	Common mode		> 10		
Output Resistance	R_{OUT}	DC differential resistance			100		Ω
		AC common mode (single-ended) resistance			50		
Pulse Response Ringing					3		%
Intra-Pair Skew					2		ps
Inter-Pair Skew					4		ps
Output Return Loss	S_{22}	10MHz to 7.5GHz	Differential		> 13		dB
		1GHz to 7.5GHz	Common Mode		> 8		
Channel Isolation	V_{Coup}	100MHz to 7.5GHz, Figure 4 (Note 6)			40		dB
LVCMOS I/O							
Input Logic-High Voltage	V_{IH}			0.7 x V_{CC}		V_{CC} + 0.3	V
Input Logic-Low Voltage	V_{IL}			-0.3		0.3 x V_{CC}	V
Output Logic-High Voltage	V_{OH}	At I_{OH} = -200µA		V_{CC} + 0.2			V
Output Logic-Low Voltage	V_{OL}	At I_{OL} = -200µA				0.2	V
Open State Current Tolerance	H_{IZ}				±5		µA
Input Logic-High Current	I_{IH}	$V_{IH(MIN)} < V_{IN} < V_{IH(MAX)}$, all other CMOS pins				±450	µA
		$V_{IH(MIN)} < V_{IN} < V_{IH(MAX)}$, $\overline{PGM\_IN}$				+120	
Input Logic-Low Current	I_{IL}	$V_{IL(MIN)} < V_{IN} < V_{IL(MAX)}$, all other CMOS pins		-450			µA
		$V_{IL(MIN)} < V_{IN} < V_{IL(MAX)}$, $\overline{PGM\_IN}$		-18			

Electrical Characteristics (continued)

(Typical values are at V_{CCR} = V_{CCT} = V_{CCP} = 2.5V, T_A = +25°C. See Figure 1 for typical supply filtering.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
I²C CHARACTERISTICS (SDA, SCL) (Note 7)						
Low-Level Input Voltage	V_{IL}				0.3 x V_{CC}	V
High-Level Input Voltage	V_{IH}		0.7 x V_{CC}			V
Input Hysteresis	V_{HYS}			200		mV
Input Capacitance	C_{IN}			10		pF
Input Leakage Current	I_{IN}				±1	mA
Output Low Voltage SDA	V_{OL}	I_{SINK} = 3mA			0.4	V
		I_{SINK} = 6mA			0.6	
SCLK Clock Frequency	f_{SCLK}				400	kHz

Note 2: The MAX24101 is 100% production tested at T_A = +25°C and T_A = +85°C**.** Specification at T_A = -40°C is guaranteed by design or characterization, unless otherwise noted.

Note 3: Guaranteed by design and characterization.

Note 4: Measured with circuit board loss optimized for best DJ. Residual jitter is the difference in deterministic jitter between the reference data source and device output. DJRESIDUAL = DJOUTPUT – DJSOURCE. The deterministic jitter at the output of the transmission line must be from media induced loss. Measured at point D in Figure 2. Test Patter: 66 Zeroes, 1010, PRBS7, 66 ones, 0101 Inverted PRBS7.

Note 5: The output voltage range in which a linear relationship between the input and output maintains less than or equal to 1dB compression.

Note 6: Measured using a vector-network analyzer (VNA) with -15dBm power level applied to the adjacent input. The VNA detects the signal at the output of the victim channel. All other inputs and outputs are terminated with 50Ω.

Note 7: Refer to UM10204: I²C-bus specification and user manual, Rev. 03 – 19 June 2007.

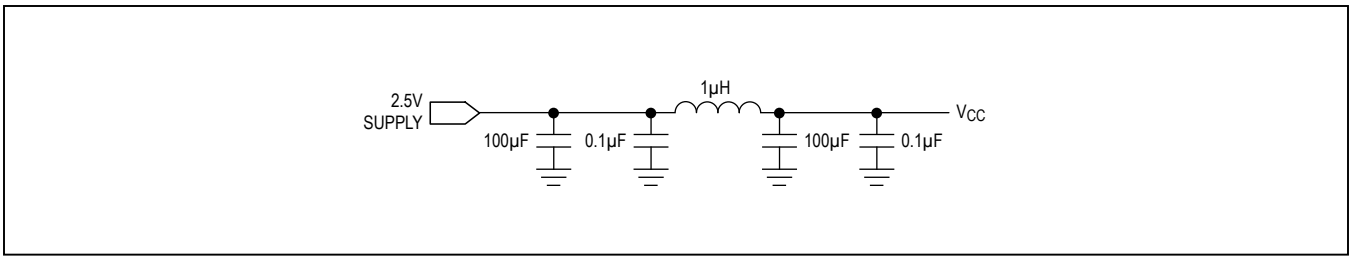


Figure 1. Recommended Supply Filtering

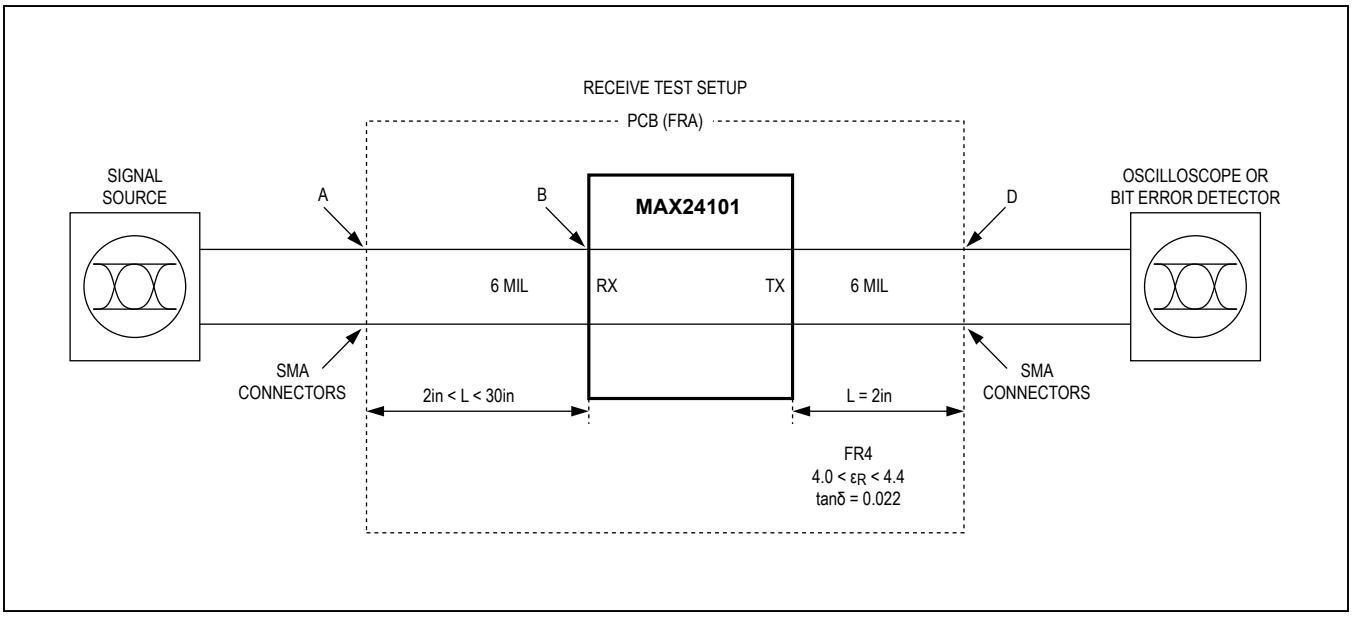


Figure 2. Receiver Test Setup (Points Labeled A, B, and D are Referenced for AC Parameter Test Conditions)

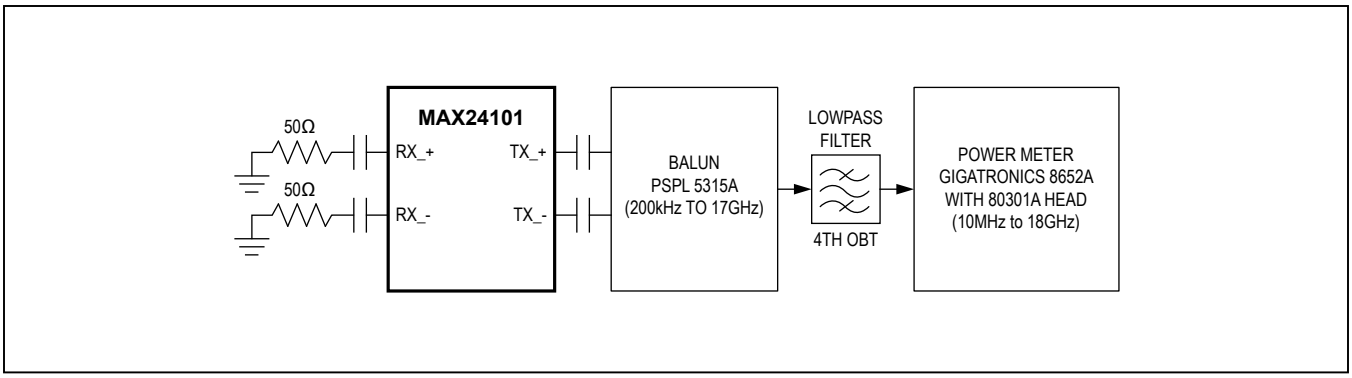


Figure 3. Noise Test Configuration

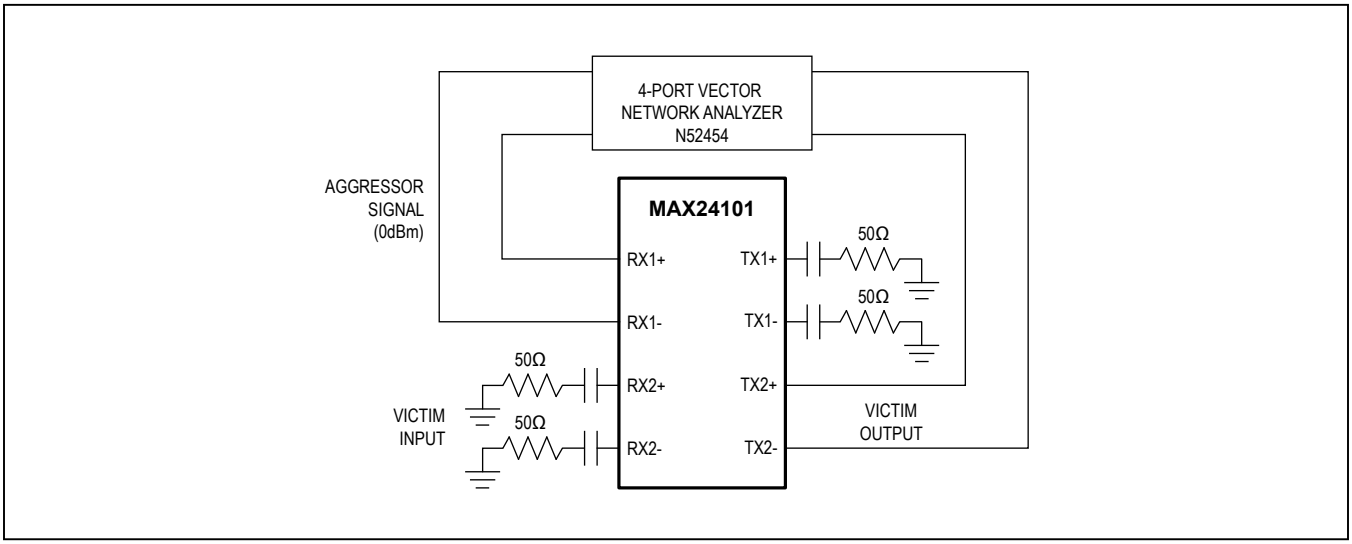
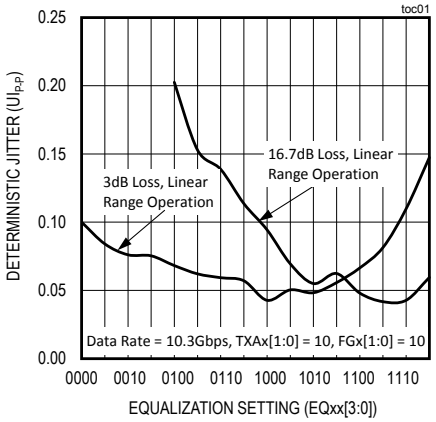


Figure 4. Channel-Isolation Test Configuration

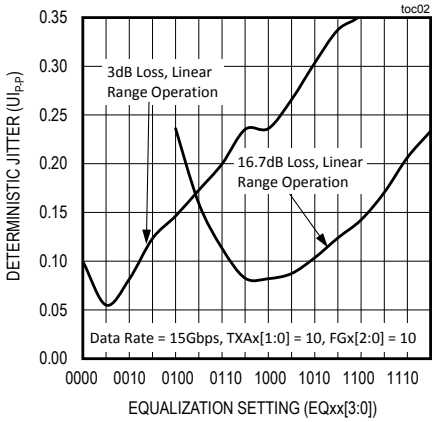
Typical Operating Characteristics

(Typical values are at V_{CCR} = V_{CCT} = V_{CC_DG} = 2.5V, T_A = +25°C, unless otherwise noted.)

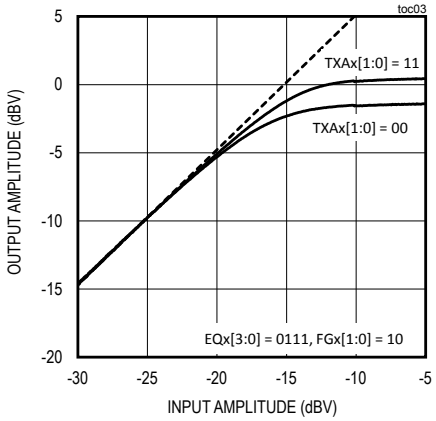
DETERMINISTIC JITTER vs. EQUALIZATION SETTING



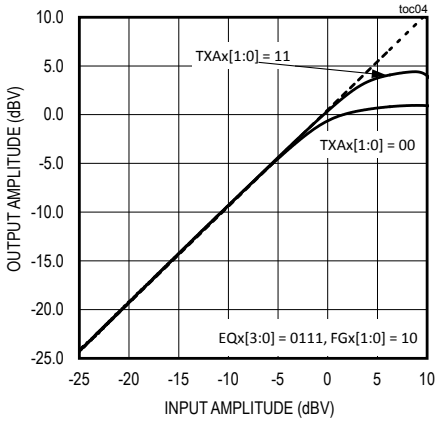
DETERMINISTIC JITTER vs. EQUALIZATION SETTING



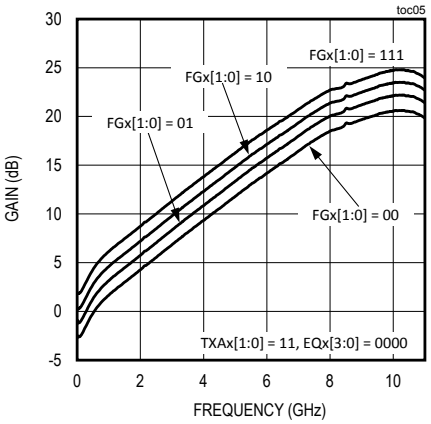
1dB Compression (7.5GHz Nyquist)



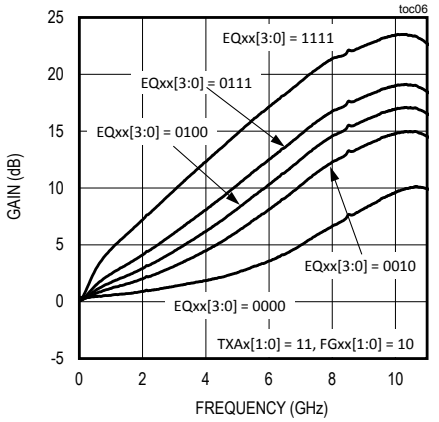
1dB COMPRESSION (100MHz Nyquist)



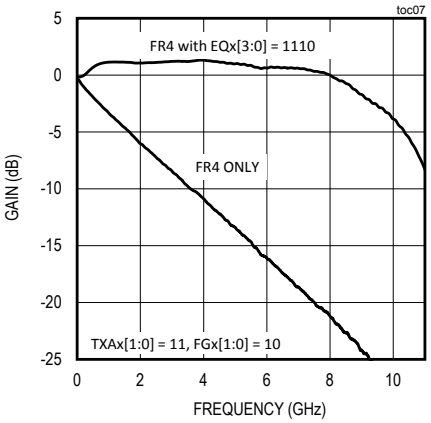
FREQUENCY RESPONSE



FREQUENCY RESPONSE



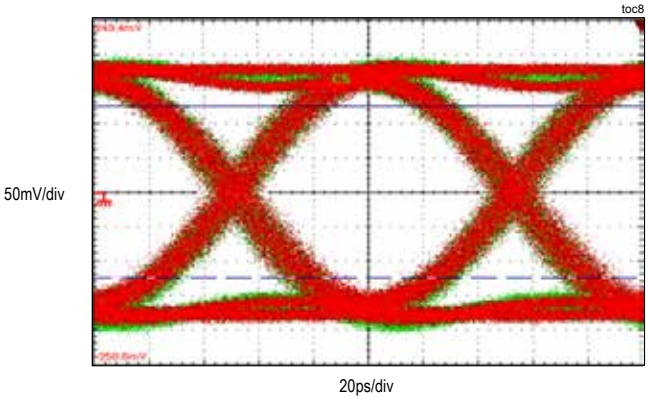
FREQUENCY RESPONSE WITH 18in of FR4



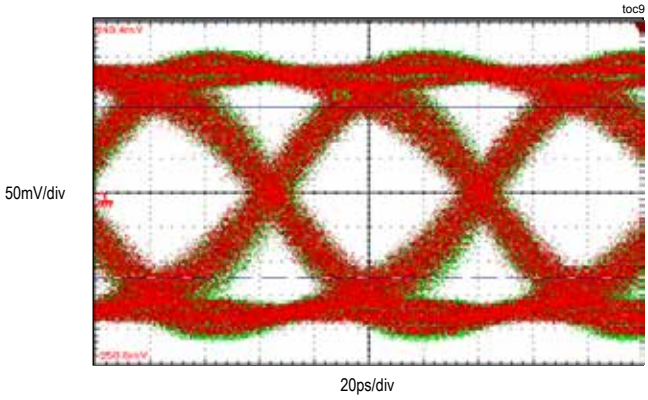
Typical Operating Characteristics (continued)

(Typical values are at V_{CCR} = V_{CCT} = V_{CC_DG} = 2.5V, T_A = +25°C, unless otherwise noted.)

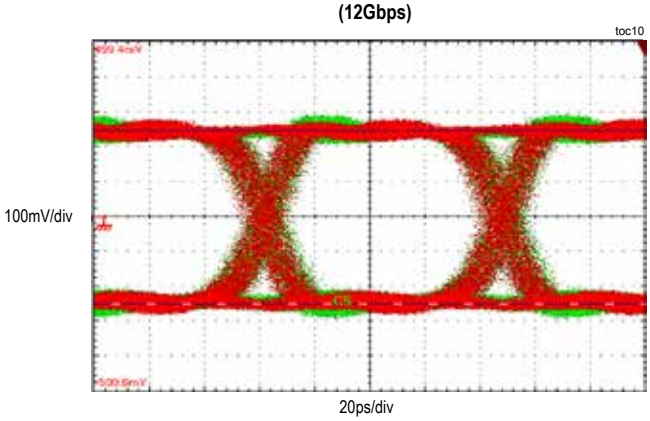
MAX24101 SINGLE-ENDED OUTPUT AFTER 18in FR4 AT INPUT (EQx[3:0] = 1110, FGx[1:0] = 01, TXAx[1:0] = 11, 10.3Gbps)



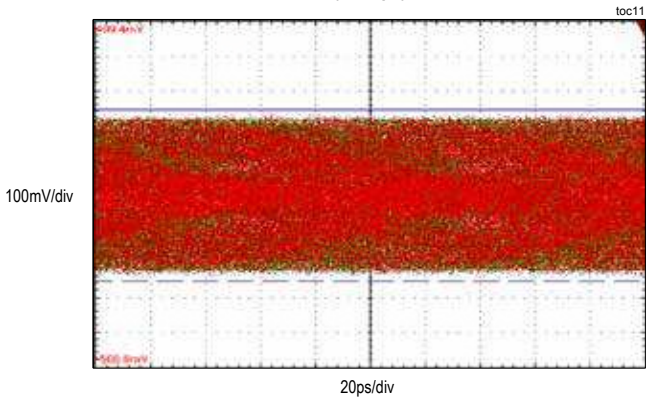
MAX24101 SINGLE-ENDED OUTPUT AFTER 18in OF INPUT FR4 (EQx[3:0] = 1110, FGx[1:0] = 01, TXAx[1:0] = 11, 13.5Gbps)



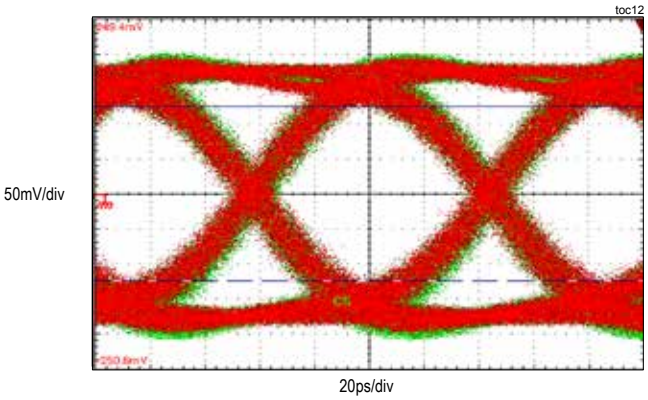
SINGLE-ENDED OUTPUT FROM BERT SOURCE (12Gbps)



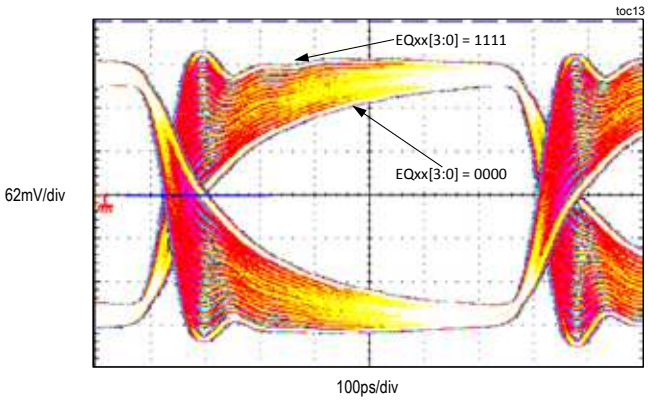
SINGLE-ENDED OUTPUT FROM BERT SOURCE AFTER 18in FR4 (12Gbps)



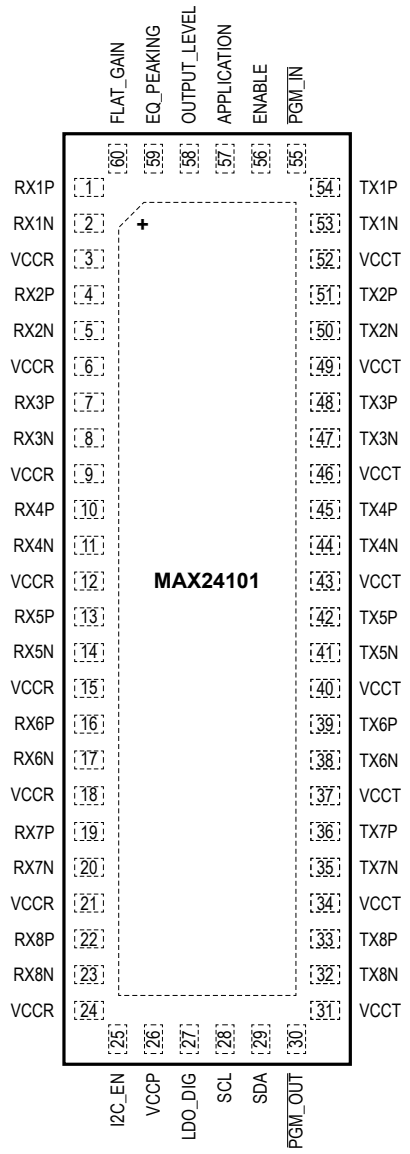
MAX24101 SINGLE-ENDED OUTPUT AFTER 18in FR4 AT INPUT (EQx[3:0] = 1110, FGx[1:0] = 01, TXAx[1:0] = 11, 12Gbps)



MAX24101 SINGLE-ENDED TIME DOMAIN OUTPUT VS. EQUALIZATION LEVEL (FGx[1:0] = 01, TXAx[1:0] = 11, WITH 18in FR4 AT 1Gbps)



Pin Configuration



FCLGA
4mm x 13mm

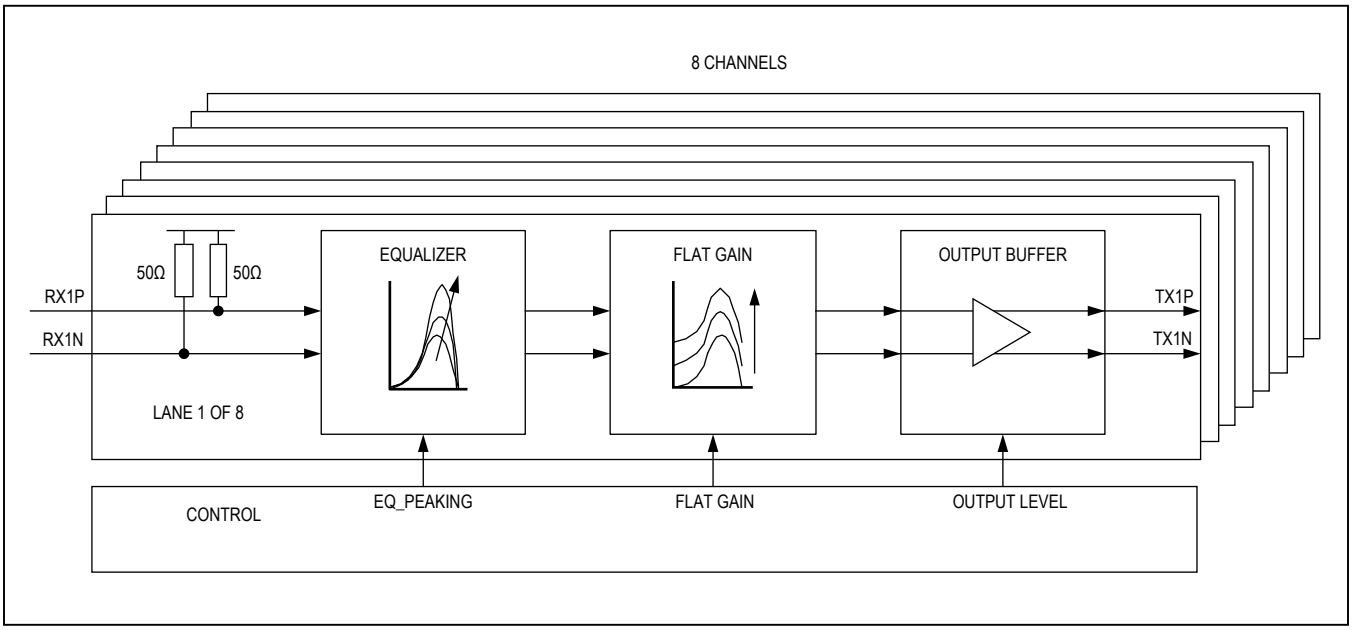
Pin Description

PIN	NAME	FUNCTION
1, 2	RX1P, RX1N	Differential Channel 1 Input, CML
3, 6, 9, 12, 15, 18, 21, 24	VCCR	Positive Receive Power Supply, 2.5V. Filter each pin with a 0.1µF capacitor to GND.
4, 5	RX2P, RX2N	Differential Channel 2 Input, CML

Pin Description (continued)

PIN	NAME	FUNCTION
7, 8	RX3P, RX3N	Differential Channel 3 Input, CML
10, 11	RX4P, RX4N	Differential Channel 4 Input, CML
13, 14	RX5P, RX5N	Differential Channel 5 Input, CML
16, 17	RX6P, RX6N	Differential Channel 6 Input, CML
19, 20	RX7P, RX7N	Differential Channel 7 Input, CML
22, 23	RX8P, RX8N	Differential Channel 8 Input, CML
25	I2C_EN	I^2C Enable Input, LVCMOS. Hardwire low for pin control. Hardwire high for I^2C control. User must select mode of operation before power-on reset.
26	VCCP	Positive Power Supply, 2.5V. Filter each pin with a 0.1µF capacitor to GND.
27	LDO_DIG	Compensation capacitor pin for internal LDO. Bypass pin with a 0.22µF capacitor to GND.
28	SCL	Analog I^2C Serial-Interface Clock Input. Use external 4.7kΩ pullup to V_{CC}.
29	SDA	Analog I^2C Serial-Interface Data Input and Output. Use external 4.7kΩ pullup to V_{CC}.
30	$\overline{PGM\_OUT}$	Cascadable I^2C Output. LVCMOS. See the *Slave Address Configuration* section.
31, 34, 37, 40, 43, 46, 49, 52	VCCT	Positive Transmit Power Supply, 2.5V. Filter each pin with a 0.1µF capacitor to GND.
32, 33	TX8N, TX8P	Differential Channel 8 Output, CML
35, 36	TX7N, TX7P	Differential Channel 7 Output, CML
38, 39	TX6N, TX6P	Differential Channel 6 Output, CML
41, 42	TX5N, TX5P	Differential Channel 5 Output, CML
44, 45	TX4N, TX4P	Differential Channel 4 Output, CML
47, 48	TX3N, TX3P	Differential Channel 3 Output, CML
50, 51	TX2N, TX2P	Differential Channel 2 Output, CML
53, 54	TX1N, TX1P	Differential Channel 1 Output, CML
55	$\overline{PGM\_IN}$	Cascadable I^2C Input. Has 30kΩ pulldown, see the *I^2C Address Configuration* section.
56	ENABLE	Power-Down Enable Pin, LVCMOS. Three-state pin to program the power mode of the part at startup. For high and open, see Table 5 for settings. Set low for reset. Reset, disables all communication to the chip along with resetting the registers to their default states.
57	APPLICATION	Application Select Input, LVCMOS. Select between channel cases: Short and Long. Set low or open for long. Set high for short.
58	OUTPUT_LEVEL	Output Level Control, LVCMOS. Three-state pin to program the output level of all channels. See Table 4 for settings.
59	EQ_PEAKING	Equalization Control Pin, LVCMOS. Three-state pin to program the equalization level of all channels. See Table 2 for settings.
60	FLAT_GAIN	Gain Adjust Control Pin, LVCMOS. Three-state pin to program the flat gain level of all channels. See Table 3 for settings.
—	EP	Exposed Pad. Internally connected to GND. Ground reference for power supplies, three-state, and other low-speed pins. Connect EP to a large ground plane to maximize thermal performance.

Functional Diagram



Detailed Description

The MAX24101 is an 8-channel linear equalizer (EQ) functioning up to 15Gbps. Each channel has a programmable equalization network and programmable flat gain adjust. All controls for equalization, gain, output enable/disable, etc., are individually programmed through the on-chip programming block. The programming block can be controlled either through pin controls or the I^2C serial bus.

APPLICATION Pin Control

The placement range of a linear equalizer is limited by its dynamic range and noise performance. To allow the widest placement range, the MAX24101 has two optimizations. The two cases are Short and Long Channels. By selecting the case based on channel loss as shown in Table 1, the best dynamic range and noise operating points are selected for the application.

Input Termination

The input termination consists of two 50Ω resistors forming a differential termination between the input pins. The excellent return loss minimizes reflections in a channel.

Table 1. APPLICATION Pin Control

INPUT LEVEL	CHANNEL LENGTH
High	Short Channel. 0dB to 18dB channel loss before MAX24101.
Low, Open	Long Channel. 18dB to 33dB channel loss before MAX24101.

Receive Equalizer

For the MAX24101, the input data goes into a selectable equalization stage. The receive equalizer is designed to compensate losses up to 19dB (at 7.5GHz) of channel loss. The selectable equalization can be controlled using commands sent over the I2C serial bus or pin control. With pin control the equalization setting has three available compensation levels and all the channels are controlled globally. See Table 2 for details. With the I2C serial bus, the equalization has 16 settings and each channel can be adjusted independently.

Gain Stage

The MAX24101 data path goes through a wideband flat gain stage. With pin control the flat gain can be adjusted globally from -2.9dB to +1.7dB as shown in Table 3. With I2C control, the flat gain can be adjusted independently for each channel.

Output Stage

The MAX24101 data path transitions from the gain stages into a linear output buffer with selectable output level. With pin control the output levels can be adjusted globally as shown in Table 4. With I2C control, the output levels can be adjusted independently for each channel.

Power Saving

The MAX24101 features a power-down enable input (ENABLE) pin to shut down the device and reduce supply current at startup. Set high to power down the output stage of all channels. Set open to power up all channels. Set low for reset. Reset disables all communication to the chip along with resetting the registers to their default states.

Table 2. EQ_PEAKING Pin Control

INPUT LEVEL	LONG CHANNEL (APPLICATION = LOW, OPEN)	MEDIUM CHANNEL (APPLICATION = OPEN)	SHORT CHANNEL (APPLICATION = HIGH)	UNITS
High	+15 (EQx[3:0] = 1110)	+15 (EQx[3:0] = 1110)	+12 (EQx[3:0] = 1001)	dB
Open	+12 (EQx[3:0] = 1001)	+12 (EQx[3:0] = 1001)	+9 (EQx[3:0] = 0101)	
Low	+9 (EQx[3:0] = 0101)	+9 (EQx[3:0] = 0101)	+6 (EQx[3:0] = 0011)	

Table 3. FLAT_GAIN Pin Control

INPUT LEVEL	LONG CHANNEL (APPLICATION = LOW, OPEN)	MEDIUM CHANNEL (APPLICATION = OPEN)	SHORT CHANNEL (APPLICATION = HIGH)	UNITS
High	1.7 (FGx[1:0] = 11)	1.7 (FGx[1:0] = 11)	0.1 (FGx[1:0] = 10)	dB
Open	0.1 (FGx[1:0] = 10)	0.1 (FGx[1:0] = 10)	-1.4 (FGx[1:0] = 01)	
Low	-1.4 (FGx[1:0] = 01)	-1.4 (FGx[1:0] = 01)	-2.9 (FGx[1:0] = 00)	

Table 4. OUTPUT_LEVEL Pin Control

INPUT LEVEL	OUTPUT AMPLITUDE	UNITS
High	1000 (TXAx[1:0] = 11]	mV_{P-P}
Open	940 (TXAx[1:0] = 10]	
Low	700 (TXAx[1:0] = 01]	

Table 5. ENABLE and Reset Pin Control

INPUT LEVEL (ENABLE)	I2C CONTROL MODE (I2C_EN = high)	PIN CONTROL MODE (I2C_EN = low)
High	Upon POR or reset, power down all channels	Power down all channels
Open	Upon POR or reset, power on all channels	Power on all channels
Low	Reset (POR)	Reset (POR)

Applications Information

Linear Equalizer (EQ) Placement and Use, in 3 Steps

Placement of linear equalizers in lossy channels is bounded by output linearity and input noise (I_{RN}). See Figure 5. Although placement is quite flexible, it is important to maintain linear operation with sufficient SNR, hence the boundary conditions stated in the following two sections.

Definitions

dBV is defined as dB relative to $1V_{P-P}$ (differential). Hence, the Tx level of $1V_{P-P}$ is 0dBV, and a Tx level of $0.5V_{P-P}$ is -6dBV.

Source Tx Level [dBV] is the total measured Tx V_{P-P}, including pre-emphasis.

Desired Margin is a user decision regarding margin needed to account for all system min/max variations, including source Tx, MAX24101, and ASIC receiver.

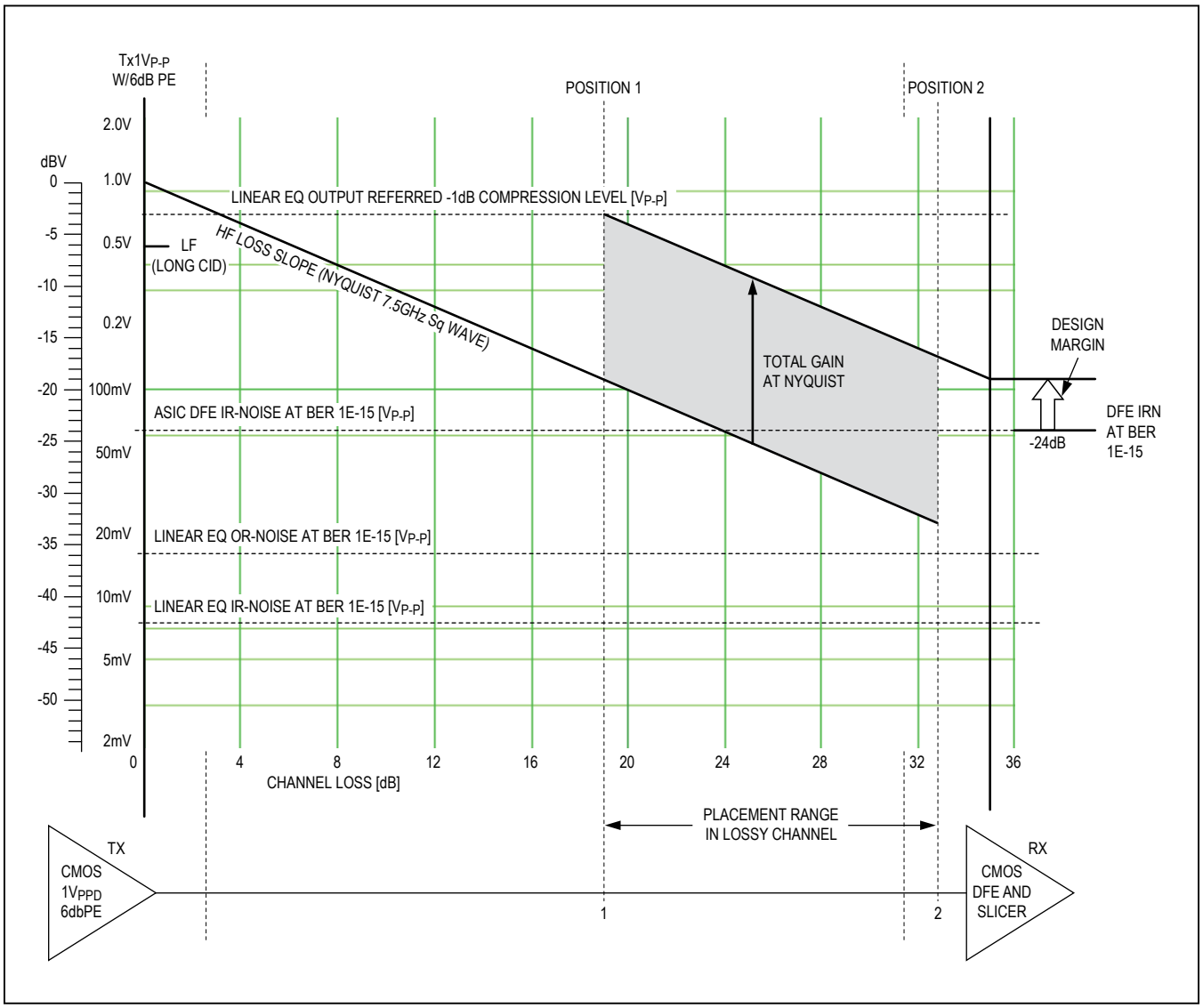


Figure 5. Linear Equalizer Placement

Step 1—Maintain EQ Linearity at Low Frequency (LF)

The source Tx low frequency (LF) amplitude needs to be considered to keep linear EQ within its linear range. The source Tx low-frequency (LF) amplitude is the differential peak-peak amplitude after any pre-emphasis has fully settled, e.g., the level of long CID (continuous identical digits) sequences. The primary controls over LF levels in Linear EQ are the Used ASIC Source Tx pre-emphasis (or de-emphasis) and the Linear EQ Flat Gain (MAX24101).

Figure 5 shows a typical example with ASIC Source Tx having 6dB pre-emphasis, with $1V_{P-P}$ peak swing and $0.5V_{P-P}$ swing after pre-emphasis (e.g., long CID LF content). Note that $0.5V_{P-P}$ fits easily under the -1dB Compression line. If the Source Tx were to have higher LF swing, driving linear EQ into nonlinearity, the linear EQ flat-gain control can be used to attenuate input signal level, as needed, to maintain linearity.

For example:

Maximum Linear EQ Flat Gain setting =

Linear EQ Output Level setting (-1dB compression) [dBV] -

Source Tx Level [dBV] +

Source Tx Pre-Emphasis (De-emphasis) [dB] -

User System Margin [dB]

For example:

Linear EQ Output Level setting (-1dB compression) [dBV] = -3dBV

Source Tx Level [dBV] = 0dB

Source Tx Pre-Emphasis (De-emphasis) [dB] = 6dB

User System Margin = 2dB

Then:

Maximum Linear EQ Flat Gain setting = (-3) - 0 + 6 - 2 = 1dB

(There are three Flat Gain settings available lower than +1dB: They are -3dB, -1.5dB, 0dB)

Step 2—Maintain EQ Linearity at High Frequency (Nyquist)

A linear equalizer when placed too close to a Source Tx is vulnerable to nonlinear compression at high frequency (Nyquist), especially if the EQ peaking gain is higher than the preceding channel loss. The -1dB compression specification gives maximum output level that guarantees linear operation. As a function of the EQ settings, the minimum placement distance from the Source Tx is calculated as follows: (see **Position 1** in Figure 5).

Minimum Distance (Nyquist Loss) from Source Tx [dB] =

Source Tx Level [dBV] +

Linear EQ Peaking Gain [dB] +

Linear EQ Flat Gain [dB] –

Linear EQ Output Level setting (-1dB Compression level) [dBV] +

User System Margin [dB]

For example:

Source Tx Level = 0dBV

Linear EQ Peaking Gain = 14dB

Linear EQ Flat Gain = 0dB

Linear EQ Output Level setting (-1dB Compression Point) = -3dBV

User System Margin = 2dB

Then:

Minimum Distance (Nyquist Loss) from Source Tx = 0 + 14 + 0 - (-3) + 2 = 19dB

Step 3—Keep Nyquist Level Sufficiently Above Noise Floor

The amplitude of the Nyquist sequence (10101010…) must be maintained sufficiently above noise floor to achieve BER goals. Hence, Nyquist level at input to the Linear EQ needs to be sufficiently above the Linear EQ self-noise, IRN (input referred noise). This sets the maximum Nyquist channel loss preceding the Linear EQ, e.g, farthest placement from Source Tx (see **Position 2** in Figure 5).

Maximum Distance (Nyquist Loss) from Source Tx [dB] =

Source Tx Level (which is Nyquist level) [dBV] –

Linear EQ IRNpp at BER goal [dBV] –

Margin required to reduce RJ creation –

User System Margin [dB]

For example:

Source Tx Level = 0dBV

Linear EQ IRNpp at BER goal (0.5mVrms x 15.9 at BER 1E-15) [dBV] = -43dB

Margin required to reduce RJ creation (to 0.2UIpp at BER) = 10dB

User System Margin = 3dB

Then:

Maximum Distance (Nyquist Loss) from Source Tx = 0 - (-43) - 10 - 3 = 30dB

Tools—Frequency Response Plotting and EQ Placement in Channel Calculator

Several simple Microsoft® Excel spreadsheet tools are available to assist in the application of the MAX24101 Linear EQs. Please visit www.maximintegrated.com to access the latest version of these spreadsheets:

I²C Interface

The SDA and SCL pins are referred to as the slave I²C. The slave I²C provides external access to the register set within the MAX24101. Typically, an MCU is connected to the slave I²C.

Framing and Data Transfer

An individual transaction is framed by a START condition and a STOP condition. A START condition occurs when a bus master pulls SDA low while SCL is high. A STOP condition occurs when the bus master allows SDA to transition low-to-high when SCL is high. Within the frame the master has exclusive control of the bus. The MAX24101 supports Repeated START conditions whereby the master may simultaneously end one frame and start another without releasing the bus by replacing the STOP condition with a START condition.

Within a frame the state of SDA only changes when SCL is low. A data bit is transferred on a low-to-high transition of SCL. Data is arranged in packets of 9 bits. The first 8 bits represent data to be transferred (most significant bit (MSB) first). The last bit is an acknowledge bit from the slave. The recipient of the data holds SDA low during the ninth clock cycle of a data packet to acknowledge (ACK) the byte. Leaving SDA left open on the ninth bit signals a not-acknowledged (NACK) condition. The interpretation of the acknowledge bit by the sender depends on the type of transaction and the nature of the byte being received. SDA is bidirectional so that the master may send data bytes during write transactions and the slave may send data bytes during reads.

Device Addressing

The first byte to be sent after a START condition is a slave address byte. The first seven bits of the byte contain the target slave address (MSB first). The eighth bit indicates the transaction type – '0' = write, '1' = read. Each slave interface on the bus is assigned a 7-bit slave address. If no slave matches the address broadcast by the master then SDA will be left open during the acknowledge bit and the master receives a NACK. The master must then assert a STOP condition. If a slave identifies the address then it acknowledges it by pulling SDA low. The master then proceeds with the transaction identified by the type bit. The two-wire interface of the MAX24101 decodes slave addresses ranging from 00h to 3Fh.

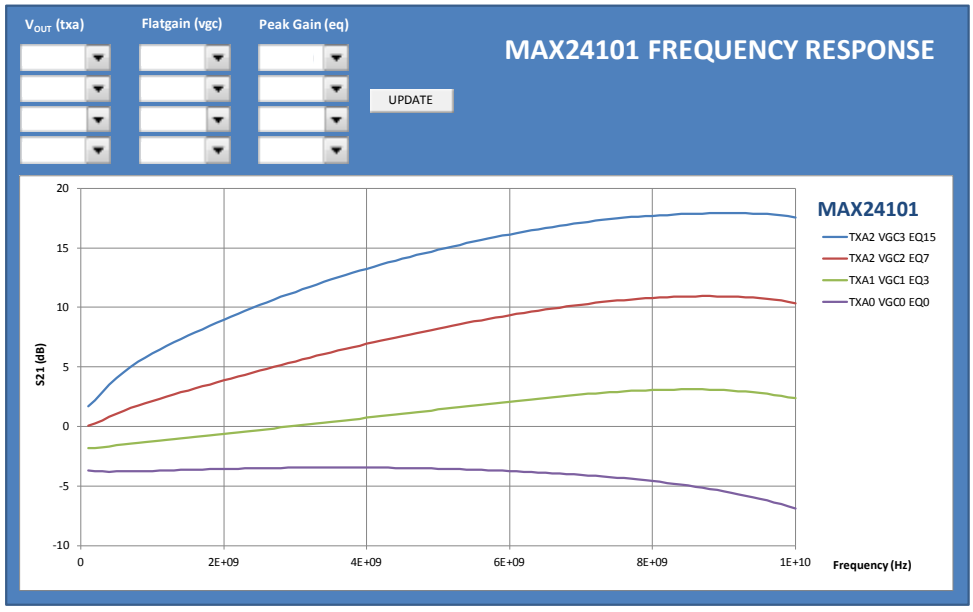


Figure 6. Frequency Response Plotting

Microsoft Excel is a registered trademark of Microsoft Corp.

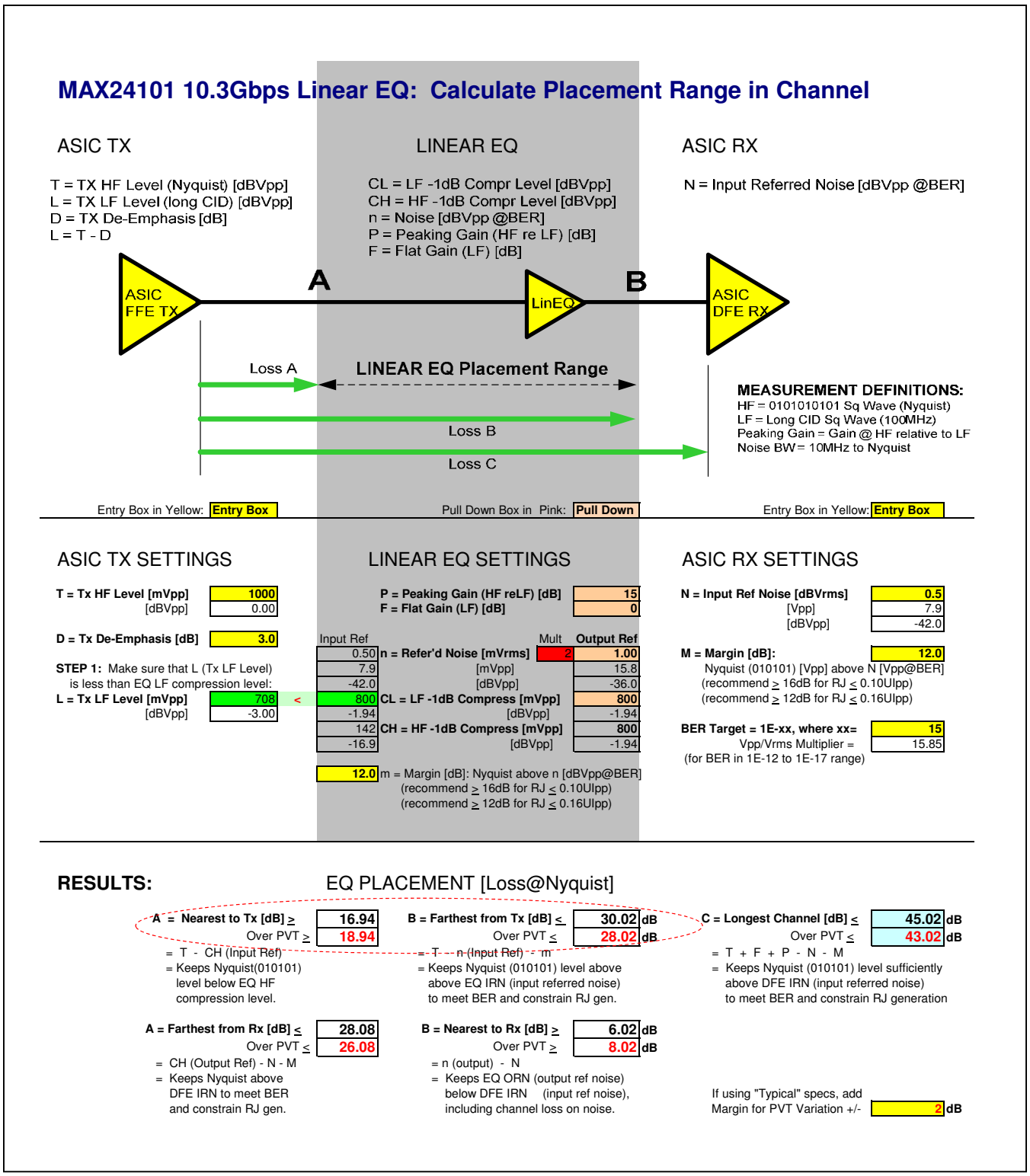


Figure 7. EQ Placement Calculator

Write Transaction

In a write transaction, the address byte is successfully acknowledged by the slave, and the type bit is set low. After the first acknowledge, the master sends a single data byte. All signaling is controlled by the master except for the SDA line during the acknowledge bits. During the acknowledge cycle the direction of the SDA line is reversed and the slave pulls SDA low to return a '0' (ACK) to the master.

The MAX24101 interprets the first data byte as a register address. This is used to set an internal memory pointer. Subsequent data bytes within the same transaction will then be written to the memory location addressed by the pointer. The pointer is auto-incremented after each byte. There is no limit to the number of bytes which may be written in a single burst to the internal registers of the MAX24101.

Read Transaction

In a read transaction, the slave address byte is successfully acknowledged by the slave, and the type bit is set high. After the ACK the slave returns a byte from the location identified by the internal memory pointer. This pointer is then auto-incremented. The slave then releases SDA so that the master can ACK the byte. If the slave receives an ACK then it will send another byte. The master identifies the last byte by sending a NACK to the slave. The master then issues a STOP to terminate the transaction.

Thus, to implement a random access read transaction, a write must first be issued by the master containing a slave address byte and a single data byte (the register address). This sets up the memory pointer. A read is then sent to retrieve data from this address.

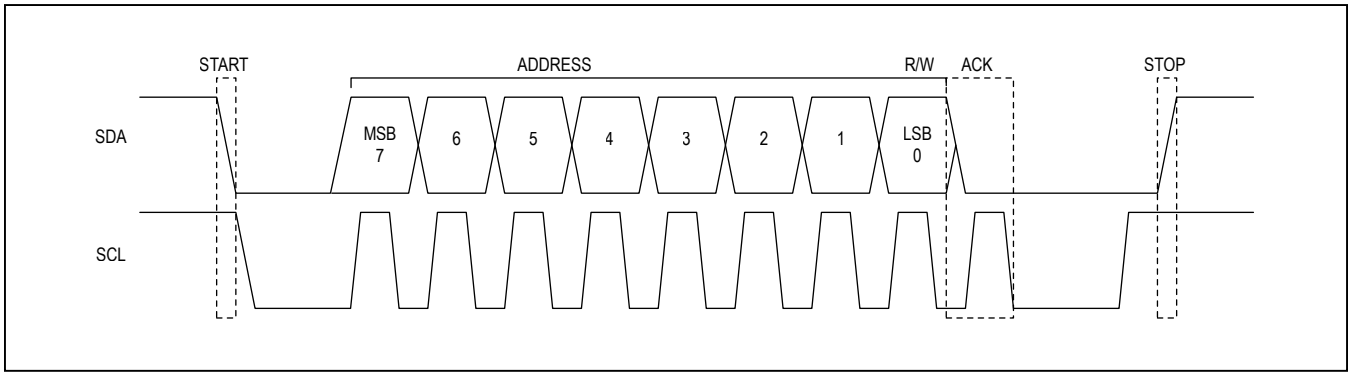


Figure 8. Device Addressing

I²C Access Destination

The MAX24101 does not provide any security level on the I²C serial bus. Accesses to unimplemented registers in the device are discarded in the case of a write, and return an unpredictable value in the case of a read. During burst mode accesses, destination addresses are tested on a byte-by-byte basis.

Slave Address Configuration

The slave address of the MAX24101 I²C can be set using an initialization procedure involving $\overline{PGM\_IN}$ and $\overline{PGM\_OUT}$, in conjunction with the standard I²C signals. This procedure facilitates the assignment of a large number of slave addresses, enabling several MAX24101s to be controlled by a single I²C serial bus and commands. All transactions on the I²C bus follow standard protocol, allowing simple firmware development.

There is little difference between a normal I²C serial bus and the MAX24101 solution except that there is a new signal which controls the programming of the device addresses. This signal is daisy-chained through all of the devices on the I²C bus via the $\overline{PGM\_IN}$ and the $\overline{PGM\_OUT}$ pins. The programming of device addresses is done as a single parallel write to all devices 1 to N.

The I²C bus is the usual “SCL” and bidirectional “SDA” with the pullup. The “program_reset” signal is a single bit passed through each device as a flying enable. The input pin for this signal is $\overline{PGM\_IN}$ and the corresponding output pin is $\overline{PGM\_OUT}$. The $\overline{PGM\_IN}$ pin on the first MAX24101 in the chain can be tied low or left unconnected because the $\overline{PGM\_IN}$ pin has an internal pulldown resistor.

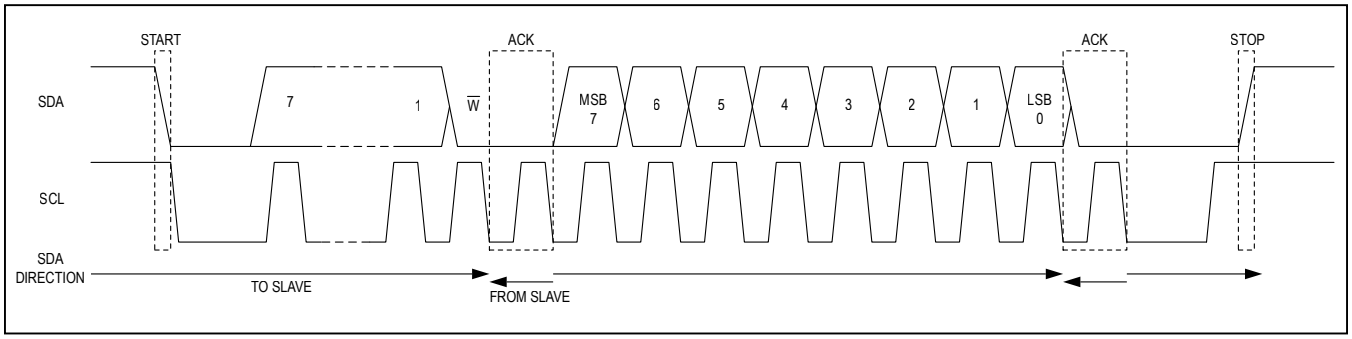


Figure 9. Write Transaction

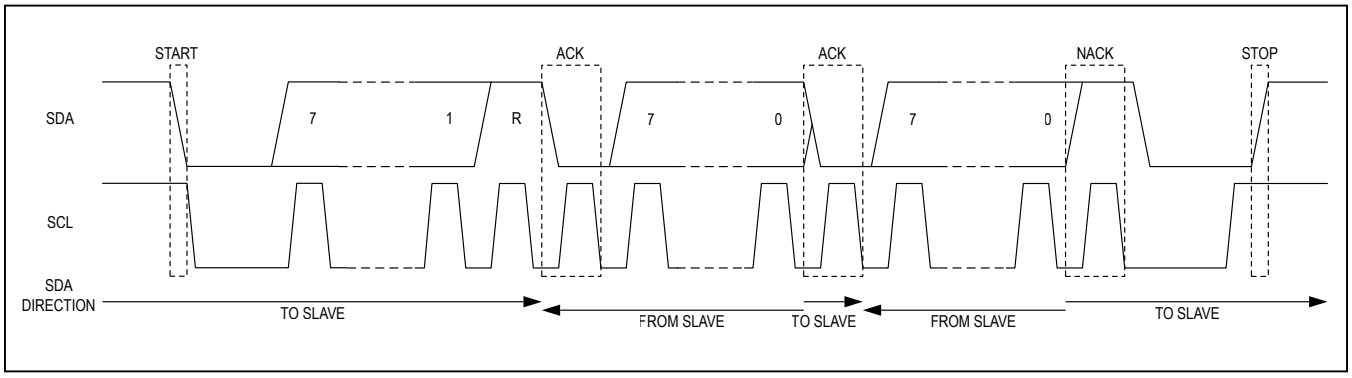


Figure 10. Read Transaction

I2C Address Configuration

The new features of this interface compared to a conventional I2C interface are:

- The daisy chain $\overline{\text{PGM\_IN}}$ and $\overline{\text{PGM\_OUT}}$ pins
- A device_address register (7 bits[7:1]). Bit[0] in this register is used as a I2C read/write bit
- An internal “write_once” bit

At power-up, the “write_once” bit will be set to ‘1’ and the device I2C address will be set to its default value (A2h). All MAX24101 devices will respond to read and writes to this slave address until a write to register 3Ch is performed. The required I2C address of device 1 (“7 bit address”+’0’) is then assigned by writing to pgm_register (3Ch) at I2C address A2h. All devices accept the new address value (for example: 10h). Each device then starts to increment it on SCL edges while $\overline{\text{PGM\_IN}}$ is high. The “program_reset” signal ripples down the chain, fixing the I2C address such that device N has an I2C address of (“address”+’0’)+2*N-1 (for example: device 1 at (10h and 12h), device 2 at (14h and 16h) and device 3 at (18h and 1Ah)). Note that each MAX24101 takes two I2C addresses with channels 1 to 4 being controlled by the lower address and channels 5 to 8 from the upper address.

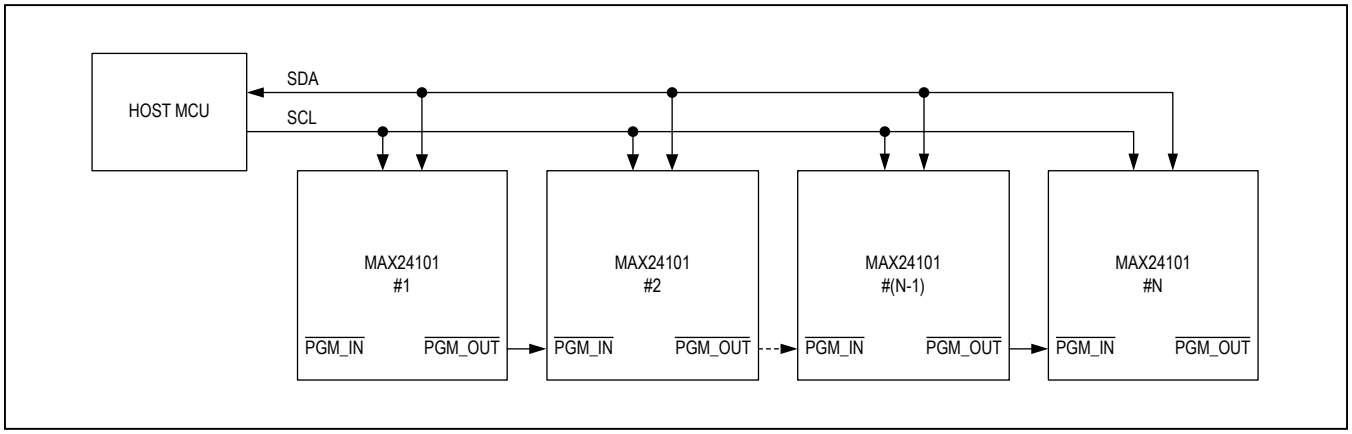


Figure 11. Slave Address Configuration

Startup Sequence

In this example, a chain of MAX24101s are loaded with the required I²C slave address.

1) Power up the devices.
2) Write I²C sequence < “A2h” ack “3Ch” ack “address” and ‘0’ ack>.
3) The first device is now accessible at its given address (“address” and ‘0’ for the lower channels and “address+1” and ‘0’ for the upper channels).
4) By accessing the first device, the SCL pin is toggled and hence the “program_reset” signal is propagated through the devices using the $\overline{\text{PGM\_IN}}$ and $\overline{\text{PGM\_OUT}}$ pins. For long chains, a number of accesses may be needed before all devices have an assigned address since each access results in 27 SCL transitions and hence 13 devices are allocated an address

To reset the slave address requires a power cycle or setting the ENABLE pin low.

Programming Tables

Table 6. EQ_PEAKING Bit Control

EQx[3:0]	EQ PEAKING GAIN	UNITS
1111	19.0	dB
1110	18.5	
1101	18.0	
1100	17.5	
1011	17.0	
1010	16.4	
1001	15.8	
1000	15.1	
0111	14.4	
0110	13.6	
0101	12.7	
0100	11.7	
0011	10.6	
0010	9.3	
0001	7.8	
0000	6.0	

Table 7. FLAT_GAIN Bit Control

FGx[1:0]	FLAT GAIN	UNITS
11	1.68	dB
10	0.14	
01	-1.36	
00	-2.87	

Table 8. OUTPUT_LEVEL Bit Control

TXAx[1:0]	OUTPUT LEVEL	UNITS
11	1000	mV_{P-P}
10	940	
01	700	
00	600	

Register Map

Table 9. Register Configuration

ADDRESS	LOWER I²C ADDRESS	UPPER I²C ADDRESS
00h	Reserved (read only)	Reserved (read only)
01h	Channel 1	Channel 5
02h	Channel 2	Channel 6
03h	Channel 3	Channel 7
04h	Channel 4	Channel 8
05h	Channel 1–4 Controls	Channel 5–8 Controls
06h	Reserved	Reserved
07h	Reserved	Reserved
08h	Reserved	Reserved
3Ch	I²C address	I²C address

The register map is split into two sections depending on the I²C address used. In general the lower address controls the lower four channels and the upper I²C address controls the upper four channels.

Register 01h (Lower I²C Address): Channel 1

BIT	7	6	5	4	3	2	1	0
NAME	EQ1[3]	EQ1[2]	EQ1[1]	EQ1[0]	FG1[1]	FG1[0]	TXA1[1]	TXA1[0]
DEFAULT VALUE	0	0	0	0	0	0	0	0
ACCESS	RW	RW	RW	RW	RW	RW	RW	RW

EQ1[3:0]: Sets the equalizer peaking for channel 1. See Table 6 for values.
FG1[1:0]: Sets the flat gain for channel 1. See Table 7 for values.
TXA1[1:0]: Sets the output amplitude for channel 1. See Table 8 for values.

Register 02h (Lower I²C Address): Channel 2

BIT	7	6	5	4	3	2	1	0
NAME	EQ2[3]	EQ2[2]	EQ2[1]	EQ2[0]	FG2[1]	FG2[0]	TXA2[1]	TXA2[0]
DEFAULT VALUE	0	0	0	0	0	0	0	0
ACCESS	RW	RW	RW	RW	RW	RW	RW	RW

EQ2[3:0]: Sets the equalizer peaking for channel 2. See Table 6 for values.
FG2[1:0]: Sets the flat gain for channel 2. See Table 7 for values.
TXA2[1:0]: Sets the output amplitude for channel 2. See Table 8 for values.

Register 03h (Lower I2C Address): Channel 3

BIT	7	6	5	4	3	2	1	0
NAME	EQ3[3]	EQ3[2]	EQ3[1]	EQ3[0]	FG3[1]	FG3[0]	TXA3[1]	TXA3[0]
DEFAULT VALUE	0	0	0	0	0	0	0	0
ACCESS	RW	RW	RW	RW	RW	RW	RW	RW

EQ3[3:0]: Sets the equalizer peaking for channel 3. See Table 6 for values.
FG3[1:0]: Sets the flat gain for channel 3. See Table 7 for values.
TXA3[1:0]: Sets the output amplitude for channel 3. See Table 8 for values.

Register 04h (Lower I2C Address): Channel 4

BIT	7	6	5	4	3	2	1	0
NAME	EQ4[3]	EQ4[2]	EQ4[1]	EQ4[0]	FG4[1]	FG4[0]	TXA4[1]	TXA4[0]
DEFAULT VALUE	0	0	0	0	0	0	0	0
ACCESS	RW	RW	RW	RW	RW	RW	RW	RW

EQ4[3:0]: Sets the equalizer peaking for channel 3. See Table 6 for values.
FG4[1:0]: Sets the flat gain for channel 3. See Table 7 for values.
TXA4[1:0]: Sets the output amplitude for channel 3. See Table 8 for values.

Register 05h (Lower I2C Address): Channel 1–4 Controls

BIT	7	6	5	4	3	2	1	0
NAME	Reserved	Reserved	Reserved	REGCONT14	CH1OFF	CH2OFF	CH3OFF	CH4OFF
DEFAULT VALUE	0	0	0	0	0	0	0	0
ACCESS	RW	RW	RW	RW	RW	RW	RW	RW

REGCONT14: Selects channel settings, for channels 1–4, from pin control or I²C accessible registers. 0 = pin control (equalizer peaking, flat gain and output amplitude), 1 = I2C accessible registers.
CH1OFF: Disables channel 1. 0 = enabled, 1 = disabled.
CH2OFF: Disables channel 2. 0 = enabled, 1 = disabled.
CH3OFF: Disables channel 3. 0 = enabled, 1 = disabled.
CH4OFF: Disables channel 4. 0 = enabled, 1 = disabled.

Register 01h (Upper I2C Address): Channel 5

BIT	7	6	5	4	3	2	1	0
NAME	EQ5[3]	EQ5[2]	EQ5[1]	EQ5[0]	FG5[1]	FG5[0]	TXA5[1]	TXA5[0]
DEFAULT VALUE	0	0	0	0	0	0	0	0
ACCESS	RW	RW	RW	RW	RW	RW	RW	RW

EQ5[3:0]: Sets the equalizer peaking for channel 5. See Table 6 for values.
FG5[1:0]: Sets the flat gain for channel 5. See Table 7 for values.
TXA5[1:0]: Sets the output amplitude for channel 5. See Table 8 for values.

Register 02h (Upper I2C Address): Channel 6

BIT	7	6	5	4	3	2	1	0
NAME	EQ6[3]	EQ6[2]	EQ6[1]	EQ6[0]	FG6[1]	FG6[0]	TXA6[1]	TXA6[0]
DEFAULT VALUE	0	0	0	0	0	0	0	0
ACCESS	RW	RW	RW	RW	RW	RW	RW	RW

EQ6[3:0]: Sets the equalizer peaking for channel 6. See Table 6 for values.
FG6[1:0]: Sets the flat gain for channel 6. See Table 7 for values.
TXA6[1:0]: Sets the output amplitude for channel 6. See Table 8 for values.

Register 03h (Upper I2C Address): Channel 7

BIT	7	6	5	4	3	2	1	0
NAME	EQ7[3]	EQ7[2]	EQ7[1]	EQ7[0]	FG7[1]	FG7[0]	TXA7[1]	TXA7[0]
DEFAULT VALUE	0	0	0	0	0	0	0	0
ACCESS	RW	RW	RW	RW	RW	RW	RW	RW

EQ7[3:0]: Sets the equalizer peaking for channel 7. See Table 6 for values.
FG7[1:0]: Sets the flat gain for channel 7. See Table 7 for values.
TXA7[1:0]: Sets the output amplitude for channel 7. See Table 8 for values.

Register 04h (Upper I2C Address): Channel 8

BIT	7	6	5	4	3	2	1	0
NAME	EQ8[3]	EQ8[2]	EQ8[1]	EQ8[0]	FG8[1]	FG8[0]	TXA8[1]	TXA8[0]
DEFAULT VALUE	0	0	0	0	0	0	0	0
ACCESS	RW	RW	RW	RW	RW	RW	RW	RW

EQ8[3:0]: Sets the equalizer peaking for channel 8. See Table 6 for values.
FG8[1:0]: Sets the flat gain for channel 8. See Table 7 for values.
TXA8[1:0]: Sets the output amplitude for channel 8. See Table 8 for values.

Register 05h (Upper I2C Address): Channel 5-8 Controls

BIT	7	6	5	4	3	2	1	0
NAME	Reserved	Reserved	Reserved	REGCONT58	CH5OFF	CH6OFF	CH7OFF	CH8OFF
DEFAULT VALUE	0	0	0	0	0	0	0	0
ACCESS	RW	RW	RW	RW	RW	RW	RW	RW

REGCONT58: Selects channel settings, for channels 5-8, from pin control or I²C accessible registers. 0 = pin control (equalizer peaking, flat gain and output amplitude), 1 = I2C accessible registers.
CH5OFF: Disables channel 5. 0 = enabled, 1 = disabled.
CH6OFF: Disables channel 6. 0 = enabled, 1 = disabled.
CH7OFF: Disables channel 7. 0 = enabled, 1 = disabled.
CH8OFF: Disables channel 8. 0 = enabled, 1 = disabled.

Exposed Pad Package

The exposed pad of the MAX24101 package incorporates features that provide a very low thermal resistance path for heat removal from the IC. The exposed pad on the MAX24101 must be soldered to the circuit board for proper thermal performance and correct electrical grounding. For more information on exposed-pad packages, refer to Maxim Application Note 862: HFAN-08.1: *Thermal Considerations of QFN and Other Exposed-Paddle Packages*.

Layout Considerations

Circuit board layout and design can significantly affect the performance of the MAX24101. Use good high-frequency design techniques, including minimizing ground inductance and using controlled-impedance transmission lines on the data signals. Power-supply decoupling should also be placed as close to the V_{CC} pins as possible. There should be sufficient supply filtering. Always connect all V_{CC}s to a power plane. Take care to isolate the input from the output signals to reduce feed through.

Interface Schematics

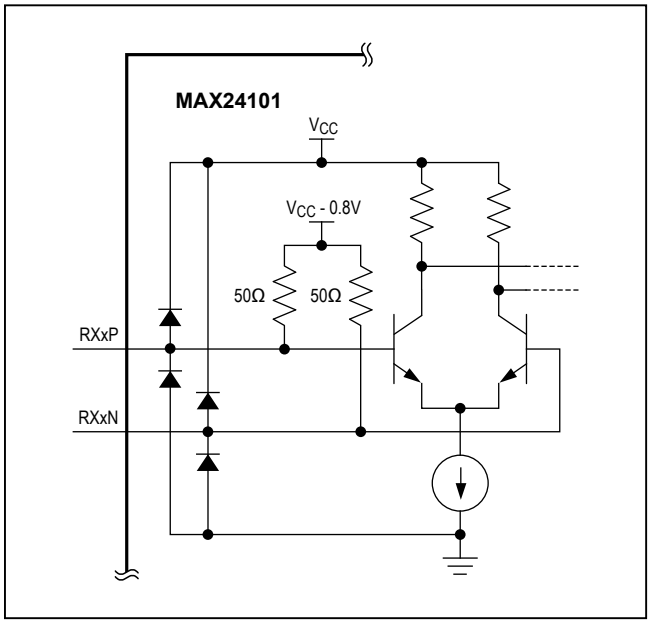


Figure 12. CML Equivalent Input Structure

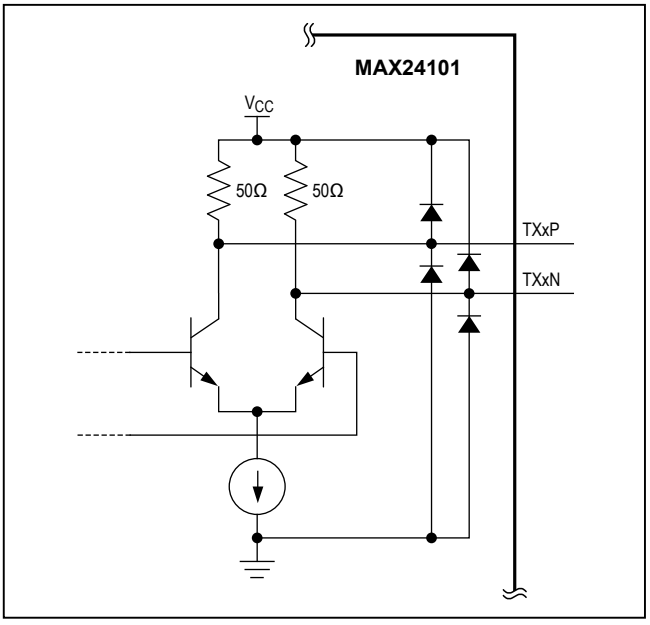


Figure 13. CML Equivalent Output Structure