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TCS3404, TCS3414

Digital Color Sensors

General Description

The TCS3404 and TCS3414 digital color light sensors are designed to accurately derive the color chromaticity and illuminance (intensity) of ambient light and provide a digital output with 16-bits of resolution. The devices include an 8 × 2 array of filtered photodiodes, analog-to-digital converters, and control functions on a single monolithic CMOS integrated circuit. Of the 16 photodiodes, 4 have red filters, 4 have green filters, 4 have blue filters, and 4 have no filter (clear). With the advanced patent pending in-package trim capability, device-to-device and system-to-system tolerance can be minimized allowing very precise repeatability to be attained.

A synchronization input (SYNC) provides precise external control of sensor integration allowing the internal conversion cycles to be synchronized to a pulsed light source. Furthermore, the synchronization feature supports the following advanced modes of operation to maximize flexibility across a broad range of hardware systems:

1. sync for one internal-time cycle, and
2. accumulate for specified number of pulses.

The device also supports free-running and serial-bus-controlled integration modes if precise coupling between the sensor and light source is not required.

Four parallel analog-to-digital converters (ADC) transform the photodiode currents to an SMBus (TCS3404) or I^2C (TCS3414) digital output that, in turn, can be input to a microprocessor. The RGB values can be read in a single read cycle to minimize the number of read command protocols defined in the communication interface. The slave address for this device is 39h (0111001b). A single SMB-Alert style interrupt (TCS3404) as well as a single traditional *level*-style interrupt (TCS3414) can be dynamically configured for any one of the four channels including a corresponding high/low threshold setting. The interrupt will remain asserted until the firmware clears the interrupt.

The TCS3404/14 devices can help

1. automatically adjust the display brightness of a backlight to extend battery, increase lamp life, and provide optimum viewing in diverse lighting conditions,
2. white-color balance display panel and/or captured images in diverse lighting conditions, and
3. manage RGB LED backlighting to maintain color consistency over a long period of time.

These devices are also ideal in controlling keyboard illumination in low ambient light conditions. Chromaticity coordinates (x,y) can be used to derive color temperature for the purpose of white-color balancing of displays and/or captured images. Illuminance, in lux, can be used to approximate the human eye response of ambient light and to manage exposure control in digital cameras. The TCS3404/14 devices are ideal in notebook/tablet PCs, LCD monitors, flat-panel televisions, cell phones, and digital cameras. Additional applications include street light control, security lighting, sunlight harvesting, and automotive instrumentation clusters.

Ordering Information and Content Guide appear at end of datasheet.

Key Benefits & Features

The benefits and features of TCS3404 and TCS3414, Digital Color Sensors are listed below:

Figure 1:
Added Value of Using TCS3404 and TCS3414

Benefits	Features
• User defined upper and lower threshold settings	• Programmable interrupt function
• Eliminates signal fluctuation due to AC light flicker	• Internal filter, no external capacitor required
• More accurate system to system repeatability	• In-package trim
• Up to 16-Bit output resolution	• 16-Bit digital output
• 1,000,000 to 1 dynamic range	• Programmable analog gain and integration time
• Synchronizes integration cycle with external modulated signal	• SYNC input
• Extended operating temperature range	• -40°C to 85°C (CS package) • -30°C to 70°C (FN package)
• 10% power supply operating range	• Operating voltage of 2.7V to 3.6V
• Smallest possible surface mount packages	• Available in both an FN and a CS package • The CS package is the smallest digital RGB color sensor

Applications

The applications of this device are:

- Provides method to derive chromaticity coordinates to manage display backlighting (i.e. RGB LED, CCFL, etc.)
- Provides means to derive color temperature to white-color balance displays under various lighting conditions

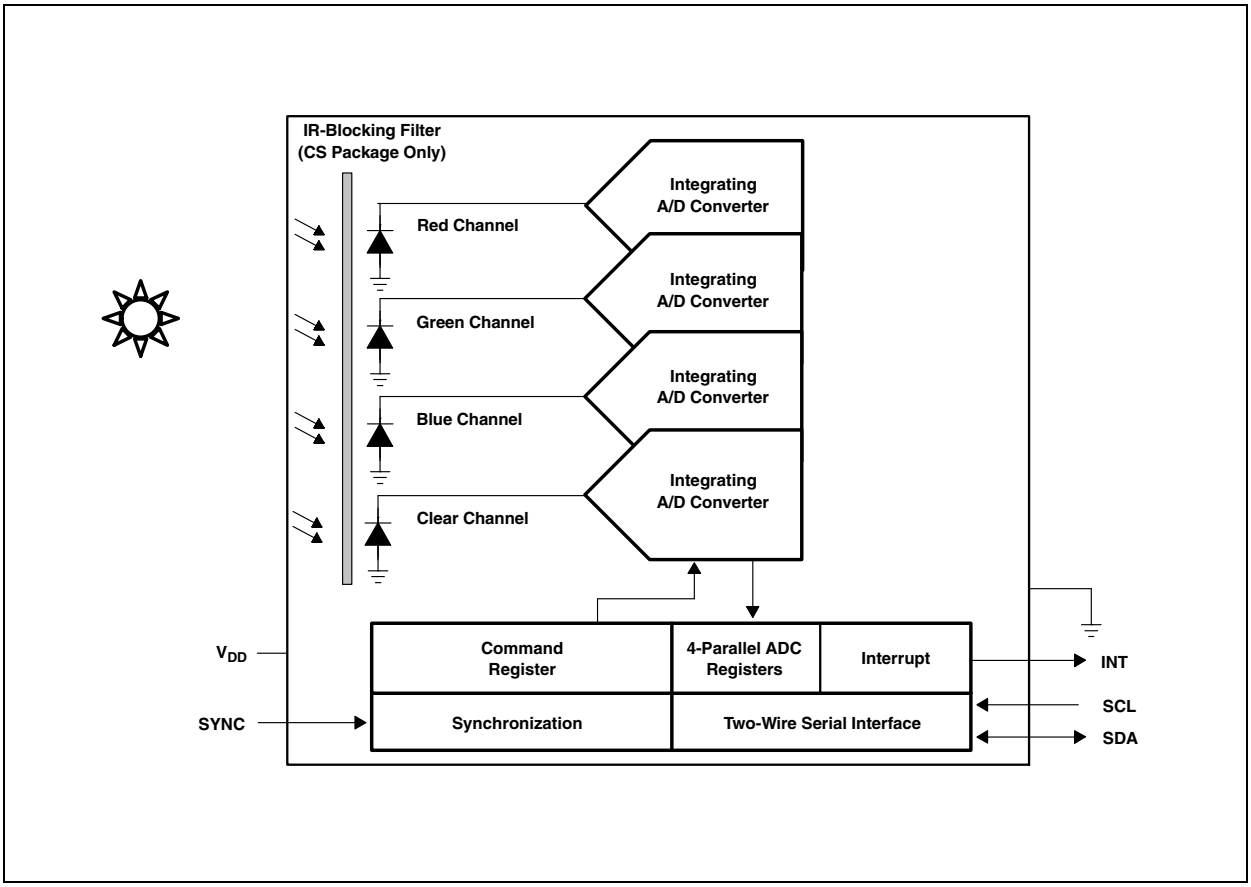
End Products and Market Segments

- HDTVs
- Tablets, laptops, monitors
- Medical instrumentation
- Consumer toys
- Industrial/commercial lighting
- Industrial process control

Block Diagram

The functional blocks of this device are shown below:

Figure 2:
TCS3404 and TCS3414 Block Diagram



Pin Assignments

The TCS3404 and TCS3414 pin assignments are described below:

Figure 3:
Pin Diagram of Package CS 6-Lead Chipscale (Top View)

Package drawings is not to scale

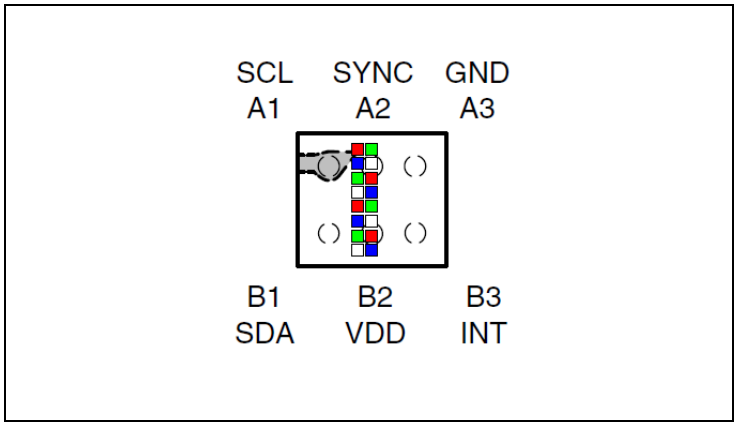


Figure 4:
Pin Diagram of Package FN Dual Flat No-Lead (Top View)

Package drawings is not to scale

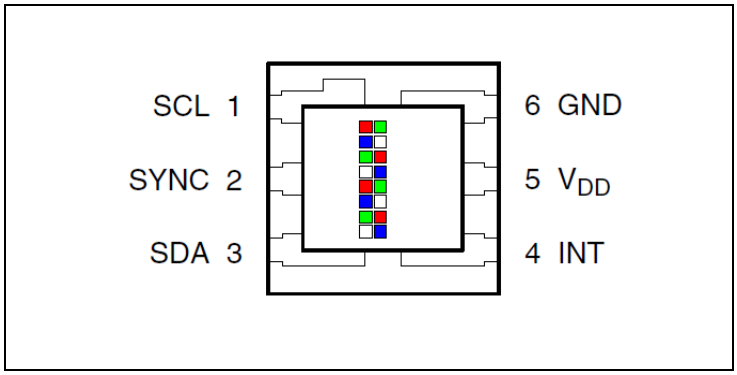


Figure 5:
Terminal Functions

Terminal			Type	Description
Name	CS Pkg No.	FN Pkg No.		
SCL	A1	1	I	Serial clock input terminal - clock signal for I^2C serial data
SYNC	A2	2	I	Synchronous input
SDA	B1	3	I/O	Serial data I/O terminal - serial data I/O for I^2C
INT	B3	4	O	Level interrupt - open drain
V_{DD}	B2	5		Supply voltage
GND	A3	6		Power supply ground. All voltages are referenced to GND

Absolute Maximum Ratings

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Figure 6:
Absolute Maximum Ratings over Operating Free-Air Temperature Range (unless otherwise noted)

Symbol	Parameter	Min	Max	Unit
V_{DD}	Supply voltage [1]		3.8	V
V_O	Digital output voltage range	-0.5	3.8	V
I_O	Digital output current	-1	20	mA
T_{strg}	Storage temperature range	-40	85	°C
ESD_{HBM}	ESD tolerance, human body model	±2000		V

Note(s):

1. All voltages are with respect to GND.

Electrical Characteristics

All limits are guaranteed. The parameters with min and max values are guaranteed with production tests or SQC (Statistical Quality Control) methods.

Figure 7:
Recommended Operating Conditions

Symbol	Parameter	Min	Nom	Max	Unit
V_{DD}	Supply voltage	2.7	3	3.6	V
T_A	Operating free-air temperature, (CS Package)	-40		85	°C
	Operating free-air temperature, (FN Package)	-30		70	°C
V_{IL}	SCL, SDA input low voltage	-0.5		0.8	V
V_{IH}	SCL, SDA input high voltage	2.1		3.6	V

Figure 8:
Electrical Characteristics, T_A = 25°C (unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
I_{DD}	Supply current @ V_{DD} = 3.6V	Power on (ADC inactive)		7.7	10	mA
		Power on (ADC active)		8.7	11	mA
		Power down		700	1000	µA
V_{OL}	INT, SDA output low voltage	3mA sink current	0		0.4	V
I_{LEAK}	Input leakage current (SDA, SCL, SYNC)	$V_{IH} = V_{DD}$, V_{IL} = GND	-5		5	µA

Figure 9:
AC Electrical Characteristics, V_{DD} = 3.3V, T_A = 25°C (unless otherwise noted)

Symbol	Parameter (1)	Test Conditions	Min	Typ	Max	Unit
$f_{(SCL)}$	Clock frequency 400kHz (I^2C)		0		400	kHz
	Clock frequency 100kHz (SMBus)		10		100	kHz
$t_{(BUF)}$	Bus free time between start and stop condition		1.3			µs
$t_{(HDSTA)}$	Hold time after (repeated) start condition. After this period, the first clock is generated.		0.6			µs
$t_{(SUSTA)}$	Repeated start condition setup time		0.6			µs

Symbol	Parameter (1)	Test Conditions	Min	Typ	Max	Unit
$t_{(SUSTO)}$	Stop condition setup time		0.6			µs
$t_{(HDDAT)}$	Data hold time		0		0.9	µs
$t_{(SUDAT)}$	Data setup time		100			ns
$t_{(LOW)}$	SCL clock low period		1.3			µs
$t_{(HIGH)}$	SCL clock high period		0.6			µs
$t_{(TIMEOUT)}$	Detect clock/data low timeout (SMBus only)		25		35	ms
t_F	Clock/data fall time				300	ns
t_R	Clock/data rise time				300	ns
C_i	Input pin capacitance				10	pF
$t_{LOW(SYNC)}$	SYNC low period (see Figure 10)			50		µs
$t_{HIGH(SYNC)}$	SYNC high period (see Figure 10)			50		µs
$t_{F(SYNC)}$	SYNC fall time (see Figure 10)			50		ns
$t_{R(SYNC)}$	SYNC rise time (see Figure 10)			50		ns

Note(s):

1. Specified by design and characterization; not production tested.

Figure 10:
Timing Diagram for Sync

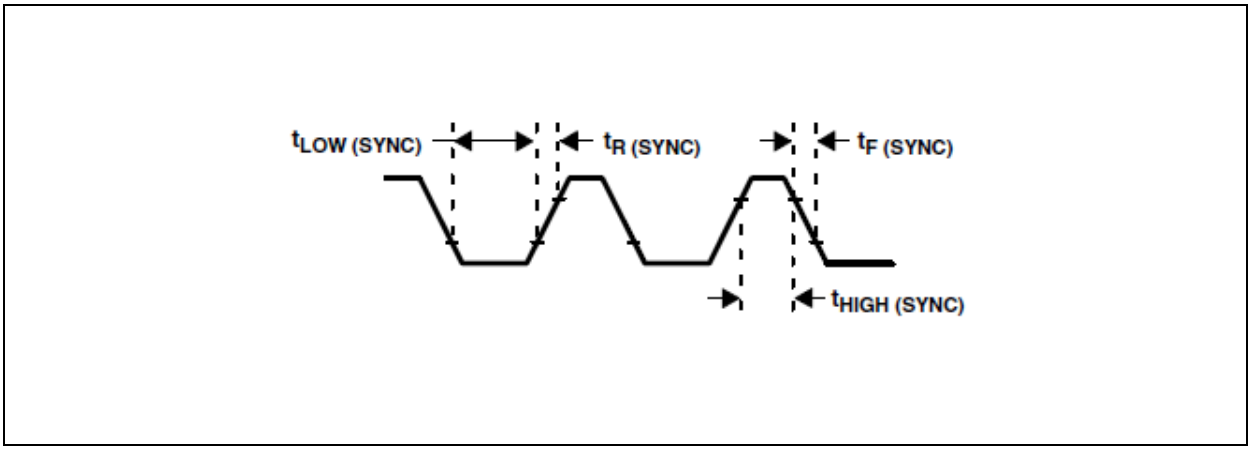


Figure 11:
Optical Characteristics, V_{DD} = 3V, T_A = 25°C, Gain = 64×, T_{int} = 12ms (unless otherwise noted) (1), (2)

Symbol	Parameter	Test Conditions	Red Channel			Green Channel			Blue Channel			Clear Channel			Unit
						Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
R_e	Irradiance responsivity (CS package)	λ_p = 470nm (3)	0%		15%	15%		50%	65%		90%	59.0	65.6	72.5	counts/ (µW/cm^2)
		λ_p = 524nm (4)	0%		15%	60%		90%	0%		35%	71.2	76.9	82.7	
		λ_p = 640nm (5)	80%		110%	0%		15%	0%		15%	80.6	90.1	99.5	
R_e	Irradiance responsivity (FN package)	λ_p = 470nm (3)	0%		15%	10%		50%	65%		90%	56.3	62.5	69.1	counts/ (µW/cm^2)
		λ_p = 524nm (4)	0%		15%	60%		90%	0%		35%	72.5	78.4	84.3	
		λ_p = 640nm (5)	80%		110%	0%		15%	0%		15%	94.2	105.3	116.3	

Note(s):

1. The percentage shown represents the ratio of the respective red, green, or blue channel value to the clear channel value.
2. Optical measurements are made using small-angle incident radiation from a light-emitting diode (LED) optical source.
3. The 470nm input irradiance is supplied by an InGaN light-emitting diode with the following characteristics: peak wavelength λ_p = 470nm, spectral halfwidth $\Delta\lambda$½ = 35nm, and luminous efficacy = 75lm/W.
4. The 524nm input irradiance is supplied by an InGaN light-emitting diode with the following characteristics: peak wavelength λ_p = 524nm, spectral halfwidth $\Delta\lambda$½ = 47nm, and luminous efficacy = 520lm/W.
5. The 640nm input irradiance is supplied by a AlInGaP light-emitting diode with the following characteristics: peak wavelength λ_p = 640nm, spectral halfwidth $\Delta\lambda$½ = 17nm, and luminous efficacy = 155lm/W.
6. Illuminance responsivity R_v is calculated from the irradiance responsivity R_e by using the LED luminous efficacy values stated in notes 3, 4, and 5 and using 1lx = 1lm/m^2.

Figure 12:
Optical Characteristics, V_{DD} = 3V, T_A = 25°C (unless otherwise noted) (2), (3), (4)

Parameter		Test Conditions	Min	Typ	Max	Unit
Gain scaling, relative to 1× gain setting	4×		3.8	4	4.2	
	16×		15.2	16	16.8	
	64×		60.8	64	67.2	
Dark ADC count value		E_e = 0, 64× gain setting, T_{int} = 400ms	0	3	15	counts
Maximum digital count value		Prescale = 1, T_{int} = 400ms (1)			65535	counts
f_{osc} Oscillator frequency			4.2	4.4	4.6	MHz
Internal integration time tolerance			-5		5	%
Temperature coefficient of responsivity (SYNC mode)		λ ≤ 700nm, -40°C ≤ T_A ≤ 85°C		±200		ppm/°C

Note(s):

1. At shorter integration times and/or higher Prescale settings, the device will reach saturation of the analog section before the digital count reaches the maximum 16-bit value. The worst-case (lowest) analog saturation value can be obtained using the formula: Analog saturation = (f_{osc}(min) ×T_{int}) ÷ Prescale, where $F_{osc(min)}$ is the minimum oscillator frequency in Hz, and tint is the actual integration time (internal, manually-timed, or sync-generated) in seconds.
2. Gain is controlled by the gain register (07h) described in the Register section.
3. Measurements taken when the Photodiode field value in the Photodiode Register (06h) is 00b and when the Prescaler field value in the Gain Register (07h) is 000b.
4. The full scale ADC count value is slew-rate limited for short integration times and is limited by the 16-bit counter for long integration times. The nominal transition between the two regions is t_{int} = 65535/5000 = 13.1ms.

Parameter Measurement Information

Figure 13:
Timing Diagrams

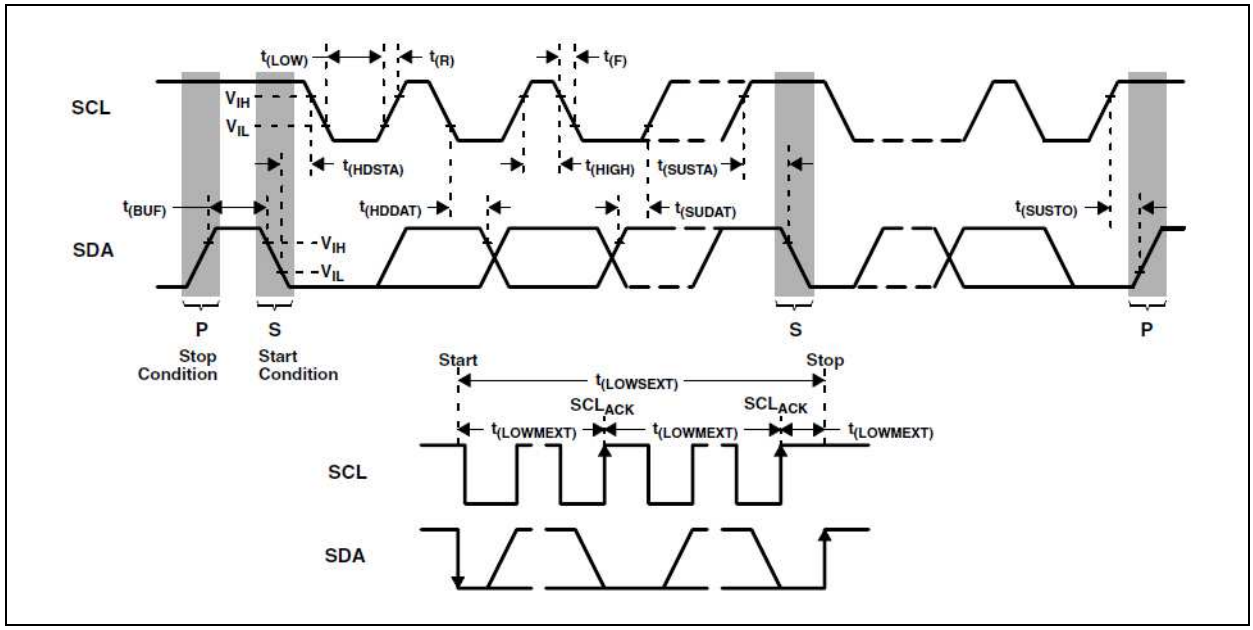


Figure 14:
Example Timing Diagram for Send Byte Format

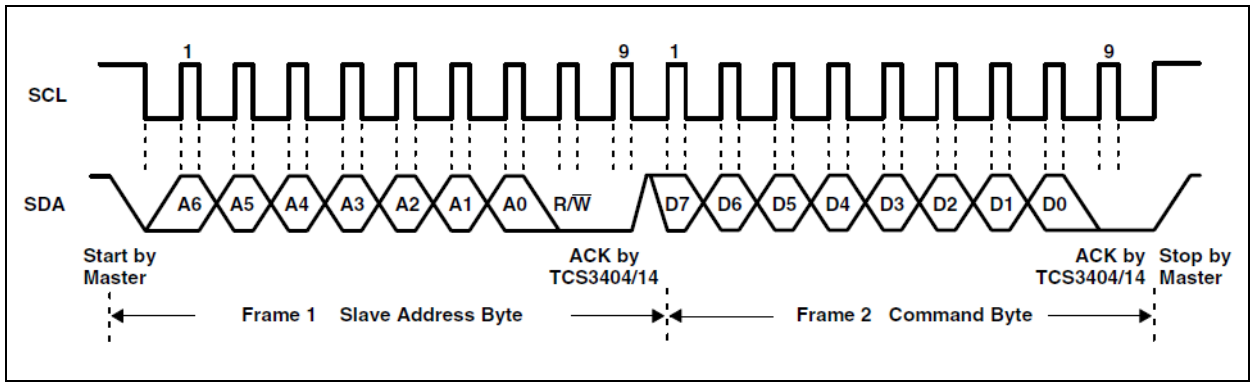
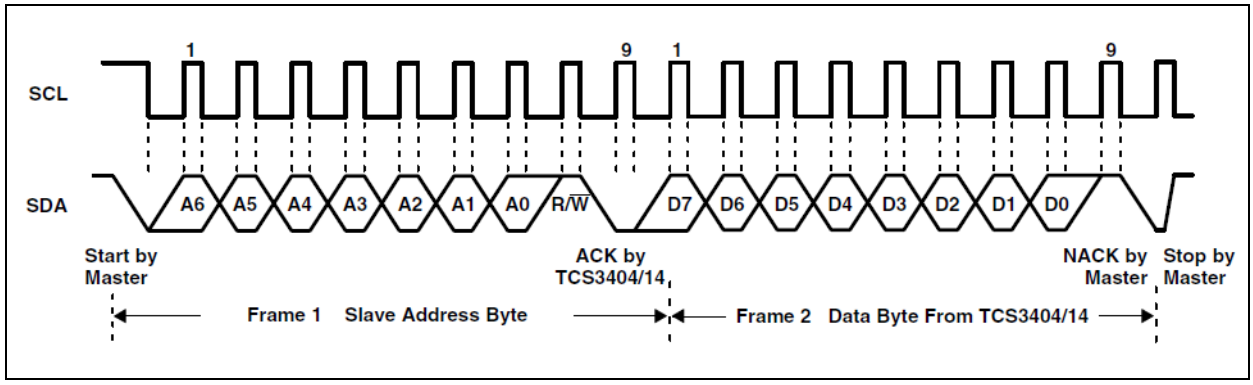


Figure 15:
Example Timing Diagram for Receive Byte Format



Typical Operating Characteristics

Figure 16:
Spectral Responsivity CS Package

Spectral responsivity is normalized at 655nm.

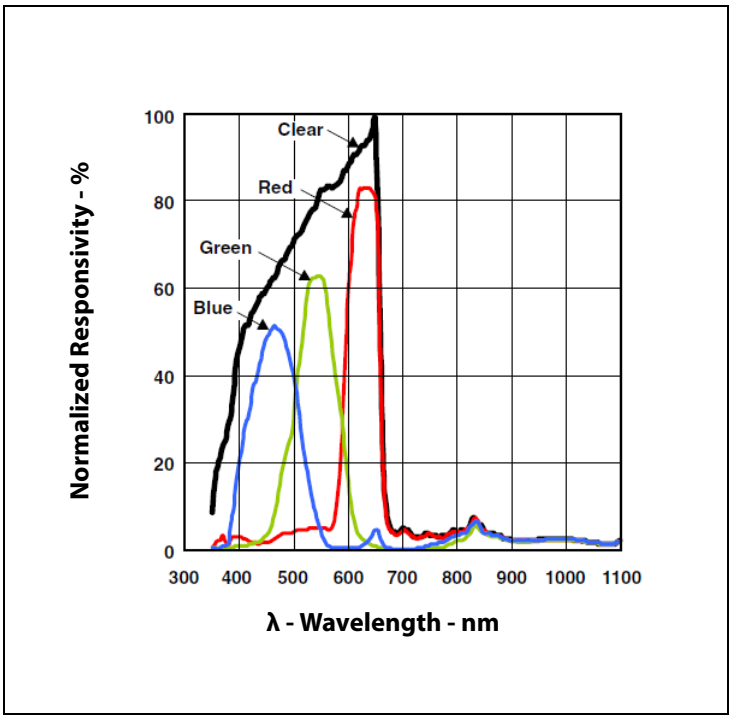


Figure 17:
Spectral Responsivity FN Package

Spectral responsivity is normalized at 850nm.

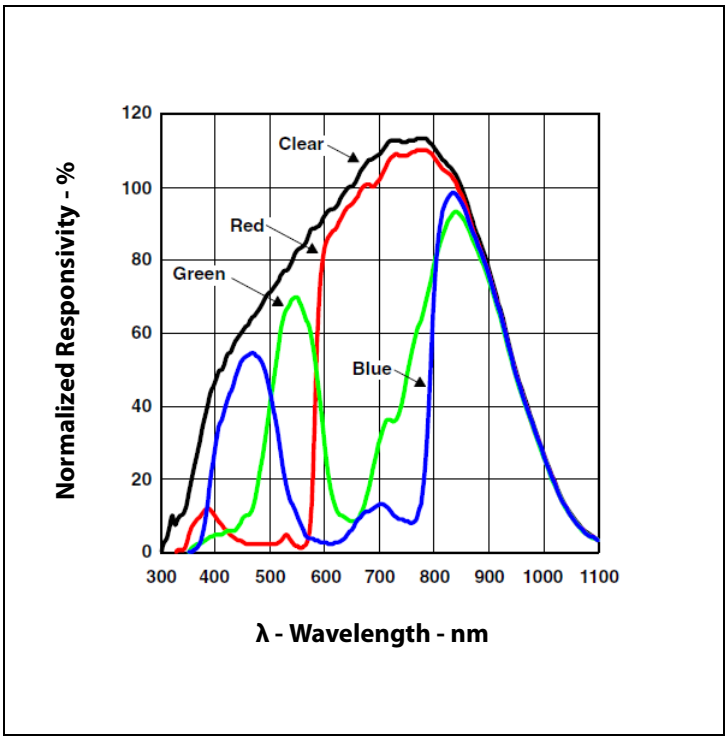


Figure 18:
I_{DD} OFF vs. Free-Air Temperature (Power Down)

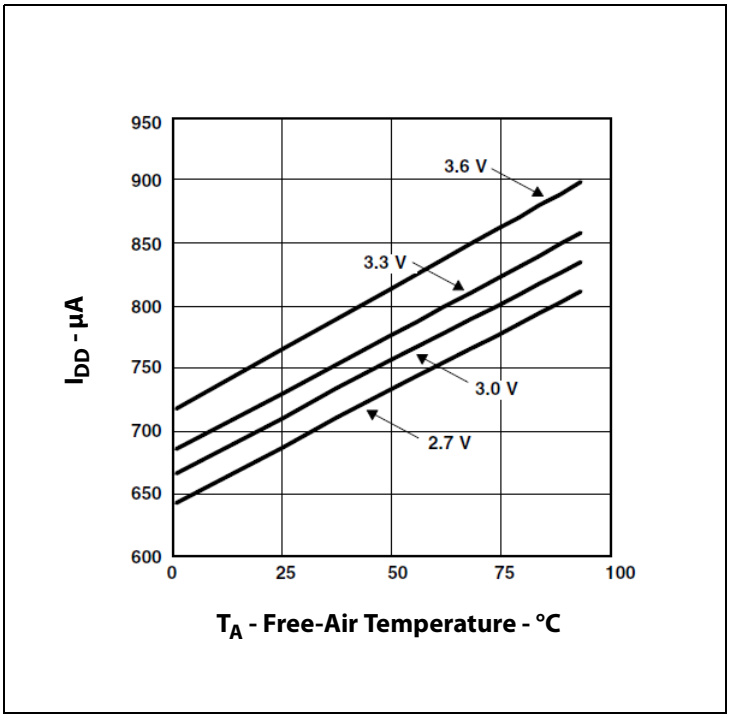


Figure 19:
I_{DD} ON vs. Free-Air Temperature (Power On - ADC Inactive)

When the device is powered on and the ADC is active, I_{DD} is approximately 1mA higher.

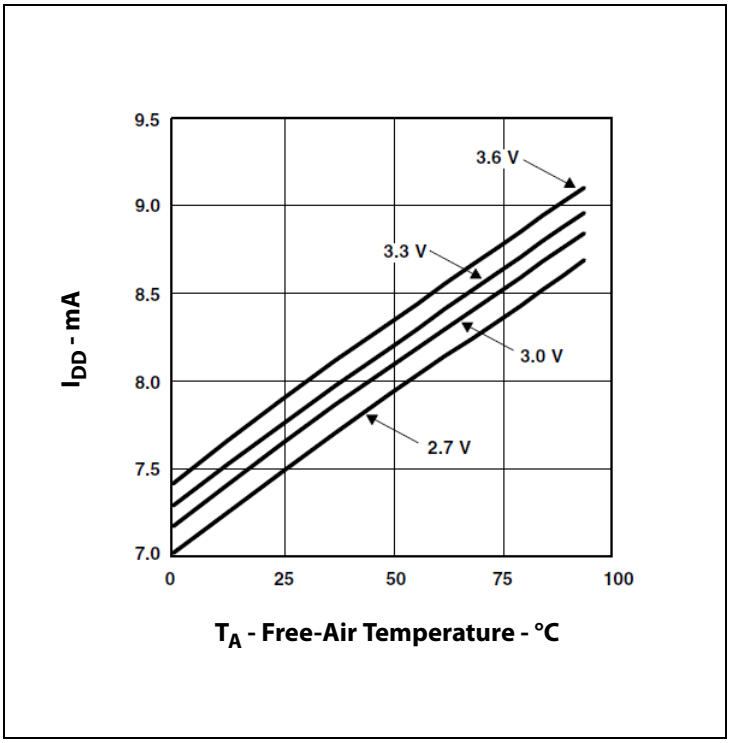


Figure 20:
Normalized Integration Time vs. Free-Air Temperature

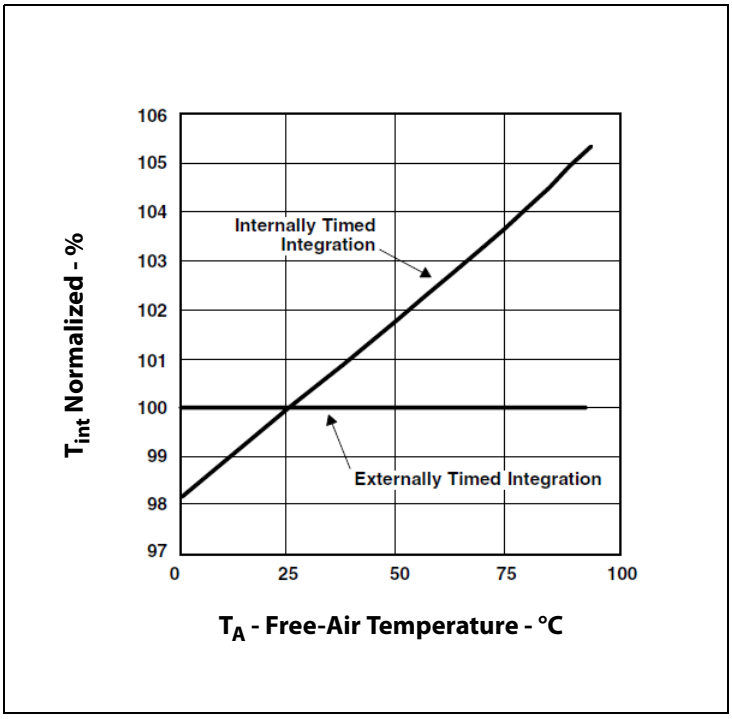


Figure 21:
Normalized Responsivity vs.
Angular Displacement - FN Package

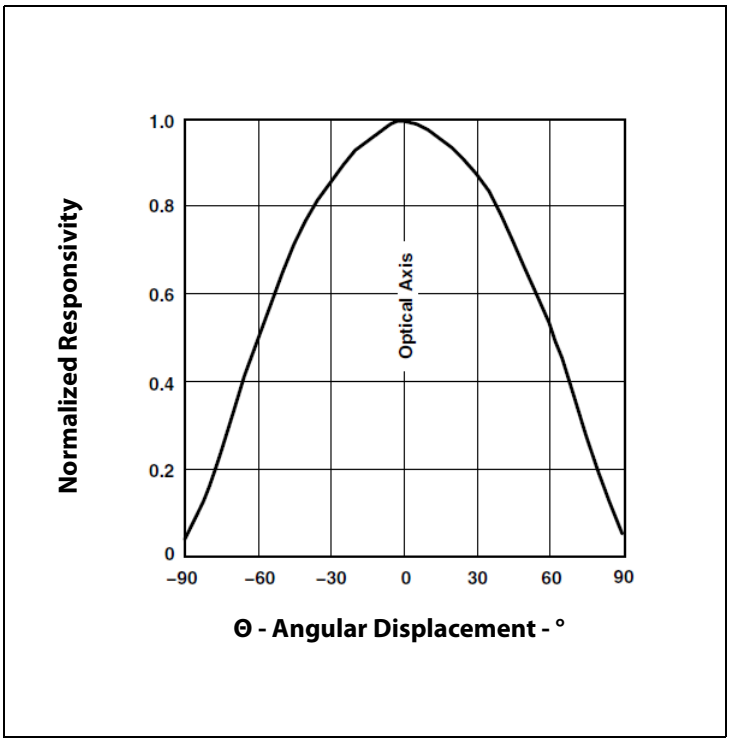


Figure 22:
Normalized Responsivity vs. Angular Displacement - CS Package

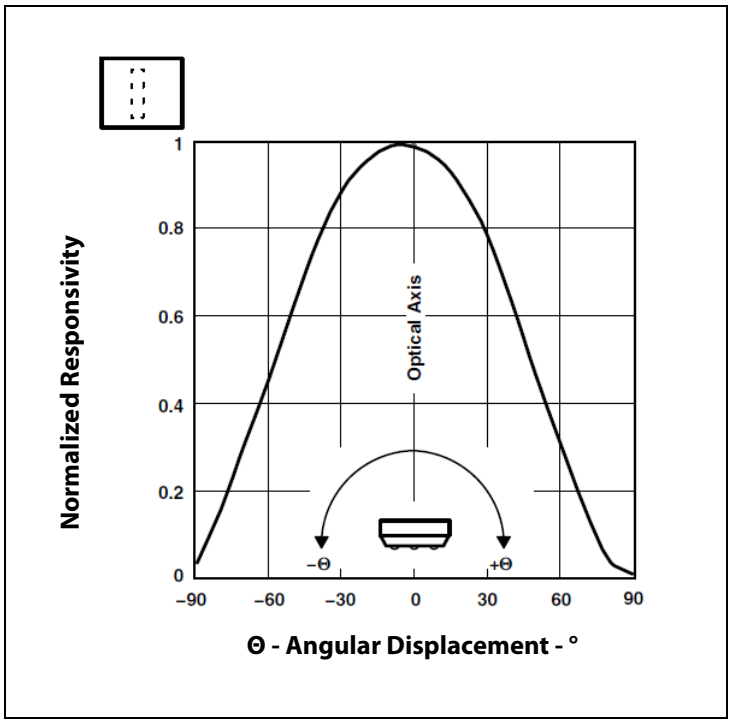
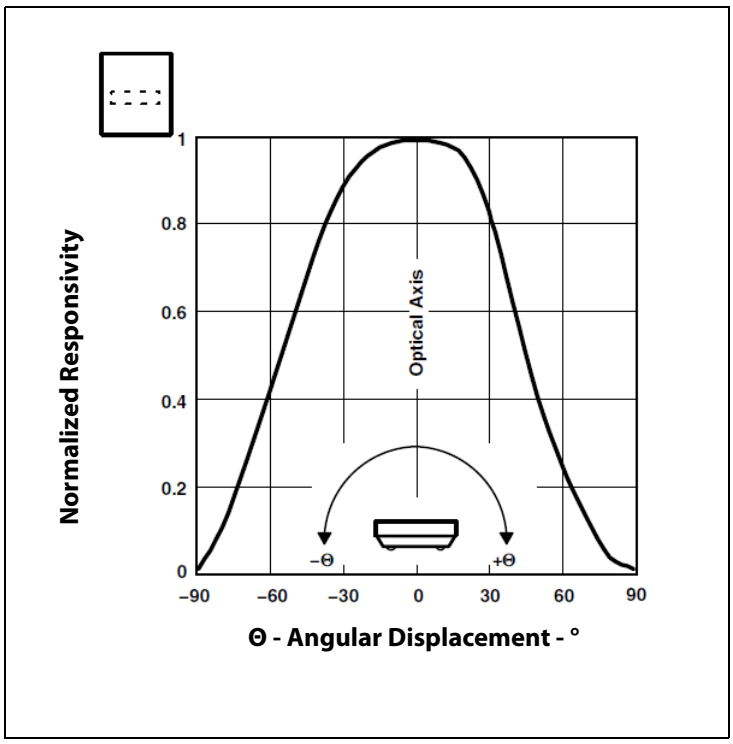


Figure 23:
Normalized Responsivity vs. Angular Displacement - CS Package



Principles of Operation

Analog-to-Digital Converter

The TCS3404/14 contains four integrating analog-to-digital converters (ADC) that integrate the currents from the four photodiodes (channel 1 through channel 4). Integration of all four channels occurs simultaneously, and upon completion of the conversion cycle the conversion results are transferred to the channel data registers, respectively. The transfers are double-buffered to ensure that invalid data is not read during the transfer. After the transfer, the device automatically begins the next integration cycle.

There are two ways to control the integration cycles: internally timed and externally timed. Internally-timed integration cycles can either be continuous back-to-back conversions or can be externally triggered as a single event using the SYNC pin. Externally-timed integrations can be controlled by setting and clearing a register bit (i.e. ADC_EN in Control Register) using the serial interface, or by 1 or more pulses input to the SYNC pin. Integration options are configured through the Timing Register (see Timing Register (01h) for more information).

Digital Interface

Interface and control of the TCS3404/14 is accomplished through a two-wire serial interface to a set of registers that provide access to device control functions and output data. The serial interface is compatible with System Management Bus (SMBus) versions 1.1 and 2.0, and I^2C bus Fast-Mode.

The TCS3404/14 device supports a single slave address outlined in Figure 24. Additional devices shown in the Ordering Information support additional I^2C slave addresses for systems requiring more than one device.

Figure 24:
Slave Address

Slave Address	SMB Alert Address
0111001	0001100

Note(s):

1. The slave and SMB Alert addresses are 7 bits. Please note the SMBus and I^2C protocols on the following pages. A read/write bit should be appended to the slave address by the master device to communicate properly with the device.

Interrupt

Although the ADC channel data registers can be read at any time to obtain the most recent conversion value, in some applications, periodic polling of the device may not be desirable. For these types of applications, the device supports a variety of interrupt options allowing the user to configure the device to signal when a change in light intensity has occurred. High and low threshold registers allow a range of light levels to be defined, outside of which the device generates an interrupt. A persistence setting allows the user to specify a time duration that the measured value must remain outside of the defined range before generating an interrupt. The interrupt function can be assigned to any one of the four ADC color channels. See Interrupt Control Register (02h) for more information on configuring the interrupt functions.

SMBus and I²C Protocols

Each *Send* and *Write* protocol is, essentially, a series of bytes. A byte sent to the TCS3404/14 with the most significant bit (MSB) equal to 1 will be interpreted as a COMMAND byte. The lower four bits of the COMMAND byte form the register select address (see Figure 24), which is used to select the destination for the subsequent byte(s) received. The TCS3404/14 responds to any Receive Byte requests with the contents of the register specified by the stored register select address.

The TCS3404/14 implements the following protocols of the SMB 2.0 specification:

- Send Byte Protocol
- Receive Byte Protocol
- Write Byte Protocol
- Write Word Protocol
- Read Word Protocol
- Block Write Protocol
- Block Read Protocol

The TCS3404/14 implements the following protocols of the I2C specification:

- I²C Write Protocol
- I²C Read (Combined Format) Protocol

When an SMBus Block Write or Block Read is initiated (see description of Command Register), the byte following the COMMAND byte is ignored but is a requirement of the SMBus specification. This field contains the byte count (i.e. the number of bytes to be transferred). The TCS3404 (SMBus) device ignores this field and extracts this information by counting the actual number of bytes transferred before the Stop condition is detected.

When an I²C Write or I²C Read (Combined Format) is initiated, the byte count is also ignored but follows the SMBus protocol specification. Data bytes continue to be transferred from the TCS3414 (I²C) device to Master until a NACK is sent by the Master.

The data formats supported by the TCS3404 and TCS3414 devices are:

- Master transmitter transmits to slave receiver (SMBus and I²C):
  - The transfer direction in this case is not changed.
- Master reads slave immediately after the first byte (SMBus only):
  - At the moment of the first acknowledgment (provided by the slave receiver) the master transmitter becomes a master receiver and the slave receiver becomes a slave transmitter.
- Combined format (SMBus and I²C):
  - During a change of direction within a transfer, the master repeats both a START condition and the slave address but with the R/W bit reversed. In this case, the master receiver terminates the transfer by generating a NACK on the last byte of the transfer and a STOP condition.

For a complete description of SMBus protocols, please review the SMBus Specification at www.smbus.org/specs. For a complete description of the I²C protocol, please review the NXP I²C design specification at www.i2c-bus.org/references.

Figure 25:
SMBus and I²C Packet Protocol Element Key

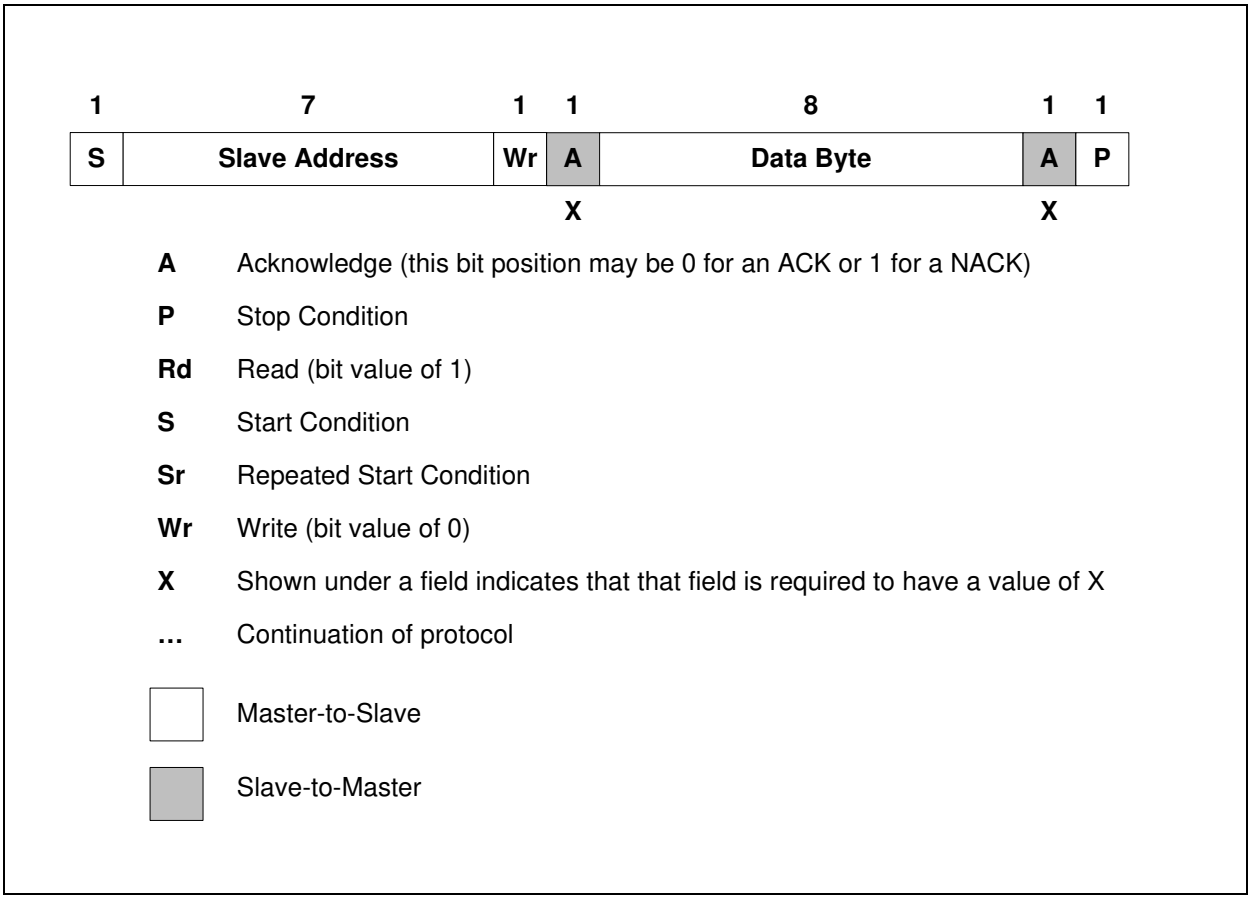


Figure 26:
SMBus Send Byte Protocol

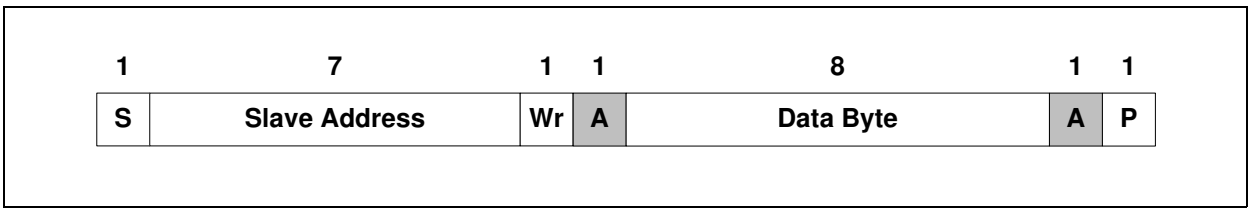


Figure 27:
SMBus Receive Byte Protocol

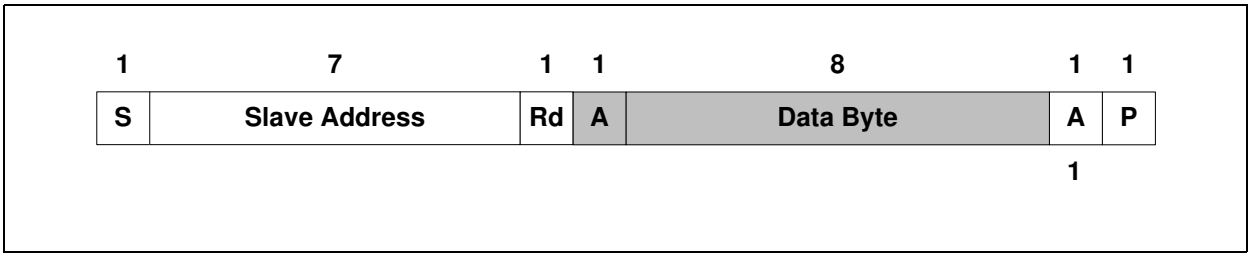


Figure 28:
SMBus Write Byte Protocol

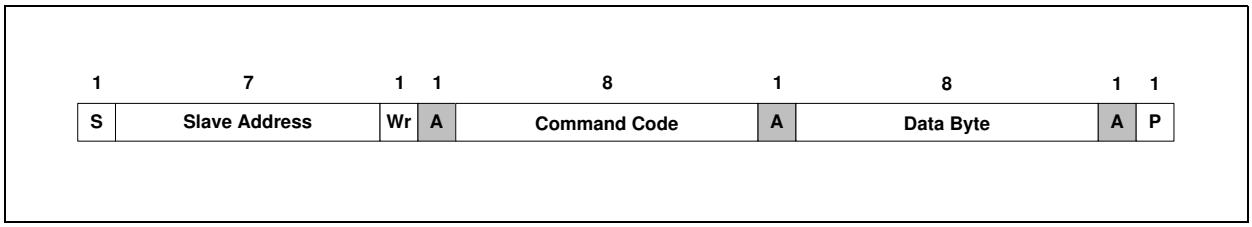


Figure 29:
SMBus Read Byte Protocol

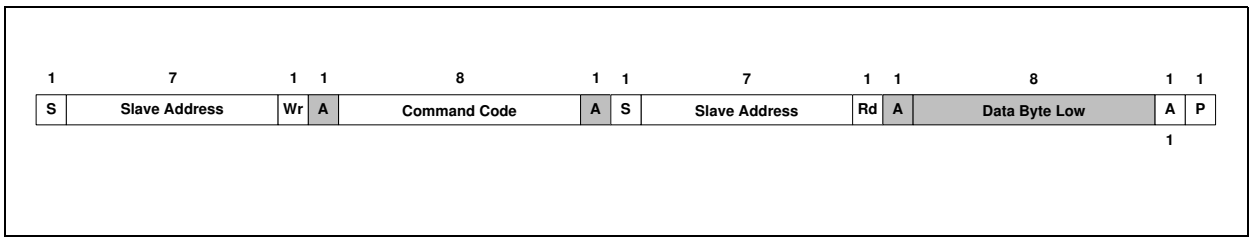


Figure 30:
SMBus Write Word Protocol

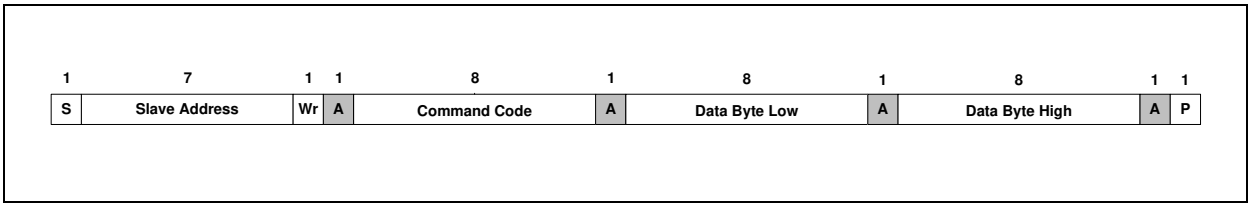


Figure 31:
SMBus Read Word Protocol

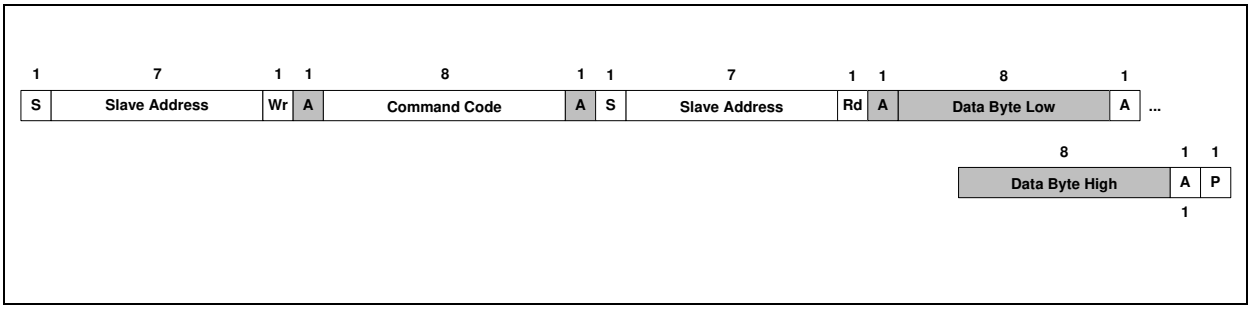
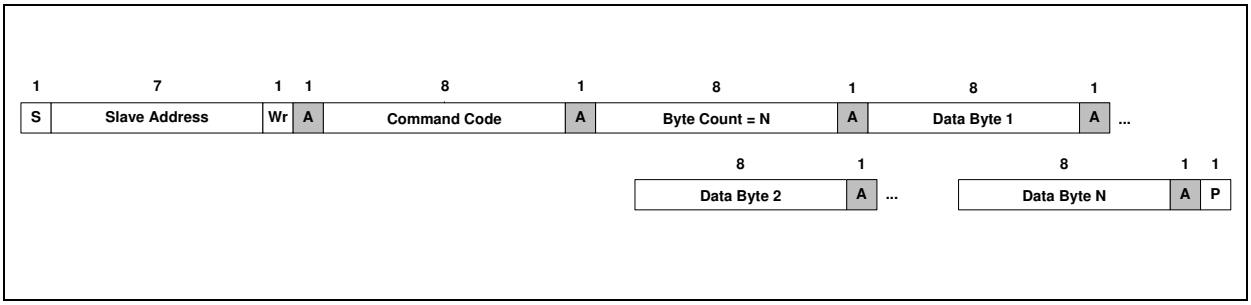


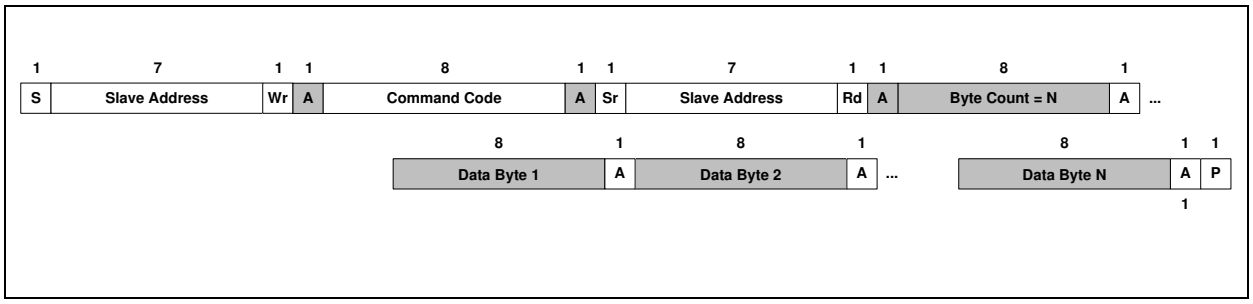
Figure 32:
SMBus Block Write or I²C Write Protocols



Note(s):

1. The I²C read protocol does not use the Byte Count packet, and the Master will continue receiving Data Bytes until the Master initiates a Stop Condition. See the Command Register for additional information regarding the Block Read/Write protocol.

Figure 33:
SMBus Block Read or I²C Read (Combined Format) Protocols



Note(s):

1. The I²C read protocol does not use the Byte Count packet, and the Master will continue receiving Data Bytes until the Master initiates a Stop Condition. See the Command Register for additional information regarding the Block Read/Write protocol.

Register Set

The TCS3404/14 is controlled and monitored by 18 user registers and a command register accessed through the serial interface. These registers provide for a variety of control functions and can be read to determine results of the ADC conversions. The Register Set is summarized in Figure 34.

Figure 34:
Register Address

Address	Register Name	Register Function
----	COMMAND	Specifies register address
00h	CONTROL	Control of basic functions
01h	TIMING	Integration time/gain control
02h	INTERRUPT	Interrupt control
03h	INT SOURCE	Interrupt source
04h	ID	Part number/Rev ID
07h	GAIN	ADC gain control
08h	LOW_THRESH_LOW_BYTE	Low byte of low interrupt threshold
09h	LOW_THRESH_HIGH_BYTE	High byte of low interrupt threshold
0Ah	HIGH_THRESH_LOW_BYTE	Low byte of high interrupt threshold
0Bh	HIGH_THRESH_HIGH_BYTE	High byte of high interrupt threshold
0Fh	----	SMBus block read (10h through 17h)
10h	DATA1LOW	Low byte of ADC green channel
11h	DATA1HIGH	High byte of ADC green channel
12h	DATA2LOW	Low byte of ADC red channel
13h	DATA2HIGH	High byte of ADC red channel
14h	DATA3LOW	Low byte of ADC blue channel
15h	DATA3HIGH	High byte of ADC blue channel
16h	DATA4LOW	Low byte of ADC clear channel
17h	DATA4HIGH	High byte of ADC clear channel

The mechanics of accessing a specific register depends on the specific SMB protocol used. Refer to the section on SMBus protocols on the previous pages. In general, the Command Register is written first to specify the specific control/status register for following read/write operations.

Command Register

The Command Register specifies the address of the target register for subsequent read and write operations. This register contains eight bits as described in Figure 35 and defaults to 00h at power on.

Figure 35:
Command Register

7	6	5	4	3	2	1	0
CMD	**TRANSACTION**		**ADDRESS**				

Field	Bits	Description		
CMD	7	Select Command Register. Must write as 1.		
TRANSACTION	6:5	Transaction. Selects type of transaction to follow in subsequent data transfer.		
		Field Value	**Transaction**	**Description**
		00	Byte protocol	SMB read/write byte protocol
		01	Word protocol	SMB read/write word protocol
		10	Block protocol	SMB read/write block protocol
		11	Interrupt clear	Clear any pending interrupt and is a write-once-to-clear field
ADDRESS	4:0	Register Address. This field selects the specific control or status register for following write and read commands according to Figure 34.		

Note(s):

1. An I^2C block transaction will continue until the Master sends a stop condition. See Figure 30 and Figure 31. Unlike the I^2C protocol, the TCS3404/14 SMBus read/write protocol requires a Byte Count. All eight ADC Channel Data Registers (10h through 17h) can be read simultaneously in a single SMBus transaction. This is the only 64-bit data block supported by the TCS3404 SMBus protocol. The TRANSACTION field must be set to 10, and a read condition should be initiated with a COMMAND CODE of CFh. By using a COMMAND CODE of CFh during an SMBus Block Read Protocol, the TCS3404 device will automatically insert the appropriate Byte Count (Byte Count = 8) as illustrated in Figure 30. A write condition should not be used in conjunction with the 0Fh register.
2. Only the Send Byte Protocol should be used when clearing interrupts.

Control Register (00h)

The Control Register contains two bits and is primarily used to power the TCS3404/14 device up and down as shown in Figure 36.

Figure 36:
Control Register

7	6	5	4	3	2	1	0
Resv	**Resv**	**Resv**	**ADC_VALID**	**Resv**	**Resv**	**ADC_EN**	**POWER**

Field	Bits	Description
Resv	7:5	Reserved. Write as 0.
ADC_VALID	4	ADC valid. This read-only field indicates that the ADC channel has completed an integration cycle.
Resv	3:2	Reserved. Write as 0.
ADC_EN	1	ADC enable. This field enables the four ADC channels to begin integration. Writing a 1 activates the ADC channels, and writing a 0 disables the ADCs.
POWER	0	Power On. Writing a 1 powers on the device, and writing a 0 turns it OFF.

Note(s):

1. Both ADC_EN and POWER must be asserted before the ADC channels will operate correctly.
2. INTEG_MODE and TIME/COUNTER fields in the Timing Register (01h) should be written before ADC_EN is asserted.
3. If a value of 03h is written, the value returned during a read cycle will be 03h. This feature can be used to verify that the device is communicating properly.
4. During writes and reads, the POWER bit is overridden and the oscillator is enabled, independent of the state of POWER.

Timing Register (01h)

The Timing Register controls the synchronization and integration time of the ADC channels. The Timing Register settings apply to all four ADC channels. The Timing Register defaults to 00h at power On.

Figure 37:
Timing Register

7	6	5	4	3	2	1	0
Resv	**SYNC_EDGE**	**INTEG_MODE**		**PARAM**			

Field	Bits	Description	
Resv	7	Reserved. Write as 0.	
SYNC_EDGE	6	Sync pin edge. If SYNC_EDGE is low, the falling edge of the sync pin is used to stop an integration cycle when INTEG_MODE is 11. If SYNC_EDGE is high, the rising edge of the sync pin is used to stop an integration cycle when INTEG_MODE is 11.	
INTEG_MODE	5:4	Selects preset integration time, manual integration (via serial bus), or external synchronization (SYNC IN) modes.	
		Field Value	**Mode**
		00	In this mode, the integrator is free-running and one of the three internally-generated Nominal Integration Times is selected for each conversion (see Integration Time table below).
		01	Manually start/stop integration through serial bus using ADC_EN field in Control Register.
		10	Synchronize exactly one internally-timed integration cycle as specified in the NOMINAL INTEGRATION TIME beginning 2.4µs after being initiated by the SYNC IN pin.
		11	Integrate over specified number of pulses on SYNC IN pin (See SYNC IN PULSE COUNT table below). Minimum width of sync pulse is 50µs. SYNC IN must be low at least 3.6µs.

<table>
<tr><th>Field</th><th>Bits</th><th>Description</th></tr>
<tr><td rowspan="14">PARAM</td><td rowspan="14">3:0</td><td colspan="2">Uses single, multipurpose bitmapped field to select one of three predefined integration times or set the number of SYNC IN pulses to count when the INTEG_MODE accumulate mode (11) is selected.(1)</td></tr>
<tr><td>Field Value</td><td>Normal Integration Time</td></tr>
<tr><td>0000</td><td>12ms</td></tr>
<tr><td>0001</td><td>100ms</td></tr>
<tr><td>0010</td><td>400ms</td></tr>
<tr><td colspan="2"></td></tr>
<tr><td>Field Value</td><td>Sync in Pulse Count</td></tr>
<tr><td>0000</td><td>1</td></tr>
<tr><td>0001</td><td>2</td></tr>
<tr><td>0010</td><td>4</td></tr>
<tr><td>0011</td><td>8</td></tr>
<tr><td>0100</td><td>16</td></tr>
<tr><td>0101</td><td>32</td></tr>
<tr><td>0110</td><td>64</td></tr>
<tr><td>0111</td><td>128</td></tr>
<tr><td>1000</td><td>256</td></tr>
</table>

Note(s):

1. INTEG_MODE and TIME/COUNTER fields should be written before ADC_EN is asserted.