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TCS3430

Color and ALS Sensor

General Description

The device features advanced digital Ambient Light Sensing (ALS) and CIE 1931 Tristimulus Color Sensing (XYZ). Each of the channels has a filter to control its optical response, which allows the device to accurately measure ambient light and sense color. These measurements are used to calculate chromaticity, illuminance and color temperature, all of which are used to support various potential applications.

Ordering Information and Content Guide appear at end of datasheet.

Key Benefits & Features

The benefits and features of the TCS3430 Color and ALS Sensor are listed below:

Figure 1:
Added Value of Using TCS3430

Benefits	Features
• Improves ALS responsiveness of the system	• Capable of ±10% illuminance and correlated color temperature accuracy
• Reduces board space requirements and enables low-profile system design	• Small footprint and low profile package: 2.41mm x 1.75mm x 1.00mm
• Improves ALS response for more accurate measurement of lighting environment	• Advanced interference filter technology
• Enables accurate color and ALS sensing under varying lighting conditions and behind dark glass	• Wide dynamic range and high sensitivity
• Enables accurate color temperature calculations and ambient light sensing	• XYZ tristimulus filters • Programmable gain and integration time
• Low power consumption	• 1.8V supply voltage and I^2C bus

Applications

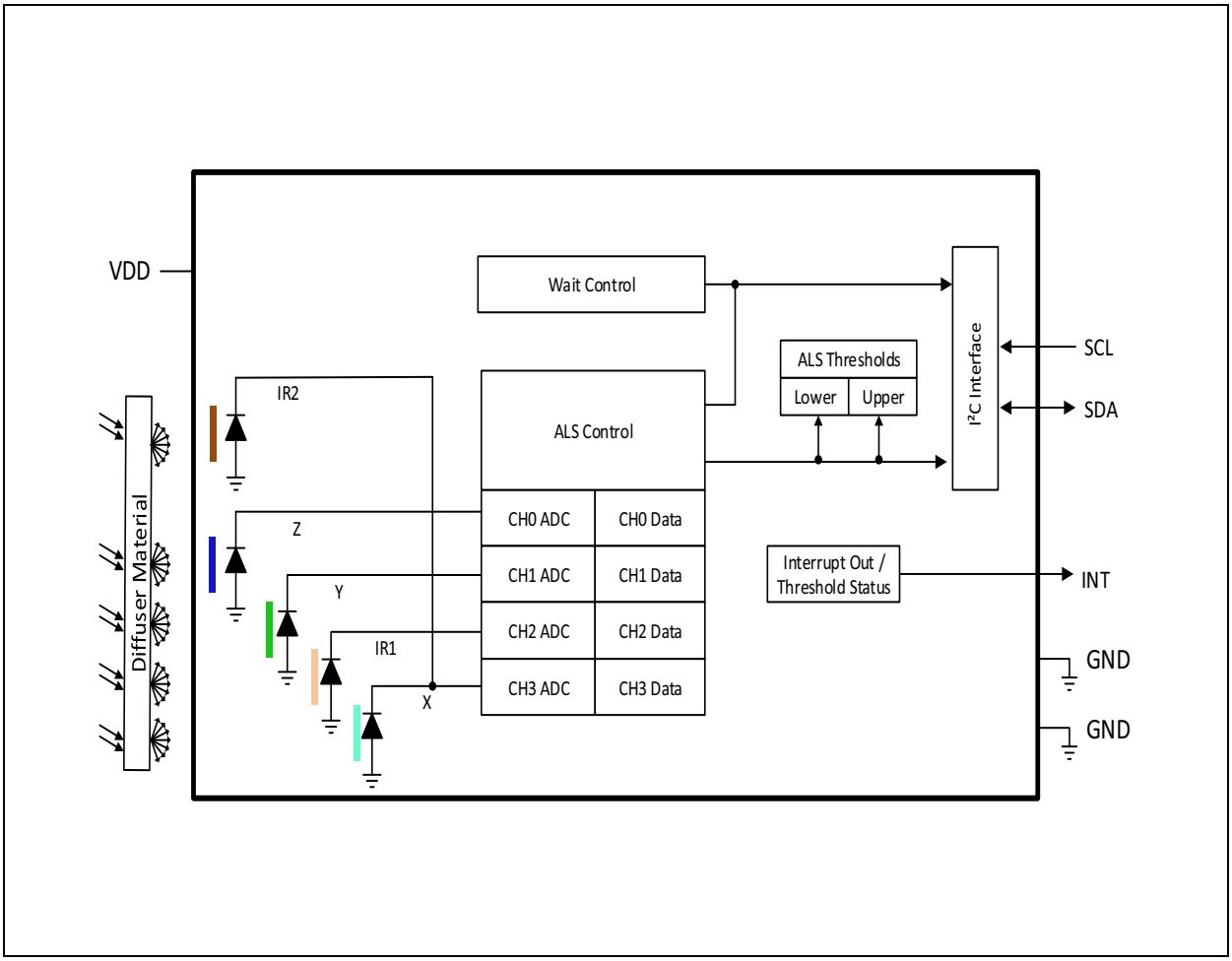
The TCS3430 applications include:

- Display management
- Camera image correction and enhancement
- Color sensing
- Ambient light sensing
- Optical identification
- Color matching

Block Diagram

The functional blocks of this device are shown below:

Figure 2:
TCS3430 Block Diagram



Pin Assignment

Figure 3:
TCS3430 Pinout (Top View)

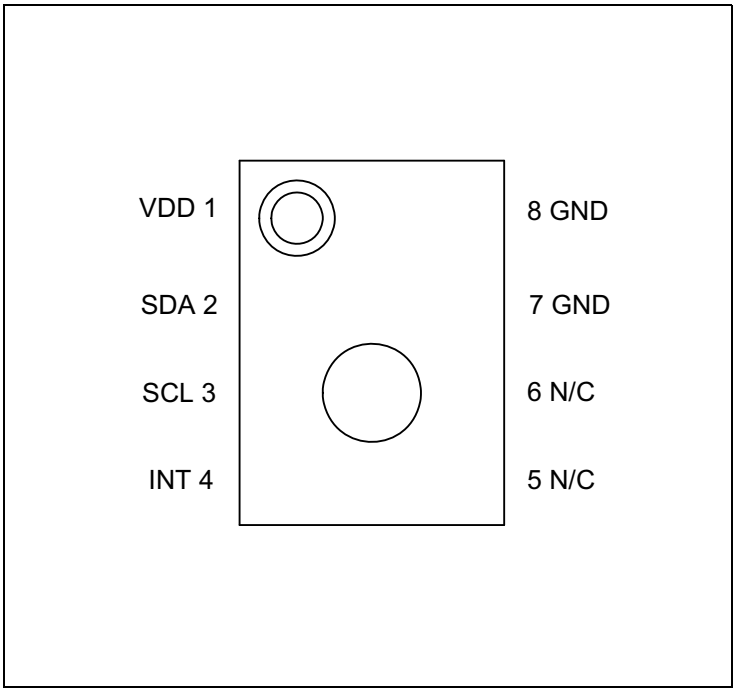


Figure 4:
Pin Description

Pin Number	Pin Name	Description
1	VDD	Supply voltage
2	SDA	I^2C serial data I/O terminal
3	SCL	I^2C serial clock input terminal
4	INT	Interrupt. Open drain output (active low)
5	N/C	No connection. May be connected to Ground or not connected.
6	N/C	No connection. May be connected to Ground or not connected.
7	GND	Ground. All voltages are referenced to GND
8	GND	Ground. All voltages are referenced to GND

Absolute Maximum Ratings

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Figure 5:
Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Units
V_{DD}	Supply voltage	-0.3	2.2	V
V_{IO}	Digital I/O terminal voltage	-0.3	3.6	V
I_{IO}	Output terminal current	-1	20	mA
T_{STRG}	Storage temperature range	-40	85	°C
T_J	Junction temperature range	-40	90	°C
ESD_{HBM}	Electrostatic discharge HBM (JS-001-2014)	±2000		V
ESD_{CDM}	Electrostatic discharge CDM JEDEC JESD22-C101F Oct 2013	±500		V
I_{SCR}	Input current (latch up immunity) JEDEC JESD78D Nov 2011	CLASS 2		

Electrical Characteristics

Figure 6:
Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Units
V_{DD}	Supply voltage	1.7	1.8	2.0	V
T_A	Operating free-air temperature (1)	-30		85	℃

Note(s):

1. While the device is operational across the temperature range, performance will vary with temperature. Operational characteristics are at 25°C, unless otherwise noted.

Figure 7:
Operating Characteristics, V_{DD} = 1.8 V, T_A = 25°C (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
f_{OSC}	Oscillator frequency			8.1		MHz
I_{DD}	Supply current (1)	Active ALS state (PON=AEN=1) (2)		100	150	µA
		Idle state (PON=1, AEN=0) (3)		30	60	
		Sleep State (4)		0.7	5.0	µA
V_{OL}	INT, SDA output low voltage	6 mA sink current			0.6	V
I_{LEAK}	Leakage current, SDA, SCL, INT, pins		-5		5	µA
V_{IH}	SCL, SDA input high voltage		1.26			V
V_{IL}	SCL, SDA input low voltage				0.54	V

Note(s):

1. Values are shown at the VDD pin.
2. This parameter indicates the supply current during periods of ALS integration. If Wait is enabled (WEN=1), the supply current is lower during the Wait period.
3. Idle state occurs when PON=1 and all functions are not enabled.
4. Sleep state occurs when PON = 0 and I^2C bus is idle. If Sleep state has been entered as the result of operational flow, SAI = 1, PON will remain high.

Figure 8:
Optical Characteristics

Parameter	Channel	Light Source	Min	Typ	Max	Units
Irradiance Responsivity 16x gain, 400ms (1)	X	Warm White LED (2700K, 25 µW/cm^2)	58	74	90	counts/ (µW/cm^2)
	Y		56	62	70	
	Z		6.5	10.3	14	
	IR1	Far Red LED (λ = 730nm, 11.6 µW/cm^2)	90	135	180	
	IR2	IR LED (λ = 950nm, 41.8 µW/cm^2)	90	160	230	

Note(s):

1. Tested using collimated light sources.

Figure 9:
Filter Characteristics

Symbol	Parameter	Min	Typ	Max	Units
λ_X1	Peak 1 wavelength of channel X	427	437	447	nm
λ_X2	Peak 2 wavelength of channel X	564	574	584	nm
λ_Y	Peak wavelength of channel Y	527	537	547	nm
λ_Z	Peak wavelength of channel Z	424	434	444	nm
FWHM_X1	Full width at half maximum of channel X peak 1	45	55	65	nm
FWHM_X2	Full width at half maximum of channel X peak 2	83	93	103	nm
FWHM_Y	Full width at half maximum of channel Y	92	102	112	nm
FWHM_Z	Full width at half maximum of channel Z	53	63	73	nm
T50L_IR1	Lower edge of IR1 at 50% of transition	672	687	702	nm
T50H_IR1	Higher edge of IR1 at 50% of transition	815	830	845	nm
T50_IR2	At 50% of transition of IR2	812	827	842	nm

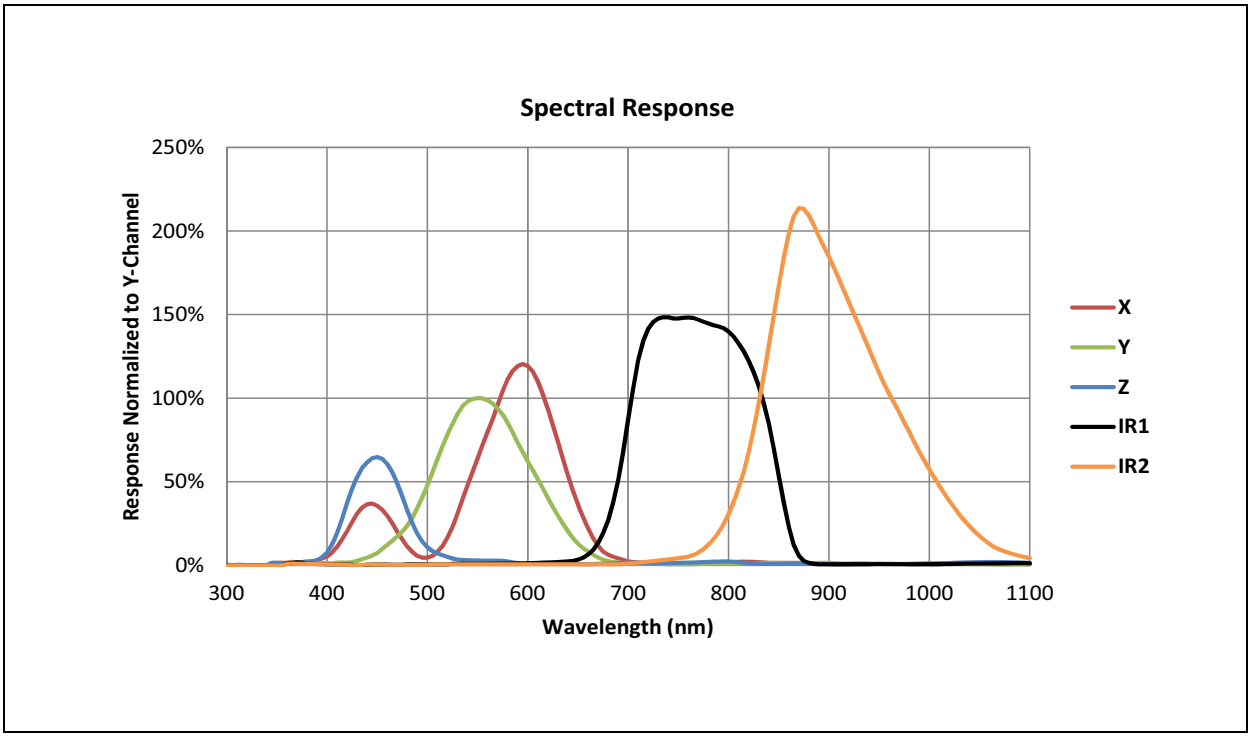
Note(s):

1. Filter parameters are measured on a production ongoing sample basis using diffused light.

Figure 10:
ALS Operating Characteristics, VDD = 1.8 V, T_A = 25°C, AGAIN = 16x, ATIME = 0x09 (27ms) (unless otherwise noted)

Parameter	Conditions	Min	Typ	Max	Units
Integration time step size		2.64	2.78	2.92	ms
Dark ADC count value	Ee = 0 µW/cm^2 AGAIN: 64x ATIME: 100ms (0x23)	0	1	3	counts
Gain scaling, relative to 1x gain setting	AGAIN: 4x		4		
	AGAIN: 16x		16		
	AGAIN: 64x		66		
	AGAIN: 128x		137		
ADC noise	AGAIN: 16x		0.005		% full scale

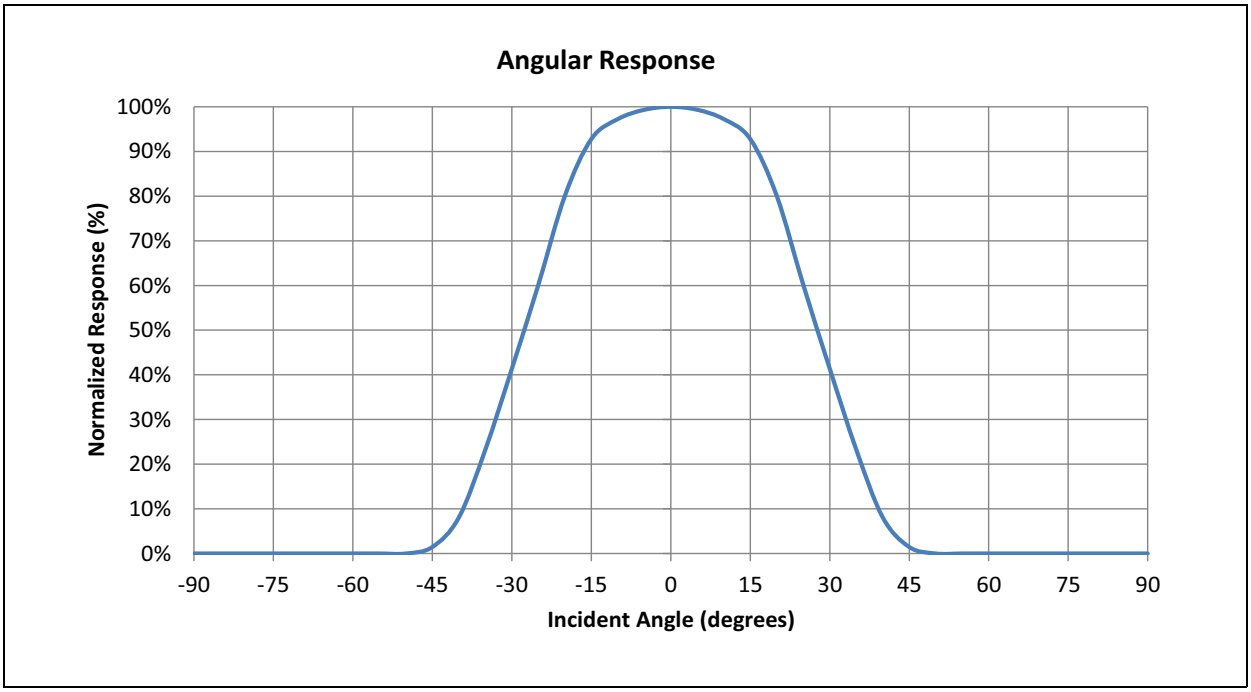
Figure 11:
Spectral Response



Note(s):

1. Response is measured with a diffuser on the surface of TCS3430 that matches the minimum recommended scattering characteristic shown in Figure 40.

Figure 12:
ALS Average Angular Response



Note(s):

1. Response is measured without a diffuser on the surface of TCS3430 that matches the minimum recommended scattering characteristic shown in Figure 40.

I²C Protocol

The device uses I²C serial communication protocol for communication. The device supports 7-bit chip addressing and both standard and full-speed clock frequency modes. Read and Write transactions comply with the standard set by Philips (now NXP).

Note(s): The I²C device address can be found in Ordering Information.

Internal to the device, an 8-bit buffer stores the register address location of the desired byte to read or write. This buffer auto-increments upon each byte transfer and is retained between transaction events (I.e. valid even after the master issues a STOP command and the I²C bus is released). During consecutive Read transactions, the future/repeated I²C Read transaction may omit the memory address byte normally following the chip address byte; the buffer retains the last register address +1.

All 16-bit fields have a latching scheme for reading and writing. In general it is recommended to use I²C bursts whenever possible, especially in this case when accessing two bytes of one logical entity. When reading these fields, the low byte must be read first, and it triggers a 16-bit latch that stores the 16-bit field. The high byte must be read immediately afterwards. When writing to these fields, the low byte must be written first, immediately followed by the high byte. Reading or writing to these registers without following these requirements will cause errors.

I²C Write Transaction

A Write transaction consists of a START, CHIP-ADDRESSWRITE, REGISTER-ADDRESS WRITE, DATA BYTE(S), and STOP. Following each byte (9TH clock pulse) the slave places an ACKNOWLEDGE/NOT- ACKNOWLEDGE (ACK/NACK) on the bus. If NACK is transmitted by the slave, the master may issue a STOP.

I²C Read Transaction

A Read transaction consists of a START, CHIP-ADDRESSWRITE, REGISTER-ADDRESS, RESTART, CHIP-ADDRESSREAD, DATA BYTE(S), and STOP. Following all but the final byte the master places an ACK on the bus (9TH clock pulse). Termination of the Read transaction is indicated by a NACK being placed on the bus by the master, followed by STOP.

The I²C bus protocol was developed by Philips (now NXP). For a complete description of the I²C protocol, please review the NXP I²C design specification.

Register Description

Figure 13:
Register Overview

Address	Register Name	R/W	Register Function	Reset Value
0x80	ENABLE	R/W	Enables states and interrupts	0x00
0x81	ATIME	R/W	ADC integration time	0x00
0x83	WTIME	R/W	ALS wait time	0x00
0x84	AILTL	R/W	ALS interrupt low threshold low byte	0x00
0x85	AILTH	R/W	ALS interrupt low threshold high byte	0x00
0x86	AIHTL	R/W	ALS interrupt high threshold low byte	0x00
0x87	AIHTH	R/W	ALS interrupt high threshold high byte	0x00
0x8C	PERS	R/W	ALS interrupt persistence filters	0x00
0x8D	CFG0	R/W	Configuration register zero	0x80
0x90	CFG1	R/W	Configuration register one	0x00
0x91	REVID	R	Revision ID	0x41
0x92	ID	R	Device ID	0xDC
0x93	STATUS	R	Device status register one	0x00
0x94	CH0DATAL	R	Z CH0 ADC Low Byte Register	0x00
0x95	CH0DATAH	R	Z CH0 ADC High Byte Register	0x00
0x96	CH1DATAL	R	Y Ch1 ADC Low Byte Register	0x00
0x97	CH1DATAH	R	Y CH1 ADC High Byte Register	0x00
0x98	CH2DATAL	R	IR1 - CH2 ADC Low Byte Register	0x00
0x99	CH2DATAH	R	IR1 - Ch2 ADC High Byte Register	0x00
0x9A	CH3DATAL	R	X or IR2 - CH3 ADC Low Byte Register	0x00
0x9B	CH3DATAH	R	X or IR2 - CH3 ADC High Byte Register	0x00
0x9F	CFG2	R/W	Configuration register two	0x04
0xAB	CFG3	R/W	Configuration register three	0x00
0xD6	AZ_CONFIG	R/W	Auto zero configuration	0x7F
0xDD	INTENAB	R/W	Interrupt enables	0x00

Note(s):

1. Register Access:
   R = Read Only
   W = Write Only
   R/W = Read or Write
   SC = Self Clearing after access

ENABLE Register (0x80)

Figure 14:
ENABLE Register

0x80: ENABLE				
Field	**Name**	**Reset**	**Type**	**Description**
7:4	RESERVED	0	RW	Reserved
3	WEN	0	RW	Wait Enable. This bit activates the wait feature. Writing a one actives the wait timer. Writing a zero disables the wait timer.
2	RESERVED	0	RW	Reserved
1	AEN	0	RW	ALS Enable. This bit actives the ALS function. Set aen=1 and pon=1 in the same command to ensure autozero function is run prior to the first measurement.
0	PON	0	RW	Power ON. This field activates the internal oscillator to permit the timers and ADC channels to operate. Writing a one activates the oscillator. Writing a zero disables the oscillator.

The mode/parameter fields should be written before AEN is asserted. The function AEN requires PON to be asserted to operate correctly.

ATIME Register (0x81)

Figure 15:
ATIME Register

<table>
<tr><th colspan="5">0x81: ATIME</th></tr>
<tr><th>Field</th><th>Name</th><th>Reset</th><th>Type</th><th>Description</th></tr>
<tr><td rowspan="9">7:0</td><td rowspan="9">ATIME</td><td rowspan="9">0x00</td><td rowspan="9">RW</td><td>Integration Time. Eight bit value that specifies the integration time in 2.78ms intervals. 0x00 indicates 2.78ms, 0x01 indicates 5.56ms. The maximum ALS value depends on the integration time. For every 2.78ms, the maximum value increases by 1024. This means that to be able to reach ALS full scale, the integration time has to be at least 64*2.78ms.</td></tr>
<tr><td>
<table>
<tr><th>Value</th><th>Integration Cycles</th><th>Integration Time</th><th>Maximum ALS Value</th></tr>
<tr><td>0x00</td><td>1</td><td>2.78ms</td><td>1023</td></tr>
<tr><td>0x01</td><td>2</td><td>5.56ms</td><td>2047</td></tr>
<tr><td>...</td><td>...</td><td>...</td><td>...</td></tr>
<tr><td>0x11</td><td>18</td><td>50ms</td><td>18431</td></tr>
<tr><td>0x40</td><td>65</td><td>181ms</td><td>65535</td></tr>
<tr><td>...</td><td>...</td><td>...</td><td>...</td></tr>
<tr><td>0xff</td><td>256</td><td>711ms</td><td>65535</td></tr>
</table>
</td></tr>
</table>

The ATIME register controls the integration time of the ALS ADCs.

The timer is implemented with a down counter with 0x00 as the terminal count. The timer is clocked at a 2.78ms nominal rate. Loading 0x00 will generate a 2.78ms integration time, loading 0x01 will generate a 5.56ms integration time, and so forth.

WTIME Register (0x83)

Figure 16:
WTIME Register

0x83: WTIME						
Field	Name	Reset	Type	Description		
7:0	WTIME	0x00	RW	ALS Wait Time. Eight bit value that specifies the time in 2.78ms to wait between ALS cycles.		
				Value	**Wait Cycles**	**Wait Time**
				0x00	1	2.78ms/ 33.4ms
				0x01	2	5.56ms/ 66.7ms
				...	...	...
				0x23	36	100ms/ 1.20s
				...	...	...
				0xff	256	711ms/ 8.53s

The wait timer is implemented with an down counter with 0x00 as the terminal count. Loading 0x00 will generate a 2.78ms wait time, loading 0x01 will generate a 5.56ms wait time, and so forth; By asserting wlong, in register 0x8D the wait time is given in multiples of 33.4ms (12x).

AILTL Register (0x84)

Figure 17:
AILTL Register

0x84: AILTL				
Field	Name	Reset	Type	Description
7:0	AILTL	0x00	RW	Low Byte of the Low Threshold

This register provides the low byte of the low interrupt ALS (Channel 0) threshold.

AILTH Register (0x85)

Figure 18:
AILTH Register

0x85: AILTH				
Field	Name	Reset	Type	Description
7:0	AILTH	0x00	RW	High Byte of the Low Threshold

This register provides the high byte of the low interrupt ALS (Channel 0) threshold.

The contents of the AILTH and AILTL registers are combined and treated as a sixteen bit threshold. If the value generated by Channel 0 is below the low threshold specified and the APERS value is reached, the aint bit is asserted which will assert the INT pin if aien is set.

There is an 8-bit data latch implemented that stores the written low byte until the high byte is written. Both bytes will be applied then at the same time to avoid an invalid threshold (e.g. when going from 0x00ff to 0x0100, the invalid intermediate value 0x0000 is suppressed. This implies that 1) the LSB cannot be changed without writing to the MSB and 2) that writing to the LSB of one 16-bit value and afterwards to the MSB of another 16-bit register will write all 16 bits to the MSB related register.

AIHTL Register (0x86)

Figure 19:
AIHTL Register

0x86: AIHTL				
Field	Name	Reset	Type	Description
7:0	AIHTL	0	RW	Low Byte of the High Threshold

This register provides the low byte of the high interrupt threshold.

AIHTH Register (0x87)

Figure 20:
AIHTH Register

0x87: AIHTH				
Field	Name	Reset	Type	Description
7:0	AIHTH	0	RW	High Byte of the High Threshold

This register provides the low byte of the high interrupt threshold.

The contents of the AIHTH and AIHTL registers are combined and treated as a sixteen bit threshold. If the value generated by Channel 0 is above the high threshold specified and the APERS value is reached, the aint bit is asserted which will assert the INT pin if aien is set.

PERS Register (0x8C)

Figure 21:
PERS Register

0x8C: PERS					
Field	**Name**	**Reset**	**Type**	**Description**	
7:4	RESERVED	0	RW	Reserved	
3:0	APERS	0	RW	**Value**	**Interrupt Generated When...**
				0	Every ALS cycle
				1	Any ALS value outside of threshold range
				2	2 consecutive ALS values out of range
				3	3 consecutive ALS values out of range
				4	5...
				5	10...
				6	15...
				7	20...
				12	45...
				13	50...
				14	55...
				15	60 consecutive ALS values out of range

This register controls the interrupt filtering capabilities of the device. Configurable filtering is provided to allow interrupts to be generated after either an ALS integration cycle or if the integration cycle has produced a result that is outside of the values specified by threshold register for some specified number of times.

ALS interrupts are generated by looking only at the ADC integration results of Channel 0 photodiode.

CFG0 Register (0x8D)

Figure 22:
CFG0 Register

0x8D: CFG0				
Field	**Name**	**Reset**	**Type**	**Description**
7:3	RESERVED	1 0 0 0 0	RW	Reserved. Must be set to 10000.
2	WLONG	0	RW	Wait Long. When asserted, the wait cycle is increased by a factor 12x from that programmed in the WTIME register.
1:0	RESERVED	0 0	RW	Reserved. Must be set to 00.

CFG1 Register (0x90)

Figure 23:
CFG1 Register

0x90: CFG1					
Field	**Name**	**Reset**	**Type**	**Description**	
7:4	RESERVED	0	RW	Reserved	
3	AMUX	0	RW	ALS Multiplexer. Sets the CH3 input. Default = 0 (X Channel). Set to 1 to read IR2.	
2	RESERVED	0	RW	Reserved	
1:0	AGAIN	0	RW	ALS Gain Control. Sets the gain of the ALS DAC.	
				Field Value	**Gain**
				00	1x
				01	4x
				10	16x
				11	64x

CFG1 Register: Register CFG1 sets the gain level for ALS measurements. The valid range of values is 0x00 - 0x03.

REVID Register (0x91)

Figure 24:
REVID Register

0x91: REVID				
Field	Name	Reset	Type	Description
7:3	RESERVED	01000	RO	Reserved
2:0	REV_ID	001	RO	Revision Number Identification

ID Register (0x92)

Figure 25:
ID Register

0x92: ID					
Field	Name	Reset	Type	Description	
7:2	ID	110111	RO	Part Number Identification	
				Value	**Meaning**
				110111	TCS3430
1:0	RESERVED	00	RO	Reserved	

STATUS Register (0x93)

Figure 26:
STATUS Register

0x93: STATUS				
Field	Name	Reset	Type	Description
7	ASAT	0	R, SC	ALS Saturation. This flag is set for analog saturation writing a 1 will clear this status flag.
6:5	RESERVED	0	R, SC	Reserved
4	AINT	0	R, SC	ALS Interrupt. Indicates that the device is asserting an ALS interrupt. writing a 1 will clear this status flag.
3:0	RESERVED	0	R, SC	Reserved

CH0DATAL Register (0x94)

Figure 27:
CH0DATAL Register

0x94: CH0DATAL				
Field	Name	Reset	Type	Description
7:0	CH0DATAL	0	RO	Low Byte of CH0 ADC data. Contains Z data.

CH0DATAH Register (0x95)

Figure 28:
CH0DATAH Register

0x95: CH0DATAH				
Field	Name	Reset	Type	Description
7:0	CH0DATAH	0	RO	High Byte of CH0 ADC data. Contains Z data.

CH1DATAL Register (0x96)

Figure 29:
CH1DATAL Register

0x96: CH1DATAL				
Field	Name	Reset	Type	Description
7:0	CH1DATAL	0	RO	Low Byte of CH1 ADC data. Contains Y data.

CH1DATAH Register (0x97)

Figure 30:
CH1DATAH Register

0x97: CH1DATAH				
Field	Name	Reset	Type	Description
7:0	CH1DATAH	0	RO	High Byte of CH1 ADC data. Contains Y data.

CH2DATAL Register (0x98)

Figure 31:
CH2DATAL Register

0x98: CH2DATAL				
Field	Name	Reset	Type	Description
7:0	CH2DATAL	0	RO	Low Byte of CH2 ADC data. Contains IR1 data.

CH2DATAH Register (0x99)

Figure 32:
CH2DATAH Register

0x99: CH2DATAH				
Field	Name	Reset	Type	Description
7:0	CH2DATAH	0	RO	High Byte of CH2 ADC data. Contains IR1 data.

CH3DATAL Register (0x9A)

Figure 33:
CH3DATAL Register

0x9A: CH3DATAL				
Field	**Name**	**Reset**	**Type**	**Description**
7:0	CH3DATAL	0	RO	Low Byte of CH3 ADC data. If AMUX = 0 contains X data. If AMUX = 1 contains IR2 data. Default = X data.

CH3DATAH Register (0x9B)

Figure 34:
CH3DATAH Register

0x9B: CH3DATAH				
Field	**Name**	**Reset**	**Type**	**Description**
7:0	CH3DATAH	0	RO	High Byte of CH3 ADC data. If AMUX = 0 contains X data. If AMUX = 1 contains IR2 data. Default = X data.

CFG2 Register (0x9F)

Figure 35:
CFG2 Register

0x9F: CFG2				
Field	**Name**	**Reset**	**Type**	**Description**
7:5	Reserved	000	RW	Reserved. Set to 000.
4	HGAIN	0	RW	High 128x gain. If this bit is set and AGAIN in the CFG1 register is set to 11, then the 128x gain mode will be enabled.
3:0	Reserved	0100	RW	Reserved. Set to 0100.

CFG3 Register (0xAB)

Figure 36:
CFG3 Register

<table>
<tr><th colspan="8">0xAB: CFG3</th></tr>
<tr><th>Field</th><th>Name</th><th>Reset</th><th>Type</th><th colspan="4">Description</th></tr>
<tr><td>7</td><td>INT_READ_CLEAR</td><td>0</td><td>RW</td><td colspan="4">If this bit is set, all flag bits in the STATUS register will be reset whenever the STATUS register is read over I^{2}C.</td></tr>
<tr><td>6:5</td><td>RESERVED</td><td>0</td><td>RW</td><td colspan="4">Reserved. Set to 0.</td></tr>
<tr><td rowspan="7">4</td><td rowspan="7">SAI</td><td rowspan="7">0</td><td rowspan="7">RW</td><td colspan="4">Sleep After Interrupt. Power down the device at the end of the ALS cycle if an interrupt has been generated. (1)</td></tr>
<tr><td>PON</td><td>SAI</td><td>INT (low active)</td><td>Oscillator</td></tr>
<tr><td>0</td><td>x</td><td>x</td><td>OFF</td></tr>
<tr><td>1</td><td>0</td><td>x</td><td>ON</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>ON</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>OFF
(SAI induced sleep)</td></tr>
<tr><td colspan="4">The way to “wake up” the device from SAI-sleep is by clearing the interrupt register 0x93.</td></tr>
<tr><td>3:0</td><td>RESERVED</td><td>0</td><td>RW</td><td colspan="4">Reserved. Set to 0.</td></tr>
</table>

Note(s):

1. SAI does not modify any register bits directly, it rather uses the interrupt signal to turn OFF the oscillator.

AZ_CONFIG Register (0xD6)

Figure 37:
AZ_CONFIG Register

0xD6: AZ_CONFIG				
Field	**Name**	**Reset**	**Type**	**Description**
7	AZ_MODE	0	RW	0: Always start at zero when searching the best offset value 1: Always start at the previous (offset_c) with the auto-zero mechanism (1)
6:0	AZ_NTH_ ITERATION	0x7F	RW	Run autozero automatically every nth ALS iteration (0=never, 7Fh=only at first ALS cycle, n=every nth time)

Note(s):

1. On average mode 1 is faster, but in the worst case, mode 0 is faster.

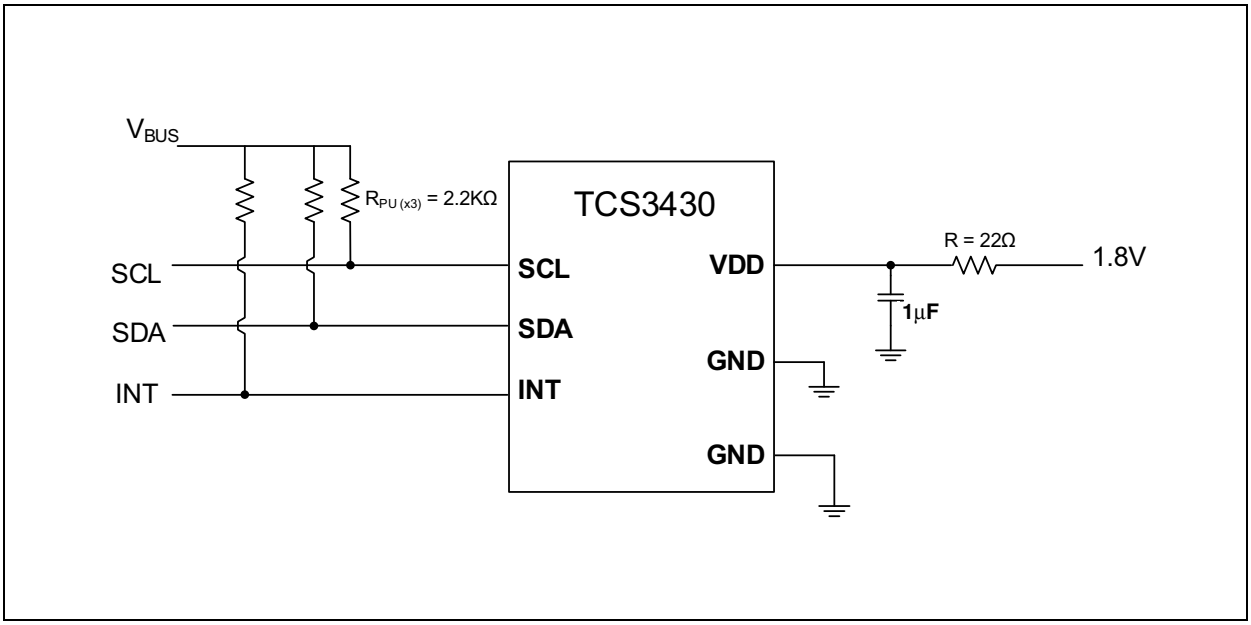
INTENAB Register (0xDD)

Figure 38:
INTENAB Register

0xDD: INTENAB				
Field	**Name**	**Reset**	**Type**	**Description**
7	ASIEN	0	RW	Writing '1' to this bit enables ASAT interrupt.
6:5	RESERVED	0	RW	Reserved
4	AIEN	0	RW	Writing '1' to this bit enables ALS interrupt.
3:0	RESERVED	0	RW	Reserved

Application Information

Figure 39:
Typical Application Hardware Circuit



Note(s):

1. Place the 1µF capacitors as close as possible to the module.
2. V_{DD} = 1.8V, V_{BUS} = 1.8V.
3. The N/C pins (5 and 6) that are not indicated in the circuit diagram may be connected to GND or not connected (remain open).

Application Optical Requirements

For optimal performance an achromatic diffuser shall be placed above the device aperture. The recommended solution is a bulk diffuser that meets the minimum recommended scattering characteristic shown below. For more details refer to the Optical Design Guide or contact **ams**.

Figure 40:
Diffuser Characteristics